

## **Supporting Information**

### **Charge Noise in Low Schottky Barrier Multilayer Tellurium Field-Effect Transistors**

Shubhadip Moulick\*<sup>1</sup>, Dipanjan Maity<sup>1, 2</sup>, Gaurab Samanta<sup>1</sup>, Kalyan Mandal<sup>1</sup>

and Atindra Nath Pal\*<sup>1</sup>

<sup>1</sup>*Department of Condensed Matter and Materials Physics, S. N. Bose National Centre for Basic Sciences, Sector III, Block JD, Salt Lake, Kolkata 700106, India*

<sup>2</sup>*Jawaharlal Nehru Centre for Advanced Scientific Research (JNCASR)  
Rachenahalli Lake Rd, Jakkur, Bengaluru, Karnataka 560064*

\*Email. [moulick.shubhadip94@gmail.com](mailto:moulick.shubhadip94@gmail.com), [atin@bose.res.in](mailto:atin@bose.res.in)

## 1. Synthesis of 2D Tellurium:

Maintaining the standard procedure described by Javey's group<sup>1</sup>, we have synthesized the hydrothermal 2D Tellurium by dissolving 1.5 g of poly(vinylpyrrolidone) (PVP) and 46 mg of sodium tellurite ( $\text{Na}_2\text{TeO}_3$ ) in 16 ml of deionized (DI) water at room temperature under magnetic stirring to form a homogeneous transparent solution. Subsequently, 1.66 ml of ammonium hydroxide ( $\text{NH}_4\text{OH}$ ) and 0.838 ml of hydrazine monohydrate ( $\text{N}_2\text{H}_4$ ) were sequentially added to the prepared solution. The resulting mixture was then transferred into a 25 ml Teflon-lined stainless-steel autoclave, which was sealed and heated from room temperature to 220°C at a ramp rate of 3°C/min, maintaining this temperature for 4 hours. After the reaction period, the autoclave was cooled to room temperature using running water. The final silver-gray-colored product was precipitated by centrifugation at 5000 rpm for 5 minutes, followed by three washes with DI water to remove residual ions. The product was then re-dispersed in pure ethanol and subsequently drop-casted onto a silicon/silicon dioxide ( $\text{Si}/\text{SiO}_2$ ) substrate for characterization and device fabrication.

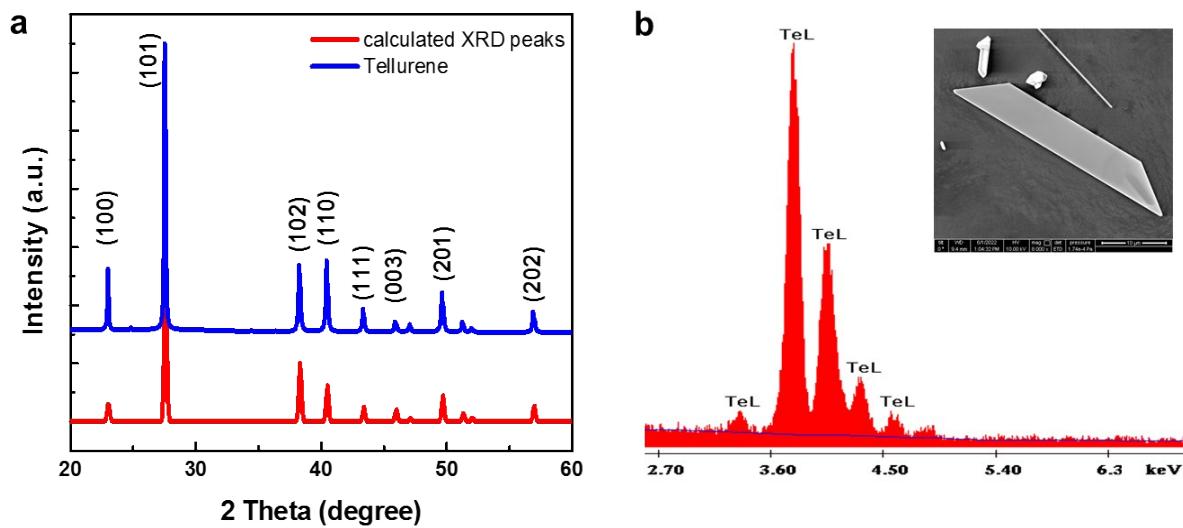
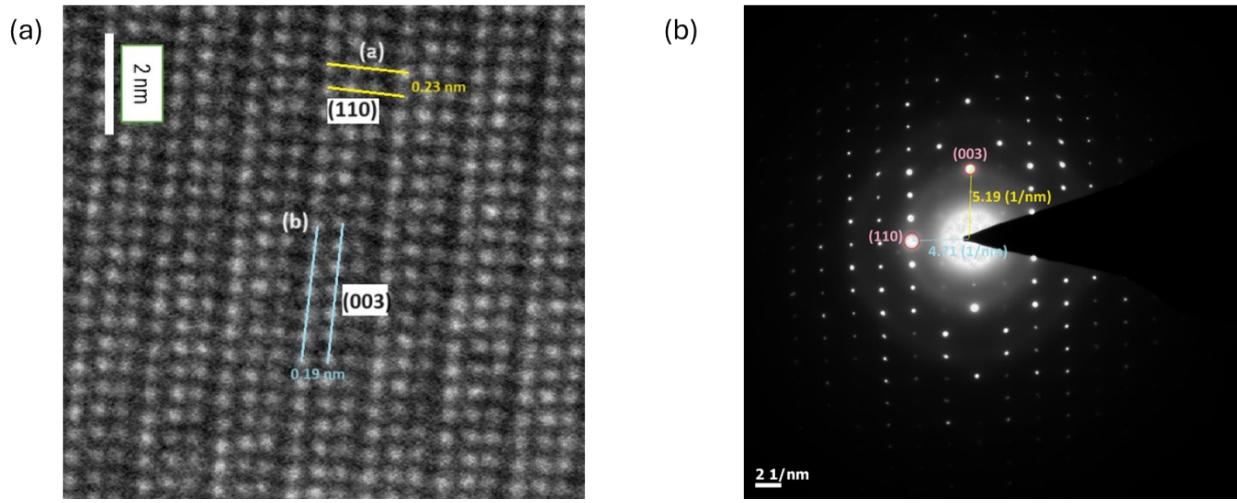


Figure S1. (a) XRD pattern of the dried 2D Tellurium flakes. (b) EDX spectrum of the prepared 2D Tellurium flakes. (Inset) Scanning electron microscope image of the 2D Tellurium flake.

## 2. 2D Tellurium characterization

The X-ray diffraction (XRD) patterns of the synthesized Te flakes (**Figure 5.2a**) Prominent peaks located at  $23^\circ$ ,  $27.6^\circ$ ,  $38.3^\circ$ ,  $40.4^\circ$ ,  $43.3^\circ$ ,  $45.8^\circ$ ,  $49.6^\circ$ ,  $56.9^\circ$ , and  $63.8^\circ$ , which correspond to the (100), (101), (102), (110), (111), (003), (201), and (202) planes in the hexagonal Te



*Figure S2. (a) TEM images of multilayer 2D Tellurium where inter planar spacing is shown. (b) SAED pattern of 2D Tellurium flake.*

structure, respectively .The full-width-half-maximums of the main peaks were narrow, indicating that a high-quality Te structure was attained<sup>2</sup>. The EDX spectra shows the characteristics Te spectrum, and no other peaks are observed which signifies the high purity of the sample.

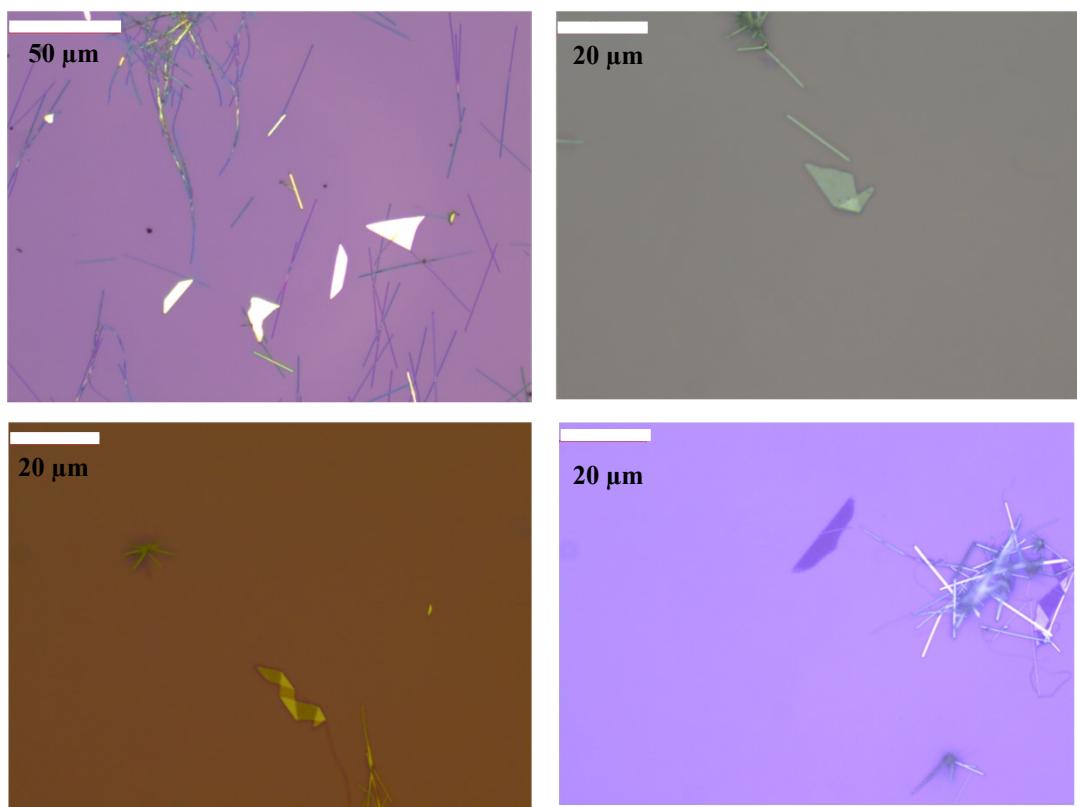


Figure S3. Optical Images of the synthesized 2D Tellurium flakes, showing a variation of the lateral dimension of the 2D Tellurium flakes

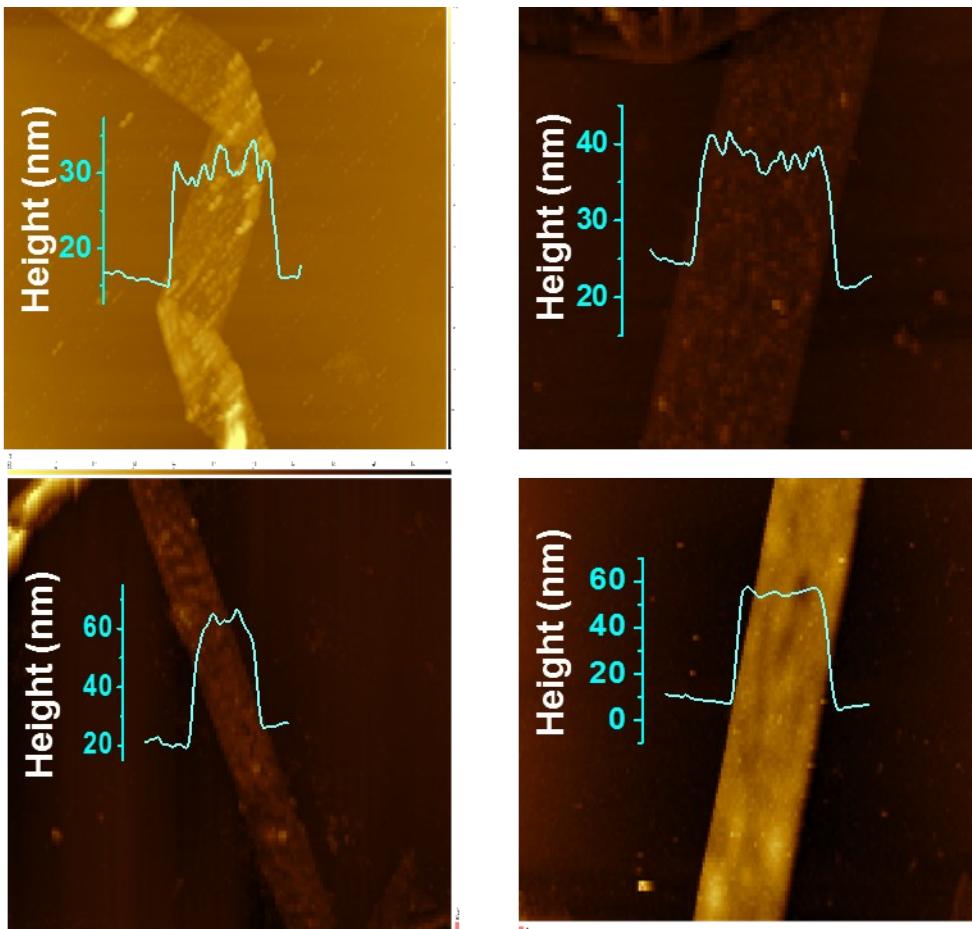


Figure S4. AFM image of the various multilayer 2D Tellurium flakes showing a variation of height from 15-60 nm.

### 3. Device fabrication and transport measurement details.

Te flakes were transferred onto a Si/SiO<sub>2</sub> substrate with a 300 nm oxide layer. Optical lithography was performed using Microtech LW405 laser writer by exposing positive photoresist (AZ-1512-HS), followed by metallization in an electron beam evaporator at high vacuum ( $\sim 1\text{e-}7$  mbar) and lift-off process with hot acetone. Finally, the devices were bonded with 25  $\mu\text{m}$  gold wire.

All electronic transport and noise measurements were performed inside a custom-made high-vacuum cryogenic insert. The temperature during measurement was controlled using a Lakeshore 340 temperature controller. The measurements were conducted in a two-probe configuration, with the back gate applied through the highly doped Si/SiO<sub>2</sub> substrate using a source measuring unit (Model 2450, Keithley Instruments). The drain current was measured using a standard lock-in amplifier (MFLI, Zurich Instruments) by applying a constant ac bias of 10-100 mV at a carrier frequency of  $\sim 223$  Hz. Noise measurements were conducted with the same lock-in

amplifier featuring a built-in data acquisition system, following the procedure outlined in ref (3) and (4).

#### 4. Transfer characteristics of additional devices

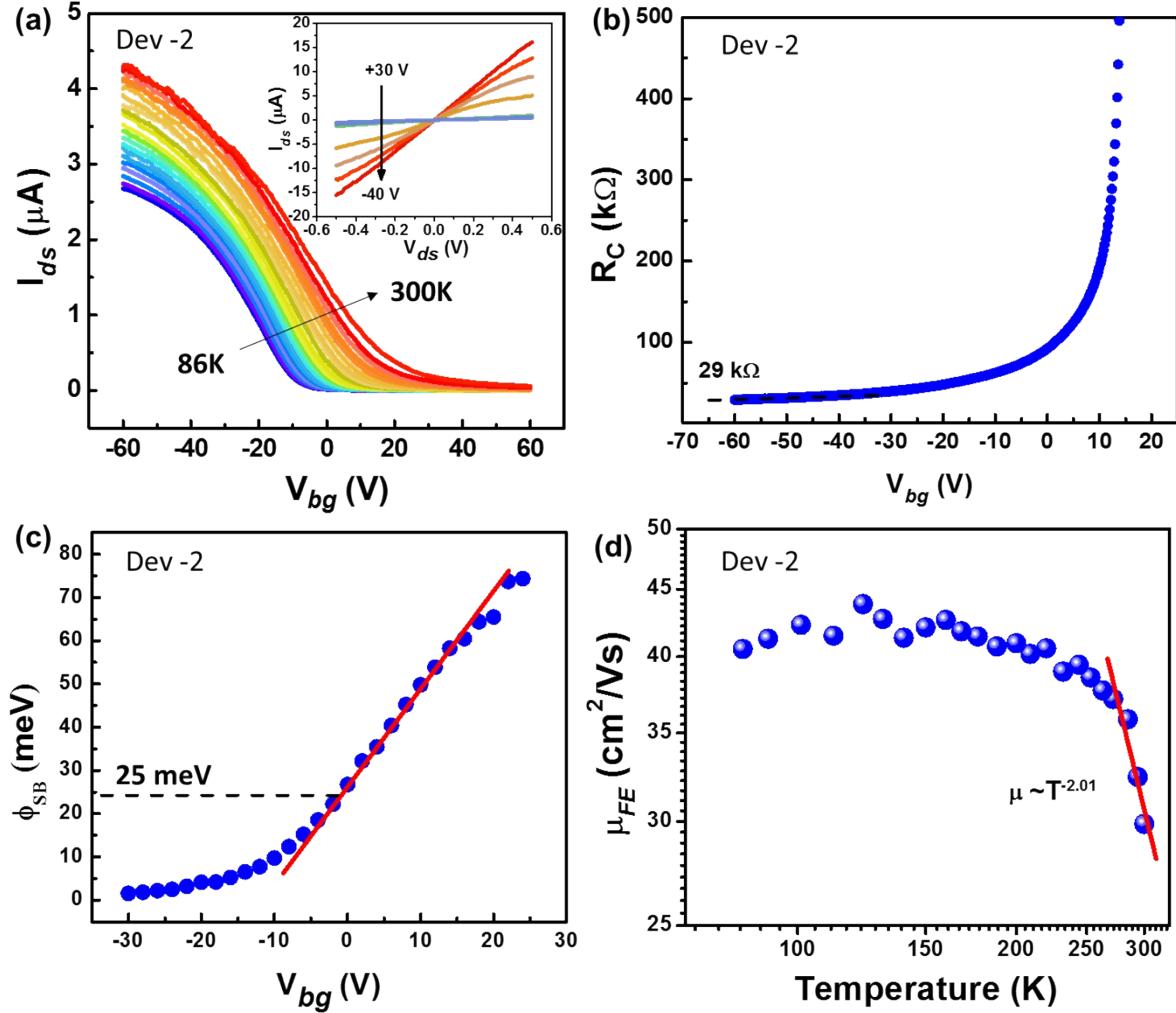


Figure S5. (a) Transfer characteristics of a Cr/Au contacted low mobility Te device at different temperature. Inset shows the  $I_{ds}$ - $V_{ds}$  plots for different gate voltages at 300 K. (b) Variation of contact resistance with gate voltage, calculated using Y-function method. (c) Calculated Schottky barrier ( $\phi_{SB}$ ) height at different gate voltages. (d) Variation of field effect mobility with temperature, with red solid line being the fit to the high temperature data following  $\mu \approx T^{-2.01}$ .

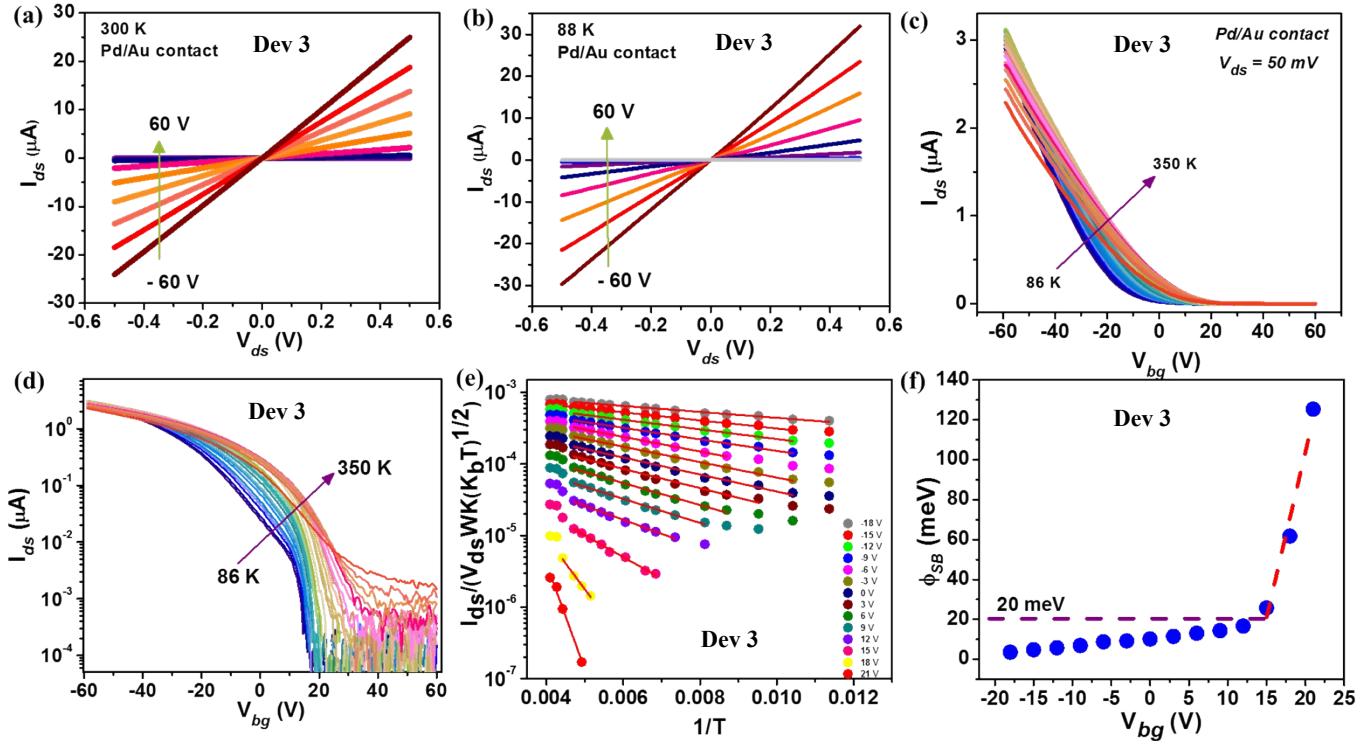


Figure S6.  $I_{ds}$ - $V_{ds}$  characteristics at different gate voltages for the Pd/Au contacted Te device (Dev 3) at (a) 300 K and (b) 88 K, exhibiting linear behavior. (c) Transfer characteristics at different temperatures, displaying metal-insulator transition at high gate voltages. (d) Transfer characteristics in semi-log scale demonstrating the increase in the  $I_{on}/I_{off}$  ratio from  $\sim 10^3$  to  $\sim 10^5$ . (e) Arrhenius-type plots of  $I_{off}$  vs.  $1/T$  at different  $V_{bg}$ . (f) Variation of the extracted barrier heights for Pd/Au contacted device at different gate voltages.

## 5. Additional Noise Data from Dev 1

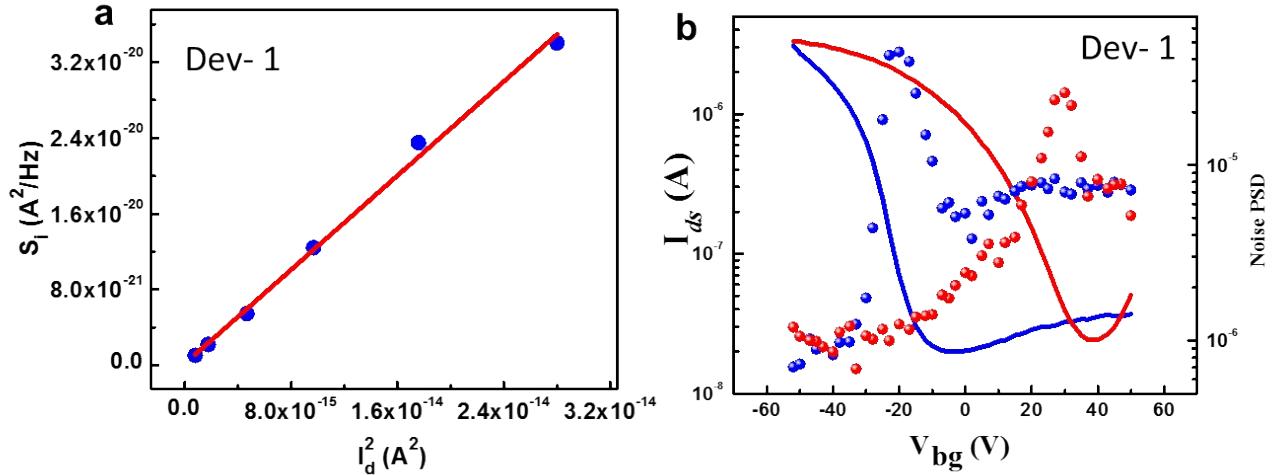


Figure S7. (a) Variation of noise power spectral density,  $S_I$  with the square of the drain current, exhibiting linear behavior (b) Variation of drain source current during noise measurement (blue and red lines) when the back-gate voltage sweeps from -ve to +ve gate voltage (blue lines) and vice versa. Blue and Red dots show the corresponding normalized PSD integrated over the experimental bandwidth.

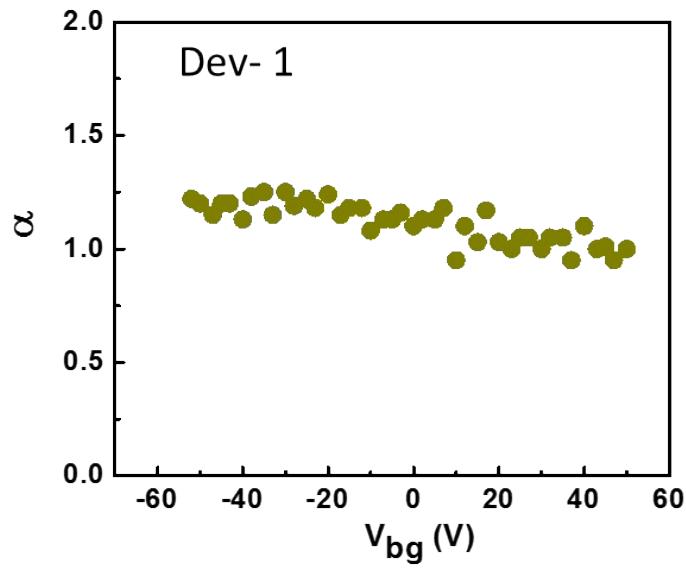


Figure S8. Variation of  $\alpha$  with gate voltage for Dev 1.

## 6. Noise in Pd/Au contacted device

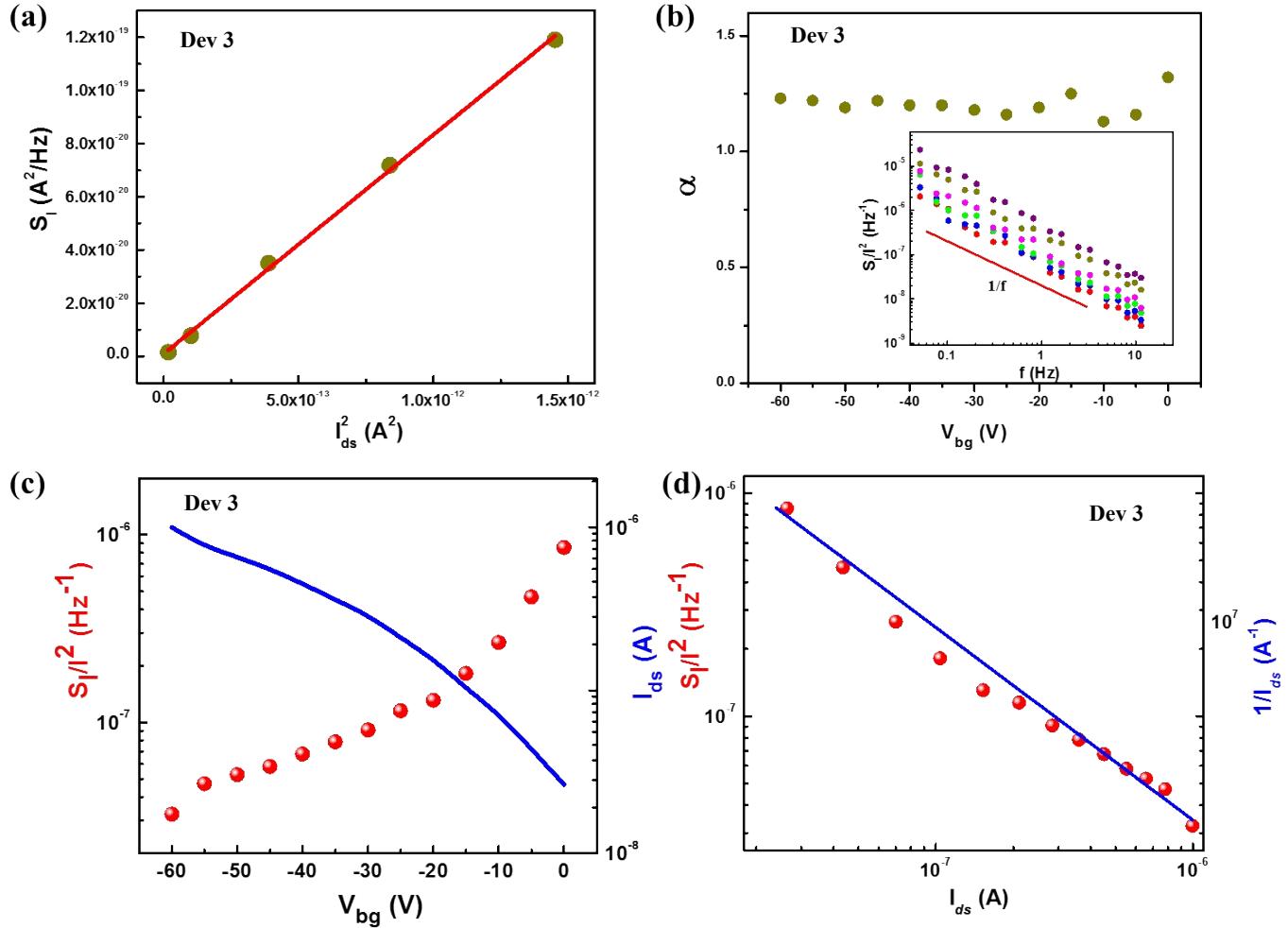


Figure S9. (a) Variation of noise power spectral density,  $S_I$  with the square of the drain current for Pd/Au contacted device, exhibiting linear behavior. (b)  $\alpha$  varies close to unity in all the gate voltages (Inset shows Noise power spectra  $S_I/I^2$  at various  $V_{bg}$ , showing  $1/f$  characteristics). (c) Variation of normalized noise PSD calculated at 1Hz (red data points) and the source drain current (blue line) with  $V_{bg}$ . A clear decrease in the noise at higher gate voltage is observed. (d) Variation of Noise PSD at 1 Hz (Red dots) and the variation of  $1/I_{ds}$  (Blue line) is plotted with  $I_{ds}$ , Noise PSD follows the trend of  $1/I_{ds}$  confirming the Hooge's mobility fluctuation model.

## 7. Y-Function method for calculating contact resistance ( $R_C$ )

The Y- function method is a common method to calculate the contact resistance ( $R_C$ ) of a 2D semiconducting system used instead of TLM method.

According to Y-function method the drain current can be expressed as <sup>5,6</sup>

$$I_d = \frac{W}{L} C_{ox} (V_g - V_T) \frac{\mu_0}{1 + \theta(V_g - V_T)} V_{ds}$$

$$\beta = \mu_0 C_{ox} \frac{W}{L}$$

Where  $I_d$ ,  $V_{ds}$ ,  $C_{ox}$ , are the drain current , drain bias, oxide capacitance accordingly.  $W$  and  $L$  are the width and length of the sample.

The channel mobility degradation factor ( $\theta$ ) can be expressed as

$$\theta = \theta_0 + \mu_0 C_{ox} \frac{W}{L} R_C = \theta_0 + \beta R_C$$

where  $\theta_0$  is intrinsic degradation coefficient of mobility, and it is very small that it can be ignored under normal condition. Therefore, we should only consider effect of  $R_C$  on degradation of mobility.

The Y-function is defined as

$$Y = \frac{I_d}{\sqrt{g_m}} = \sqrt{\beta V_d} (V_g - V_T)$$

$$g_m = \frac{dI_d}{dV_g} = \beta \frac{V_d}{[1 + \theta(V_g - V_T)^2]}$$

Where  $g_m$  is the transconductance.

Combining the above equation the contact resistance can be calculated using the following formula

$$R_C = \frac{\theta}{\beta} = \frac{V_d}{I_d} - \frac{1}{\beta(V_g - V_T)}$$

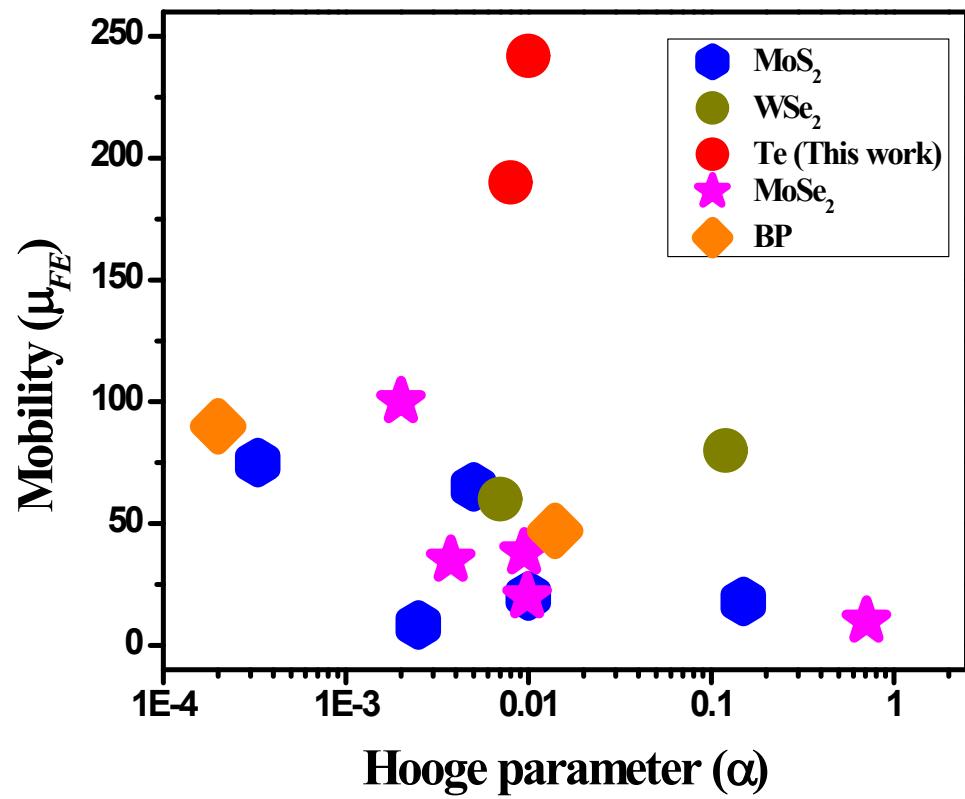


Figure S10. Graph shows the comparison between mobility and Hooge parameter between various 2D materials.

**Table 1 Comparison of Mobility and Hooge parameter reported in different samples.**

Sample name	Thickness	Mobility ( $\mu$ ) ( $\text{cm}^2/\text{Vs}$ )	Hooge Parameter ( $\alpha_H$ )	Reference
MoS <sub>2</sub>	50 nm	20.27	0.01	<sup>7</sup>
MoS <sub>2</sub>	Single layer	65	0.005	<sup>8</sup>
MoS <sub>2</sub>	Single layer	18	0.15	<sup>9</sup>
WSe <sub>2</sub>	27 nm	80	0.12	<sup>10</sup>
WSe <sub>2</sub>	50 nm	60	0.007	<sup>11</sup>
MoSe <sub>2</sub>	10 nm	100	0.002	<sup>12</sup>
MoSe <sub>2</sub>	6.2 nm	10	0.708	<sup>13</sup>
ReS <sub>2</sub>	7 nm	0.3	$2 \times 10^{-6}$	<sup>14</sup>
BP	8.6 nm	47	0.014	<sup>15</sup>
BP	7.5 nm	90	$2 \times 10^{-4}$	<sup>16</sup>
Te	20 nm (Cr/Au)	242	0.01	This work
Te	20 nm (Pd/Au)	190	0.008	This work

**Table 2. Comparison of Mobility and  $I_{on}/I_{off}$  ratio reported in Tellurium grown by various synthesis technique.**

Synthesis Method	Thickness (nm)	Field effect mobility (cm <sup>2</sup> /Vs)	$I_{on}/I_{off}$	References
Thermal evaporation	8	35	$10^4$	17
Thermal evaporation	5	100	$10^4$	18
Magnetron sputtering	4	52	$10^4$	19
Atomic layer deposition (ALD)	15	7.6	$10^4$	20
Physical Vapor deposition (PVD)	N.A.	145	$10^3$	21
Chemical Vapor Deposition (CVD)	N.A	500	2.5	22
Hydrothermal	10-30	200-700	$10^4$ - $10^3$	2,23-25
Hydrothermal	~ 20	182-242	$10^2$ - $10^4$	This Work

## References

(1) Amani, M.; Tan, C.; Zhang, G.; Zhao, C.; Bullock, J.; Song, X.; Kim, H.; Shrestha, V. R.; Gao, Y.; Crozier, K. B.; Scott, M.; Javey, A. Solution-Synthesized High-Mobility Tellurium Nanoflakes for Short-Wave Infrared Photodetectors. *ACS Nano* **2018**, *12* (7), 7253–7263.  
<https://doi.org/10.1021/acsnano.8b03424>.

(2) Wang, Y.; Qiu, G.; Wang, R.; Huang, S.; Wang, Q.; Liu, Y.; Du, Y.; Goddard, W. A.; Kim, M. J.; Xu, X.; Ye, P. D.; Wu, W. Field-Effect Transistors Made from Solution-Grown Two-Dimensional Tellurene. *Nat. Electron.* **2018**, *1* (4), 228–236. <https://doi.org/10.1038/s41928-018-0058-4>.

(3) Ghosh, A.; Kar, S.; Bid, A.; Raychaudhuri, A. K. A Set-up for Measurement of Low Frequency Conductance Fluctuation (Noise) Using Digital Signal Processing Techniques. **2004**, 1–25. <https://doi.org/10.48550/arXiv.cond-mat/0402130>.

(4) Moulick, S.; Alam, R.; Pal, A. N. Sensing Remote Bulk Defects through Resistance Noise in a Large-Area Graphene Field-Effect Transistor. *ACS Appl. Mater. Interfaces* **2022**, *14*, 51105–51112. <https://doi.org/10.1021/acsami.2c14499>.

(5) Park, J. Y.; Joe, H. E.; Yoon, H. S.; Yoo, S.; Kim, T.; Kang, K.; Min, B. K.; Jun, S. C. Contact Effect of ReS<sub>2</sub>/Metal Interface. *ACS Appl. Mater. Interfaces* **2017**, *9* (31), 26325–26332. <https://doi.org/10.1021/acsami.7b06432>.

(6) Li, W.; Jia, Q.; Dong, H.; Wang, Z.; Wang, Y.; Wu, Y.; Zhao, X.; Chen, Z.; Wang, S. ReS<sub>2</sub> Nanosheet-Based Channels for Two-Dimensional Field Effect Transistors and Phototransistors with High Photoresponsivity. *ACS Appl. Nano Mater.* **2023**, *6* (1), 512–522. <https://doi.org/10.1021/acsanm.2c04600>.

(7) Kwon, H. J.; Kang, H.; Jang, J.; Kim, S.; Grigoropoulos, C. P. Analysis of Flicker Noise in Two-Dimensional Multilayer MoS<sub>2</sub> Transistors. *Appl. Phys. Lett.* **2014**, *104* (083110). <https://doi.org/10.1063/1.4866785>.

(8) Renteria, J.; Samnakay, R.; Rumyantsev, S. L.; Jiang, C.; Goli, P.; Shur, M. S.; Balandin, A. A. Low-Frequency 1/f Noise in MoS<sub>2</sub> Transistors: Relative Contributions of the Channel and Contacts. *Appl. Phys. Lett.* **2014**, *104* (153104). [https://doi.org/https://doi.org/10.1063/1.4871374](https://doi.org/10.1063/1.4871374).

(9) Kim, J. K.; Song, Y.; Kim, T. Y.; Cho, K.; Pak, J.; Choi, B. Y.; Shin, J.; Chung, S.; Lee, T. Analysis of Noise Generation and Electric Conduction at Grain Boundaries in CVD-Grown MoS<sub>2</sub> Field Effect Transistors. *Nanotechnology* **2017**, *28* (47LT01 (7pp)). <https://doi.org/10.1088/1361-6528/aa9236>.

(10) Ko, S. P.; Piao, M.; Jang, H. K.; Shin, J. M.; Jin, J. E.; Kim, D. H.; Kim, G. T.; Cho, J. Low Frequency Noise Reduction in Multilayer WSe<sub>2</sub> Field Effect Transistors. *Appl. Phys. Lett.* **2015**, *106* (023504). <https://doi.org/10.1109/NANO.2015.7388820>.

(11) Cho, I. T.; Kang, W. M.; Roh, J.; Lee, C.; Jin, S. H.; Lee, J. H. Temperature Effects on Current-Voltage and Low Frequency Noise Characteristics of Multilayer WSe<sub>2</sub> FETs. *Proc. Int. Symp. Phys. Fail. Anal. Integr. Circuits, IPFA* **2015**, *2015-Augus*, 480–483. <https://doi.org/10.1109/IPFA.2015.7224437>.

(12) Kwon, J.; Delker, C. J.; Thomas Harris, C.; Das, S. R.; Janes, D. B. Experimental and Modeling Study of 1/f Noise in Multilayer MoS<sub>2</sub> and MoSe<sub>2</sub> Field-Effect Transistors. *J. Appl. Phys.* **2020**, *128* (094501). <https://doi.org/10.1063/5.0014759>.

(13) Das, S. R.; Kwon, J.; Prakash, A.; Delker, C. J.; Das, S.; Janes, D. B. Low-Frequency Noise in MoSe<sub>2</sub> Field Effect Transistors. *Appl. Phys. Lett.* **2015**, *106* (083507). <https://doi.org/10.1063/1.4913714>.

(14) Mitra, R.; Jariwala, B.; Bhattacharya, A.; Das, A. Probing In-Plane Anisotropy in Few-Layer ReS<sub>2</sub> Using Low Frequency Noise Measurement. *Nanotechnology* **2018**, *29* (145706). <https://doi.org/10.1088/1361-6528/aaac03>.

(15) Li, X.; Du, Y.; Si, M.; Yang, L.; Li, S.; Li, T.; Xiong, X.; Ye, P.; Wu, Y. Mechanisms of Current Fluctuation in Ambipolar Black Phosphorus Field-Effect Transistors. *Nanoscale* **2016**, *8* (6), 3572–3578. <https://doi.org/10.1039/c5nr06647f>.

(16) Na, J.; Lee, Y. T.; Lim, J. A.; Hwang, D. K.; Kim, G.; Choi, W. K.; Song, Y.; Control, I.; Convergence, F.; Korea, S.; Engineering, E.; Korea, S. Few-Layer Black Phosphorus Field-Effect Transistors with Reduced Current Fluctuation. *ACS Nano* **2014**, No. 11, 11753–11762. [https://doi.org/https://doi.org/10.1021/nn5052376](https://doi.org/10.1021/nn5052376).

(17) Zhao, C.; Tan, C.; Lien, D. H.; Song, X.; Amani, M.; Hettick, M.; Nyein, H. Y. Y.; Yuan, Z.; Li, L.; Scott, M. C.; Javey, A. Evaporated Tellurium Thin Films for P-Type Field-Effect Transistors and Circuits. *Nat. Nanotechnol.* **2020**, *15* (1), 53–58. <https://doi.org/10.1038/s41565-019-0585-9>.

(18) Zhao, C.; Batiz, H.; Yasar, B.; Kim, H.; Ji, W.; Scott, M. C.; Chrzan, D. C.; Javey, A. Tellurium Single-Crystal Arrays by Low-Temperature Evaporation and Crystallization. *Advanced Materials*. 2021. <https://doi.org/10.1002/adma.202100860>.

(19) Kim, T.; Choi, C. H.; Byeon, P.; Lee, M.; Song, A.; Chung, K. B.; Han, S.; Chung, S. Y.; Park, K. S.; Jeong, J. K. Growth of High-Quality Semiconducting Tellurium Films for High-Performance p-Channel Field-Effect Transistors with Wafer-Scale Uniformity. *npj 2D Mater. Appl.* **2022**, *6* (1), 1–7. <https://doi.org/10.1038/s41699-021-00280-7>.

(20) Kim, C.; Hur, N.; Yang, J.; Oh, S.; Yeo, J.; Jeong, H. Y.; Shong, B.; Suh, J. Atomic Layer Deposition Route to Scalable, Electronic-Grade van Der Waals Te Thin Films. *ACS Nano* **2023**, *17* (16), 15776–15786. <https://doi.org/10.1021/acs.nano.3c03559>.

(21) Meng, Y.; Li, X.; Kang, X.; Li, W.; Wang, W.; Lai, Z.; Wang, W.; Quan, Q.; Bu, X.; Yip, S. P.; Xie, P.; Chen, D.; Li, D.; Wang, F.; Yeung, C. F.; Lan, C.; Liu, C.; Shen, L.; Lu, Y.; Chen, F.; Wong, C. Y.; Ho, J. C. Van Der Waals Nanomesh Electronics on Arbitrary Surfaces. *Nat. Commun.* **2023**, *14* (1), 1–14. <https://doi.org/10.1038/s41467-023-38090-8>.

(22) Peng, M.; Xie, R.; Wang, Z.; Wang, P.; Wang, F.; Ge, H.; Wang, Y.; Zhong, F.; Wu, P.; Ye, J.; Li, Q.; Zhang, L.; Ge, X.; Ye, Y.; Lei, Y.; Jiang, W.; Hu, Z.; Wu, F.; Zhou, X.; Miao, J.; Wang, J.; Yan, H.; Shan, C.; Dai, J.; Chen, C.; Chen, X.; Lu, W.; Hu, W. Blackbody-Sensitive Room-Temperature Infrared Photodetectors Based on Low-Dimensional Tellurium Grown by Chemical Vapor Deposition. *Sci. Adv.* **2021**, *7* (16). <https://doi.org/10.1126/sciadv.abf7358>.

(23) Shen, C.; Liu, Y.; Wu, J.; Xu, C.; Cui, D.; Li, Z.; Liu, Q.; Li, Y.; Wang, Y.; Cao, X.; Kumazoe, H.; Shimojo, F.; Krishnamoorthy, A.; Kalia, R. K.; Nakano, A.; Vashishta, P. D.; Amer, M. R.; Abbas, A. N.; Wang, H.; Wu, W.; Zhou, C. Tellurene Photodetector with High Gain and Wide Bandwidth. *ACS Nano* **2020**, *14* (1), 303–310. <https://doi.org/10.1021/acs.nano.9b04507>.

(24) Ren, X.; Wang, Y.; Xie, Z.; Xue, F.; Leighton, C.; Frisbie, C. D. Gate-Tuned Insulator-Metal Transition in Electrolyte-Gated Transistors Based on Tellurene. *Nano Lett.* **2019**, *19* (7), 4738–4744. <https://doi.org/10.1021/acs.nanolett.9b01827>.

(25) Yan, Y.; Xia, K.; Gan, W.; Yang, K.; Li, G.; Tang, X.; Li, L.; Zhang, C.; Fei, G. T.; Li, H. A Tellurium Short-Wave Infrared Photodetector with Fast Response and High Specific Detectivity. *Nanoscale* **2022**, *14*, 13187–13191. <https://doi.org/10.1039/d2nr02822k>.

