

SUPPORTING INFORMATION

Anchored Epitaxial Growth of Single-Orientation One-dimensional Organic Nanowires towards their Integration into Field-effect Transistor and Polarization-sensitive Photodetector Arrays

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Experimental section

Preparation of M-sapphire substrates: The flat M-face sapphire wafers (thickness: $430 \pm 15 \mu\text{m}$, Crystal Silicon E&T Co., Suzhou) were first cut into $1 \times 1 \text{ cm}^2$ pieces and then rinsed sequentially with acetone, ethanol and deionized water for 15 minutes. The annealing process is carried out using a three-zone split quartz tube furnace (OTF-1500X-III, Hefei Kejing Material Technology Co., Ltd) heated to a temperature of $1400 \text{ }^\circ\text{C}$ for 16 hours in ambient air. This high temperature annealing process is crucial for the formation of channel array patterns on the M-plane sapphire substrate. The formation of these patterns is related to the thermal stability of specific crystal facets. During the annealing process, the atoms in the M-plane sapphire substrate undergo thermal migration and rearrangement, allowing the crystal facets to align and form distinct channels. After annealing, the substrates are cleaned again by ultrasonic cleaning with acetone, ethanol, and deionized water for 15 minutes. Finally, lyophilic modification was performed by ozone treatment for 15 minutes.

Fabrication of 1D C8-BTBT, DPA, diF-TES-ADT and C10-DNTT nanowires: 1D C8-BTBT nanowires were grown in a two-zone split quartz tube furnace (OTF-1200X, Hefei Kejing Material Technology Co., Ltd). In all, C8-BTBT powder (purity $\geq 99\%$, LT-S9054, Luminescence Technology Corp.) was placed as source material into a crucible in quartz tubes (inner diameter: 20 mm). Then, the annealed M-plane sapphire substrate was placed at a distance of 2 cm from the source C8-BTBT powder. Ar/H₂ mixture (95% Ar, 5% H₂) was used as the carrier gas and the flow rate was set at 120 sccm. The temperature rises to $120 \text{ }^\circ\text{C}$ at a rate of $4 \text{ }^\circ\text{C}/\text{min}$ and remains for 120 minutes. Optimal conditions for the growth of 1D C8-BTBT nanowires on M-plane sapphire substrates were determined by controlling temperature, position, time, and gas flow rate. The method for DPA, diF-TES-ADT and C10-DNTT nanowires growth was similar to C8-BTBT with minor modifications, source zone temperatures were referenced from literatures¹⁻³, and the fundamental properties of these materials are shown in Table S1. For the growth of 1D DPA nanowires, the distance between DPA powder (purity $\geq 98\%$, D5152, Tokyo Chemical Industry Co., Ltd.) and sapphire substrate was 9 cm, the

temperature was maintained at 160 °C for 60 minutes, and the gas flow rate was 30 sccm. For the growth of 1D diF-TES-ADT nanowires, the distance between diF-TES-ADT powder (purity \geq 99%, LT-S9027, Luminescence Technology Corp.) and sapphire substrate was 8 cm, the temperature was maintained at 160 °C for 90 minutes, and the gas flow rate was 30 sccm. For the growth of 1D C10-DNTT nanowires, the distance between C10-DNTT powder (purity \geq 99%, CS90014, Luminescence Technology Corp.) and sapphire substrate was 6 cm, the temperature was maintained at 220 °C for 120 minutes, and the gas flow rate was 120 sccm.

Transfer of 1D organic nanowires: For the 1D organic nanowire transfer from the M-plane sapphire substrate to the SiO₂ wafers, using the polyvinyl alcohol (PVA) film peeling method. PVA (5% wt, MW \sim 31000, Aladdin) was spin-coated on the nanowire-grown sapphires and placed on a heating plate at 50 °C for 30 minutes. After the PVA was cured, peeled the film off slowly and tightly attached it to the cleaned SiO₂ wafer. Then, soaked in deionized water for 1 minutes, picked up and rinsed the residual PVA with deionized water, and finally dried using nitrogen.

Characterizations of 1D C8-BTBT nanowires: 1D C8-BTBT nanowires morphology was imaged using Leica DM4P cross-polarized optical microscopy. SEM images were obtained by a Hitachi SU5000 scanning electron microscope. Transmission electron microscope (TEM, FEI Tecnai G2 F20) was operated at a voltage of 200 kV. Grazing incidence X-ray diffraction (GIXRD) were performed on a Bruker D8 DISCOVER X-ray diffractometer. Atomic force microscope (AFM) images and high-resolution AFM (HRAFM) images were obtained using Cypher ES system with UHF AFM tips from Asylum Cypher. The polarized ultraviolet–visible (UV) absorption spectra were obtained using a LAMBDA 950 double-beam spectrophotometer.

Fabrication of flexible OFETs and photodetectors: Flexible 1D C8-BTBT nanowires-based OFETs were fabricated through the following steps. First, parylene layer (parylene-C J&K Scientific) was deposited by chemical vapor deposition (Diener P6) on a glass substrate. A 40 nm thick striped Au layer was deposited as the gate electrode

on the parylene substrate by metal mask. Then, PVP was spin-coated on the gate electrode to serve as the dielectric. The capacitance of the dielectric layer was measured to be 7.5 nF cm^{-2} (Figure S9, Supporting Information). Subsequently, 1D C8-BTBT nanowires were transfer to the substrate by the PVA film. Next, patterned Ag and F4-TCNQ films were formed by thermal evaporation. Finally, the devices could be peeled off from the glass substrate, obtaining flexible OFETs. Photodetectors were fabricated by evaporating Ag electrodes directly on nanowire-grown sapphire substrates. The electrical properties of the flexible OFETs and photodetectors were measured at room temperature in the air using a semiconductor parameter analyzer (Keithley 4200-SCS). Using a 365 nm UV lamp as light source, the light intensity and polarization were changed by stacking filter paper and polarizing lens.

Supplementary Figures

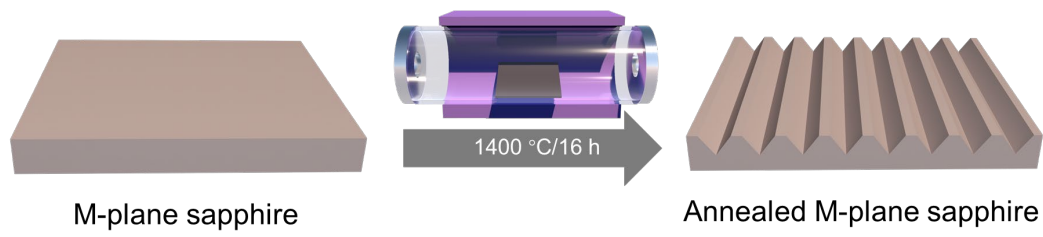


Figure S1 Schematic illustration of the M-plane sapphire substrate preparation process.

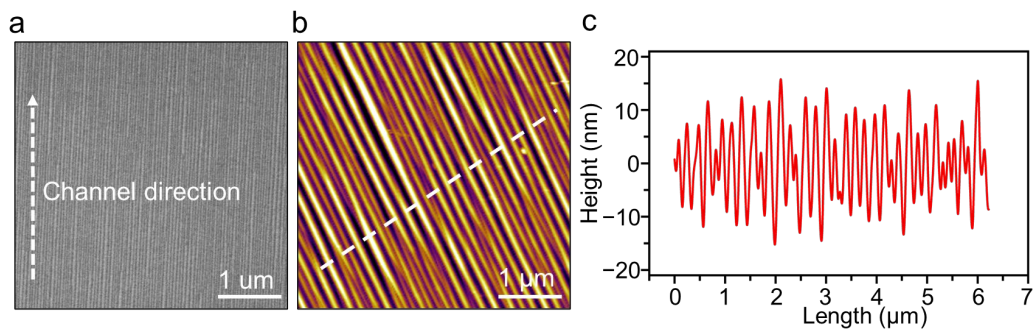


Figure S2 (a) SEM image of the annealed M-plane sapphire substrate. (b) AFM image of the annealed M-plane sapphire substrate surface and (c) the corresponding height profile.

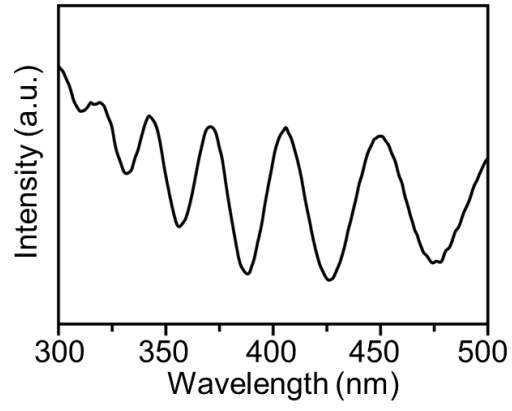


Figure S3 UV-vis absorption spectra of the annealed M-plane sapphire.

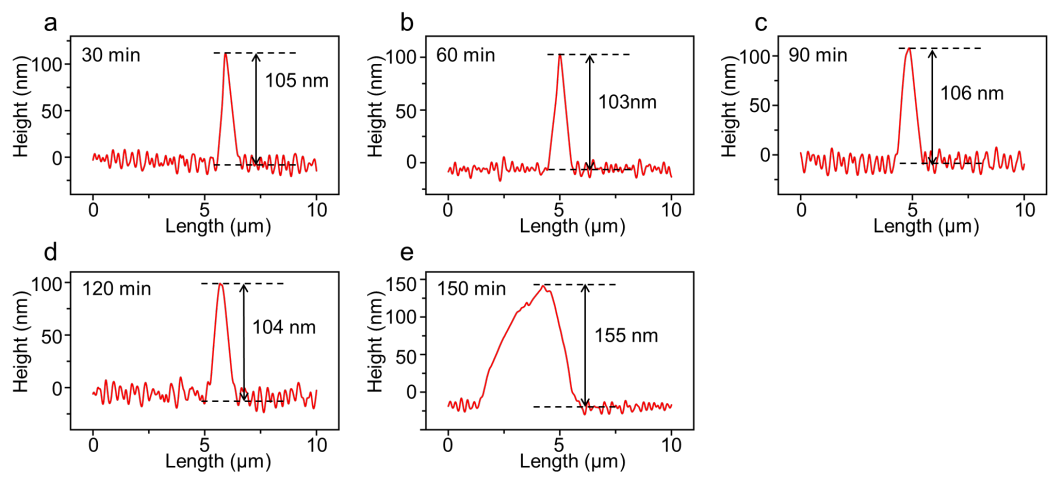


Figure S4 Height profiles of the obtained 1D C8-BTBT nanowires at different growth time: (a) 30 min, (b) 60 min, (c) 90 min, (d) 120 min, (e) 150 min.

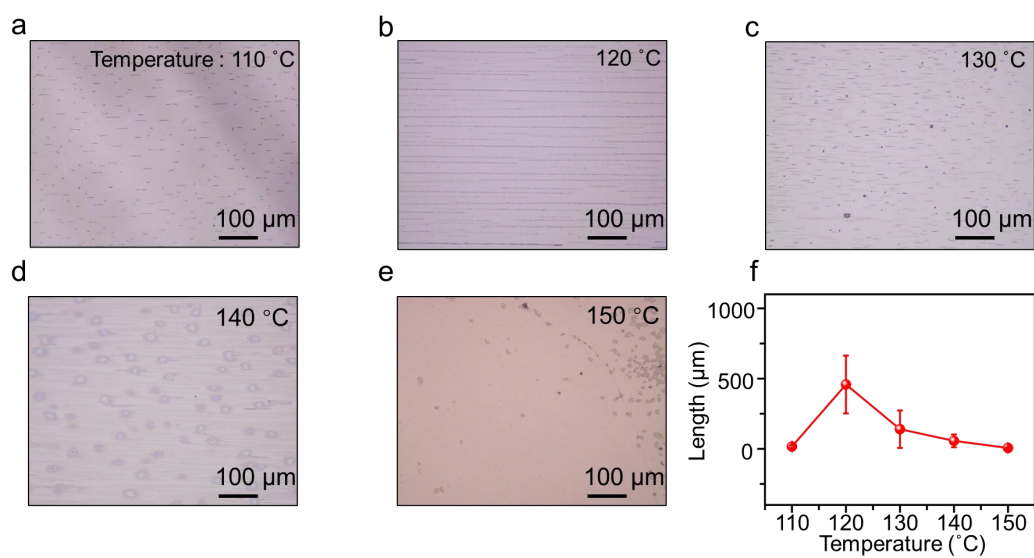


Figure S5 (a-e) OM images of the obtained 1D C8-BTBT nanowires at different growth temperatures: (a) 110 °C, (b) 120 °C, (c) 130 °C, (d) 140 °C, (e) 150 °C. (f) Statistical diagram of the length of 1D C8-BTBT nanowires related to the growth temperature.

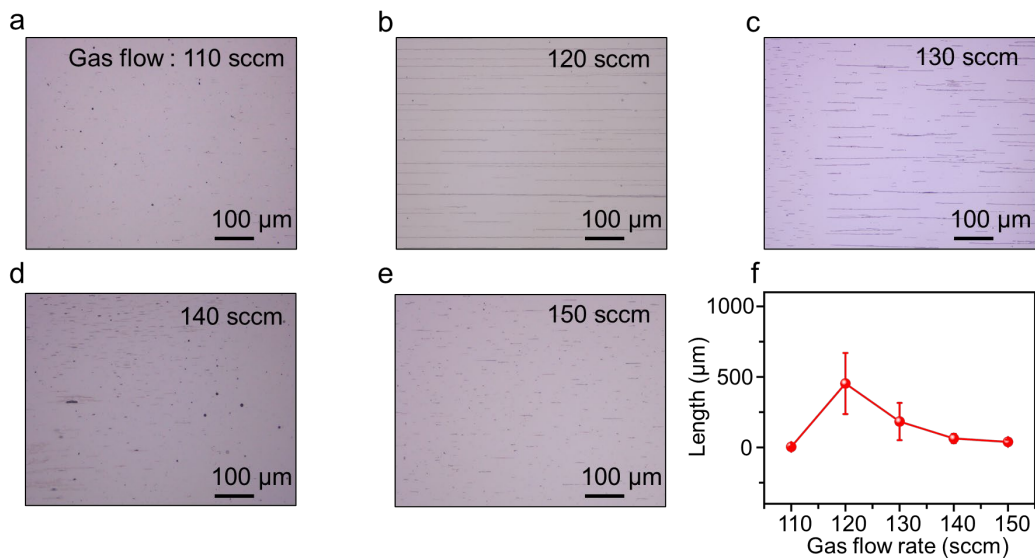


Figure S6 (a-e) OM images of 1D C8-BTBT nanowires grown at different gas flow rate: (a) 110 sccm, (b) 120 sccm, (c) 130 sccm, (d) 140 sccm, (e) 150 sccm. (f) Statistical diagram of the length of 1D C8-BTBT nanowires related to the gas flow rate.

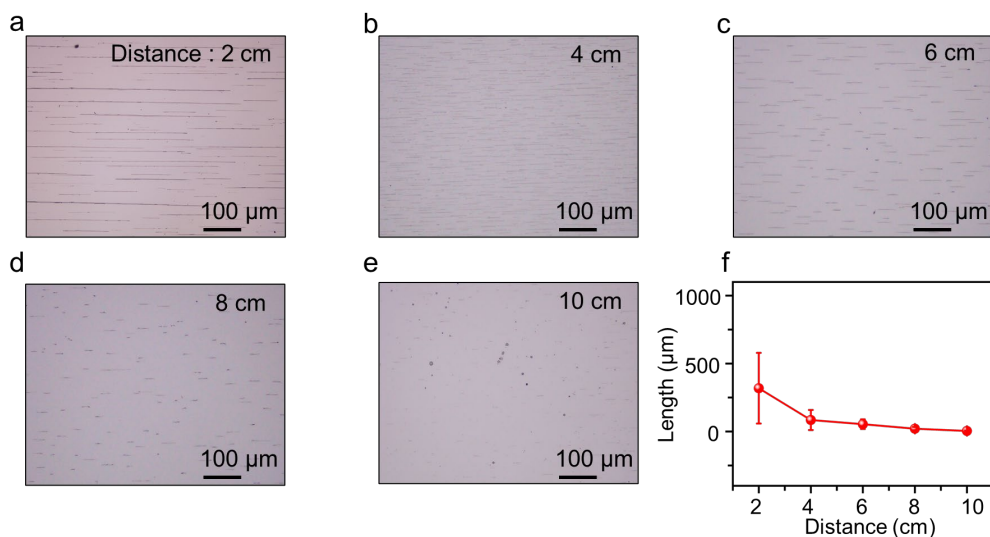


Figure S7 (a-e) OM images of 1D C8-BTBT nanowires grown at different distance: (a) 2 cm, (b) 4 cm, (c) 6 cm, (d) 8 cm, (e) 10 cm. (f) Statistical diagram of the length of 1D C8-BTBT nanowires related to the distance.

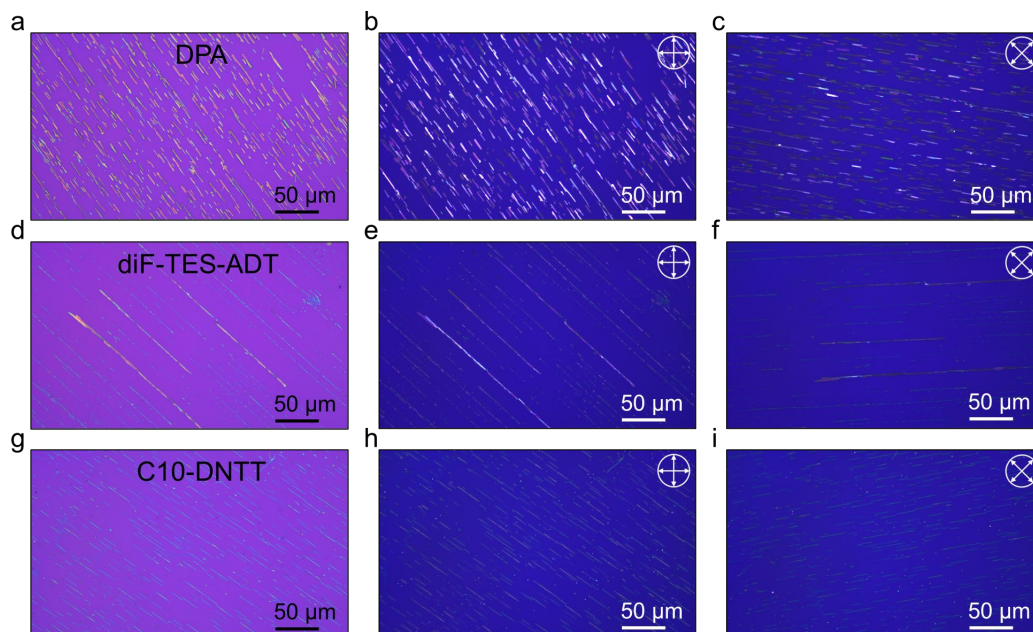


Figure S8 (a, d, g) OM image of the 1D DPA, diF-TES-ADT and C10-DNTT nanowires after being transferred to SiO₂ substrate. (b, c) POM images of the 1D DPA nanowires on SiO₂ substrate. (e, f) POM images of the 1D diF-TES-ADT nanowires on SiO₂ substrate. (h, i) POM images of the 1D C10-DNTT nanowires on SiO₂ substrate.

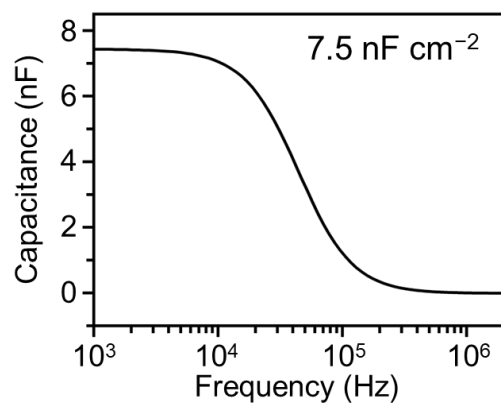


Figure S9 Capacitance of dielectric layer (PVP) in flexible OFET.

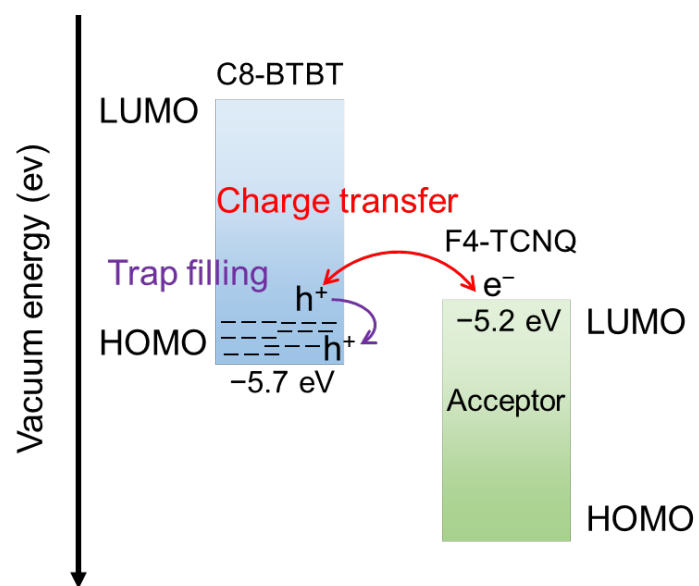


Figure S10 Energy band diagram of the F4-TCNQ surface doped C8-BTBT.

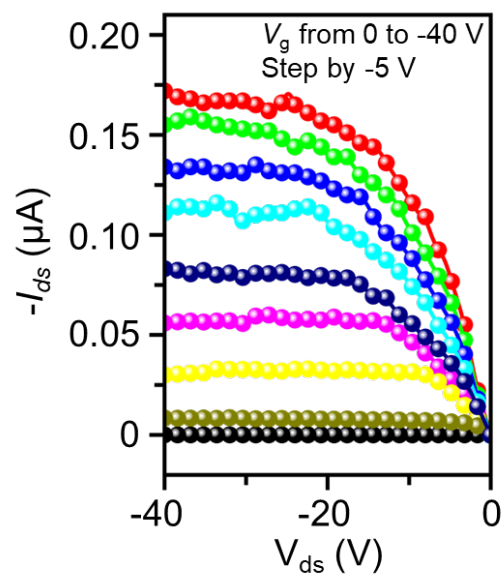


Figure S11 Output curves of a typical 1D C8-BTBT nanowire-based OFET.

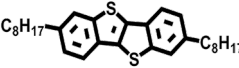
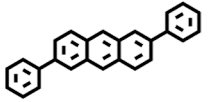
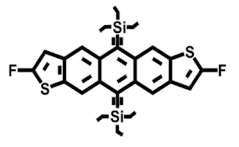
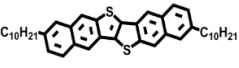
Materials	Structure	Molecular Weight (g/mol)	Band Gap (eV)	Melting point (°C)	Absorption Wavelength (nm)	Mobility (cm ² / V s)	Ref.
C8-BTBT		464.7	~3.3	245-248	300-400	1-30	4,5
DPA		330.4	~3.0	~250	~350	1-30	6,7
diF-TES-ADT		602.9	~2.2	193-198	300-500	1-20	8,9
C10-DNTT		620.9	~2.5	~300	400-800	1-15	10

Table S1 Fundamental properties of the C8-BTBT, DPA, diF-TES-ADT and C10-DNTT.

References:

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- 9 J. Wang et al., Wafer-scale epitaxial growth of two-dimensional organic semiconductor single crystals toward high-performance transistors. *Adv. Mater.*, 2023, 35, 2301017.
- 10 B. Peng et al., A simulation-assisted solution-processing method for a large-area, high-performance C10-DNTT organic semiconductor crystal. *J. Mater. Chem. C*, 2016, 4, 8628.