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Electronic Supplementary Material

Low-Voltage Polymer Monolayer Transistors for High-Gain Unipolar and Complementary Logic Inverters

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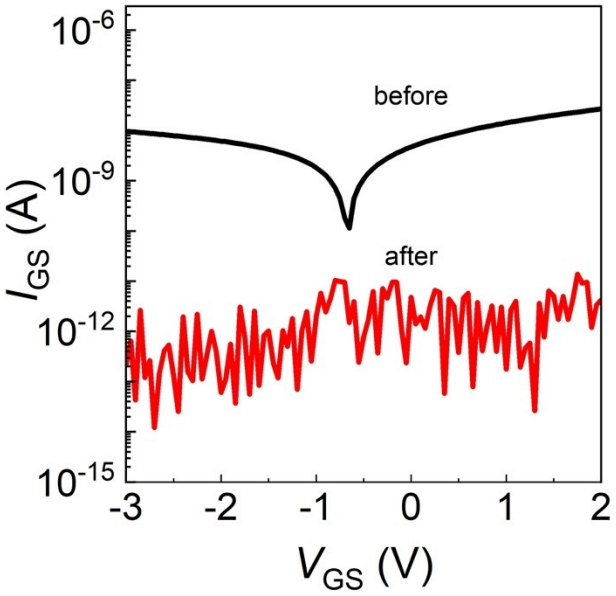

Figure S1 The gate leakage currents (I_{GS}) of polymer monolayer TFTs before and after patterning using the sacrificial layer strategy.

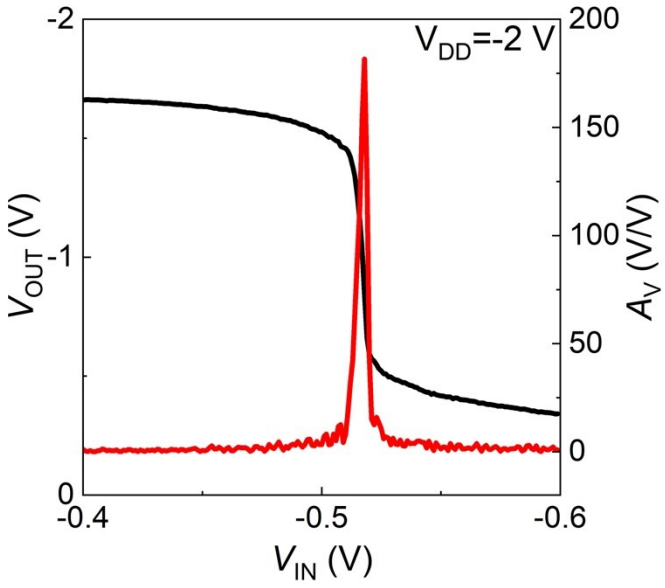

Figure S2 Input-output characteristics and voltage gain of zero-V_{GS}-load inverter based on polymer monolayer TFTs at V_{DD} = -2 V.

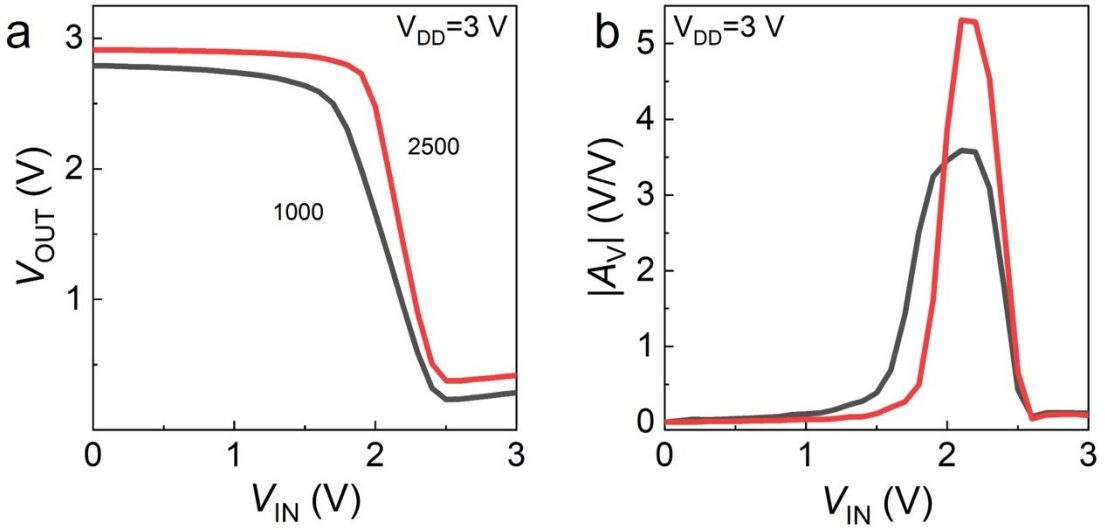

Figure S3 Influence of channel width of driver transistor on the performance of diode-load inverters. The channel width of driver transistor is 1000 and 2500 μm in this figure and 5000 μm in Fig. 4b.

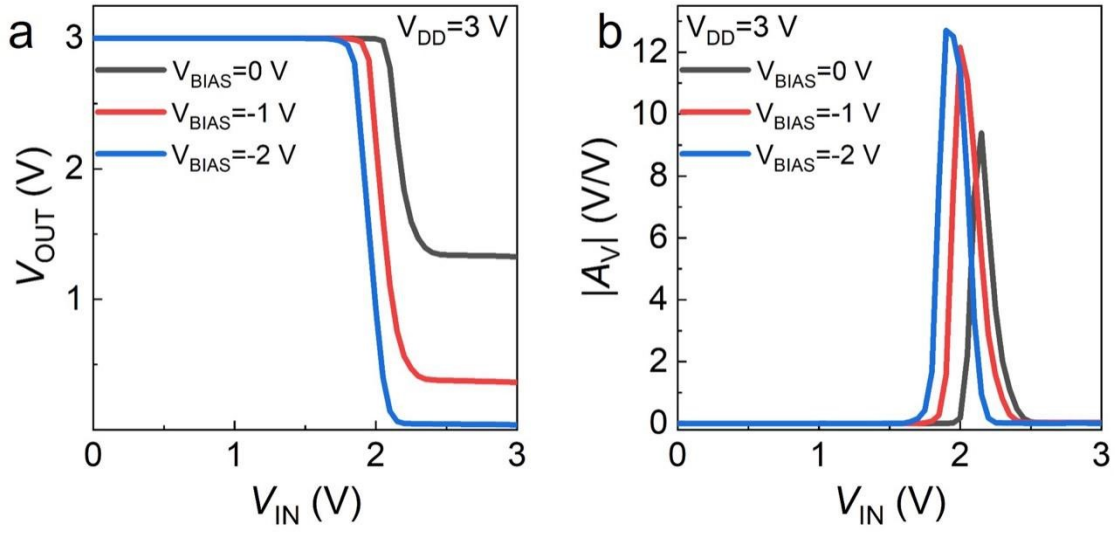

Figure S4 Influence of channel width of bias voltage (V_{BIAS}) on the performance of pseudo-E inverters. The bias voltage is -1 and -2 V in this figure and -3 V in Fig. 4e.

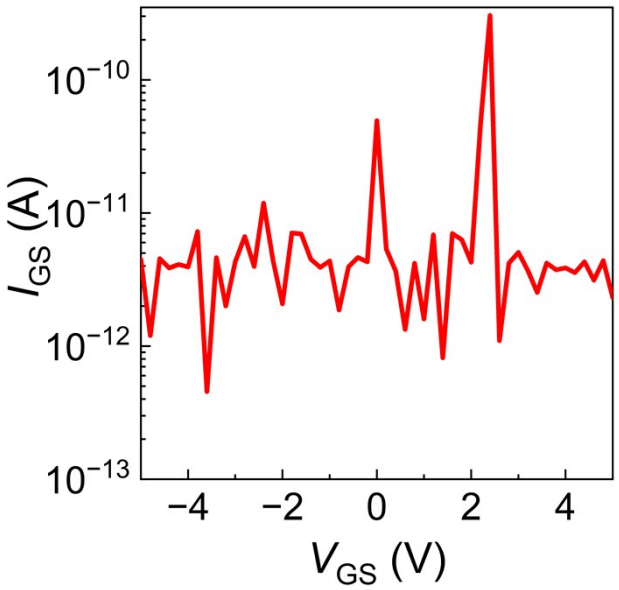

Figure S5 The gate leakage currents (IGS) of IGZO TFTs after patterning

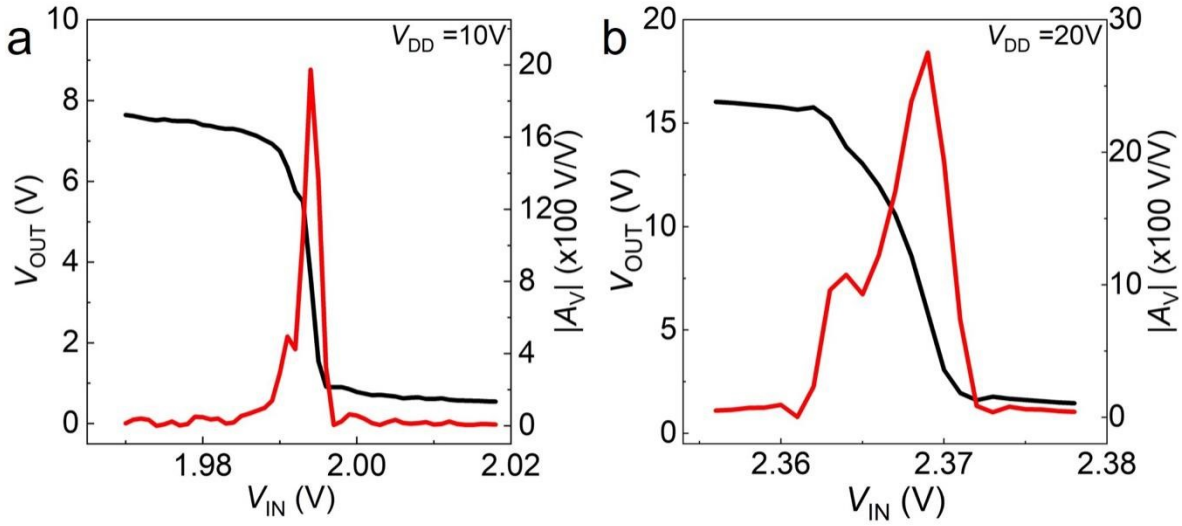

Figure S6 Input-output characteristics of complementary inverter at various V_{DD}.

Table S1 Channel dimension of TFTs reported in this work.

channel dimension		channel length (μm)	channel width (μm)	number of TFTs
polymer monolayer TFT		20	1000	-
IGZO TFT		10	20	-
zero-V_{GS}-load inverter	driver TFT	5	90	2
	load TFT	5	180	
diode-load inverter	driver TFT	5	5000	2
	load TFT	5	20	
Pseudo-E inverter	driver TFT	5	5000	4
	load TFT	5	20	