Supplementary materials

Dual Functionality of NbO_x Memristors for Synaptic and Neuronal Emulations in the Advanced Neuromorphic Systems

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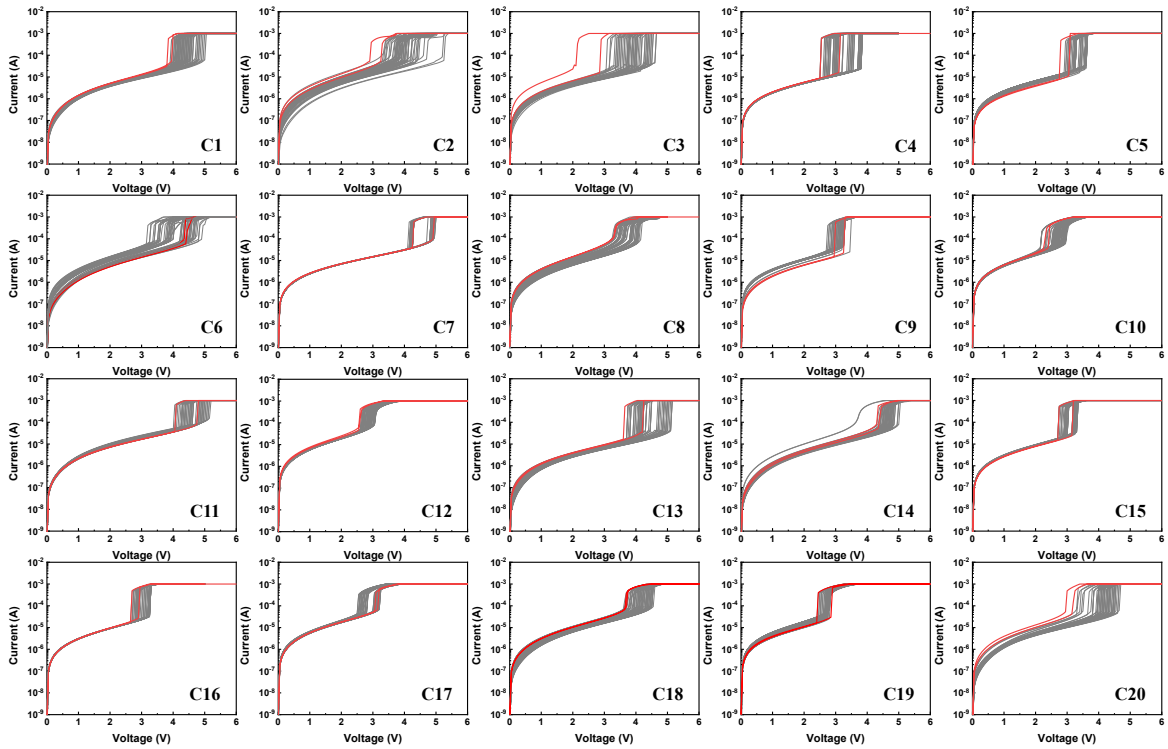


Fig. S1 TS phenomenon in 20 cells over 30 cycles at high CC of W/NbO_x/TiN memristor.

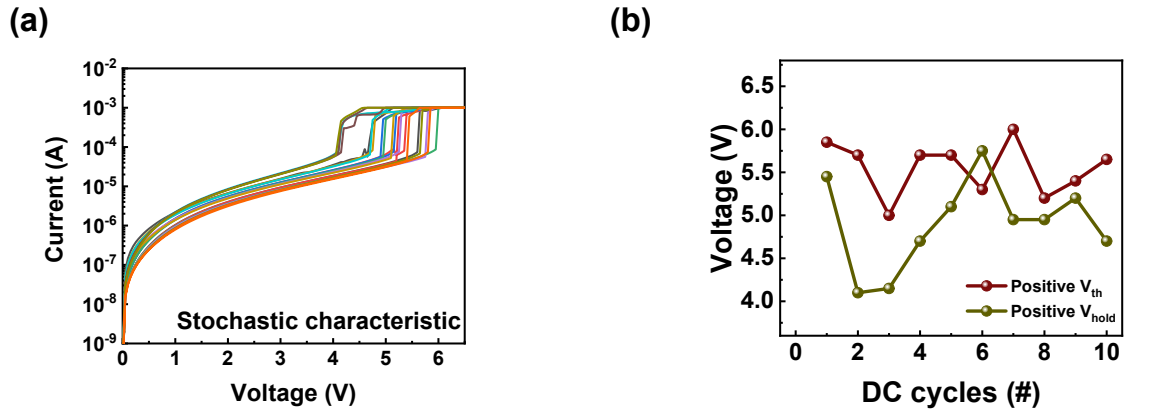
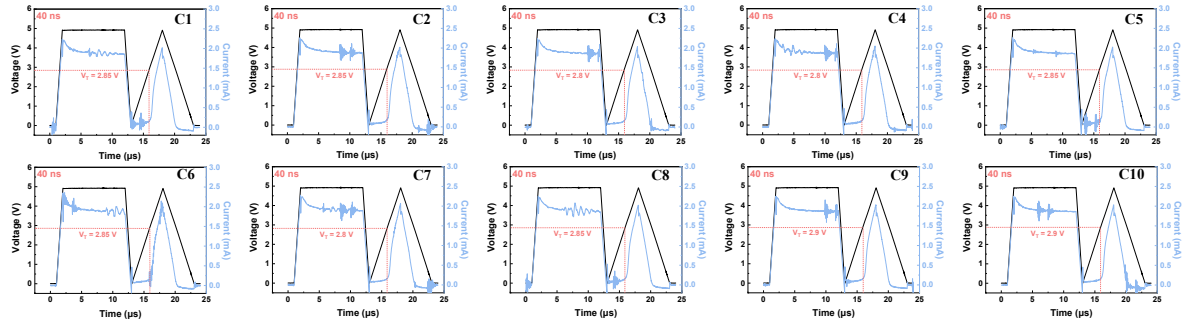
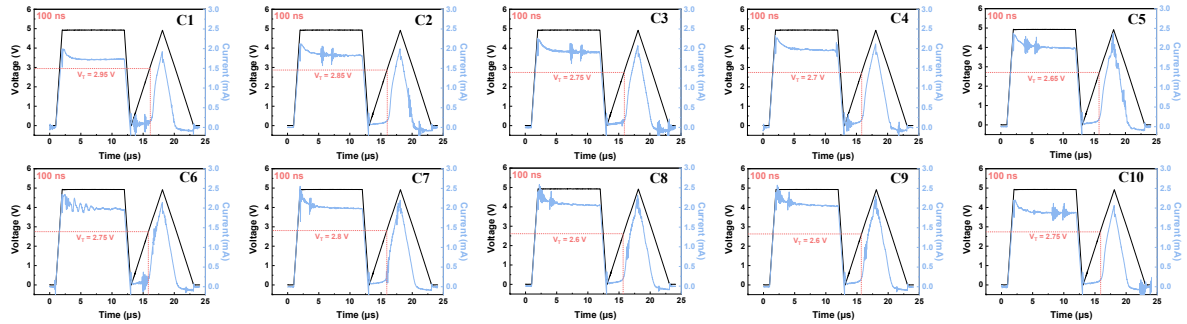


Fig. S2 (a) Randomness in I-V curves of NbO_x memristor cells during TS operation at high compliance current, illustrating the stochastic nature of TS behavior. (b) Cycle-dependent fluctuation of V_{th} and V_{hold} in NbO_x memristor cells during TS operation.

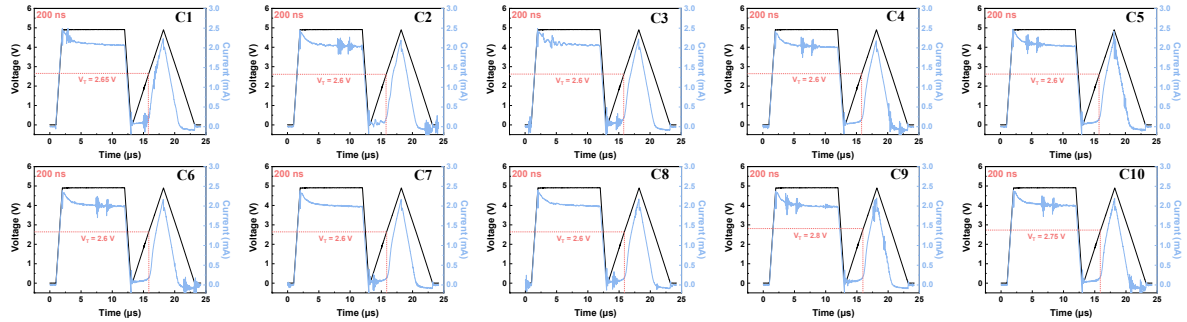
(a) Wait time = 40 ns



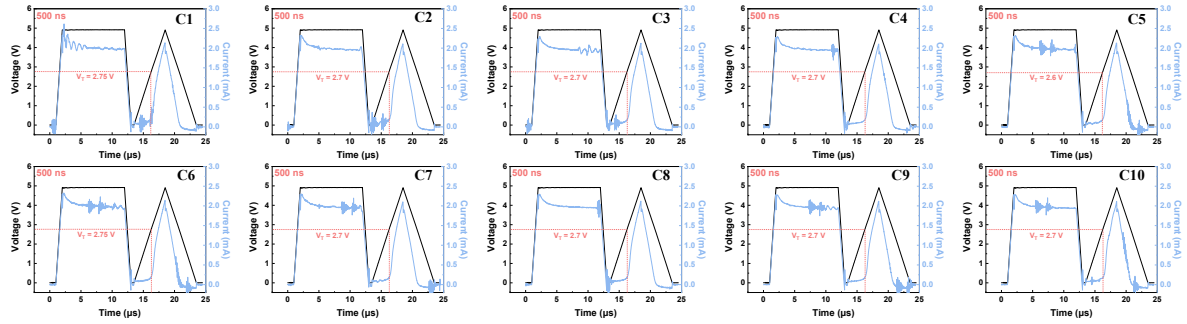
(b) Wait time = 100 ns



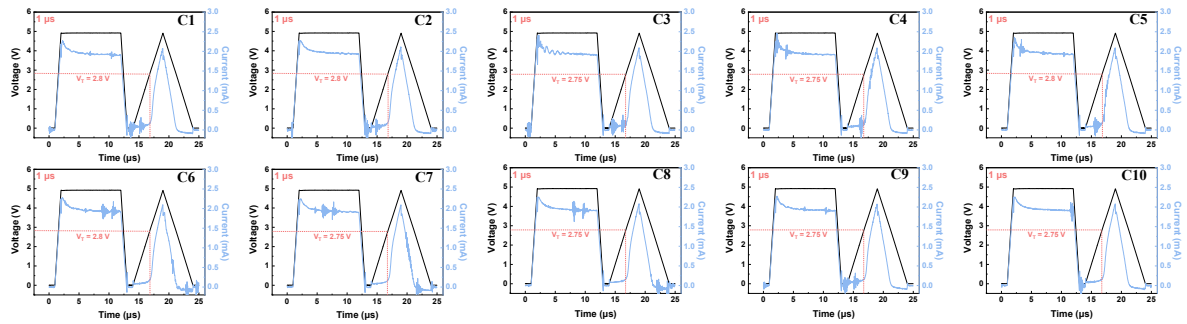
(c) Wait time 200 ns



(d) Wait time 500 ns



(e) Wait time = 1 µs



(f) Wait time = 2 µs

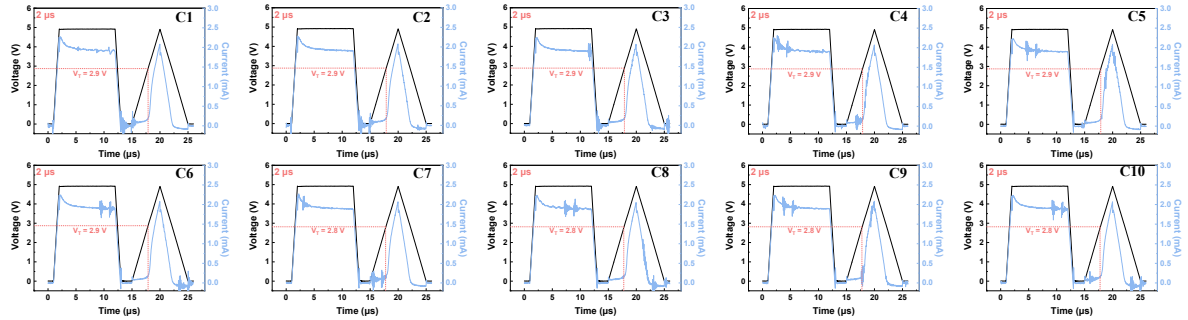
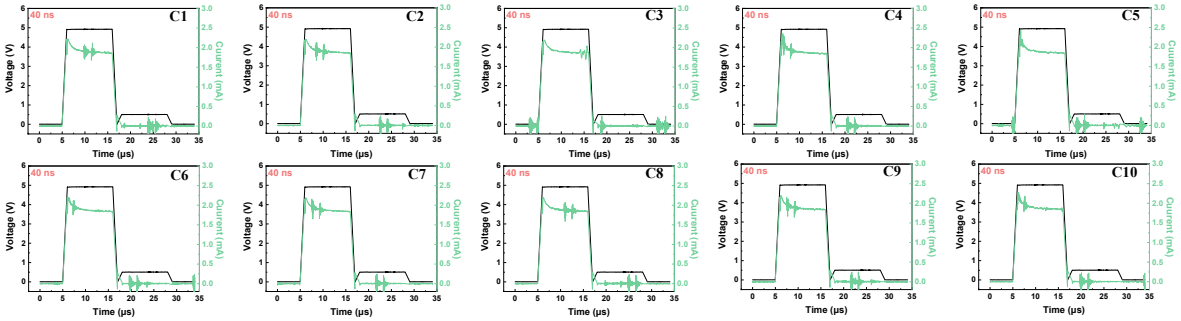
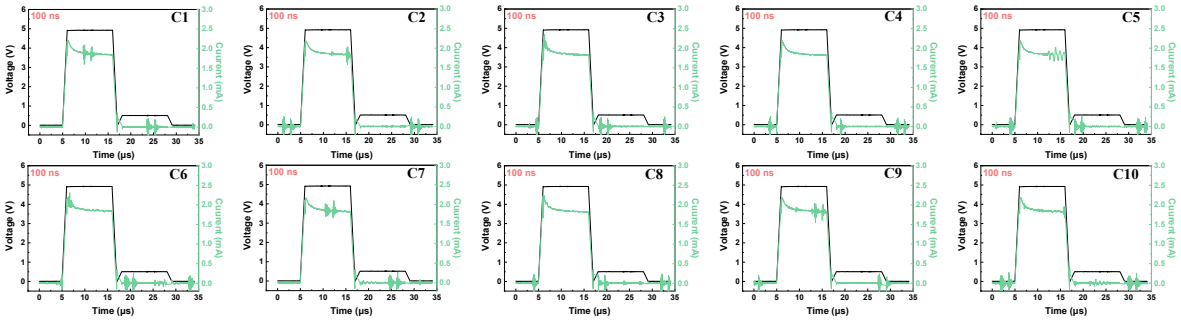


Fig. S3a-S3f Actual wait time data for 10 cells of W/NbO_x/TiN memristor, where the black line represents voltage, and the blue line denotes current.

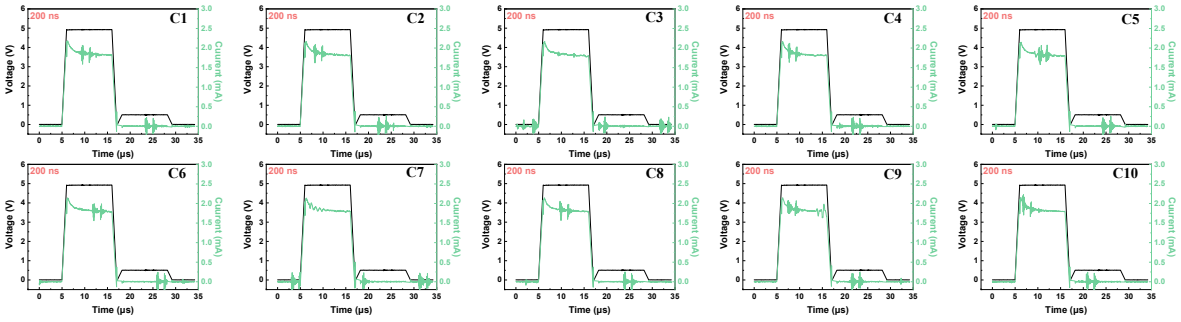
(a) Recovery time = 40 ns



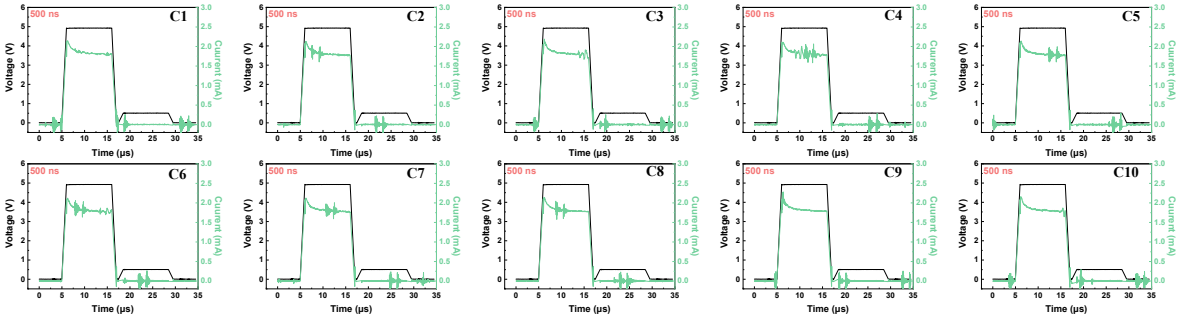
(b) Recovery time = 100 ns



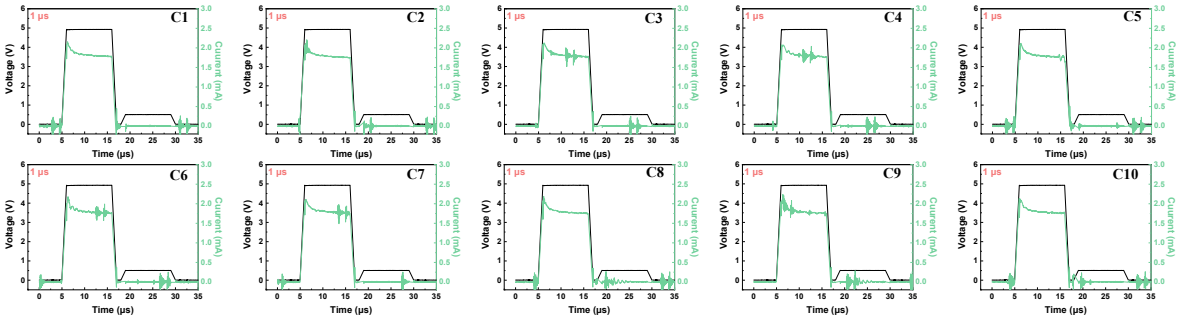
(c) Recovery time = 200 ns



(d) Recovery time = 500 ns



(e) Recovery time = 1 μs



(f) Recovery time = 2 µs

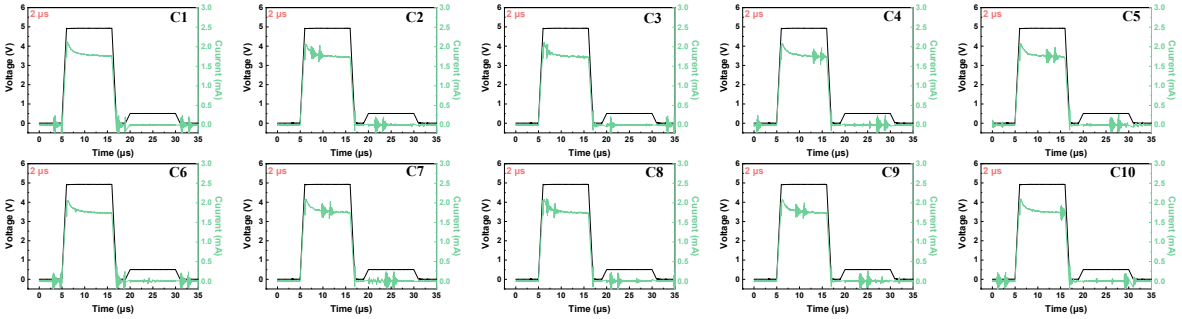


Fig. S4a-S4f Actual recovery time data for 10 cells of W/NbO_x/TiN memristor, where the black line represents voltage, and the green line denotes current.

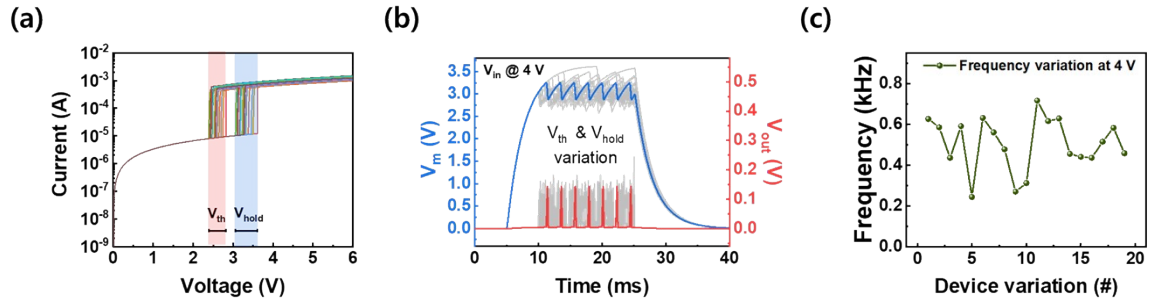


Fig. S5 Illustrating the variations in device I-V characteristic and LIF model. (a) TS I-V characteristics simulated across twenty cycles following the implementation of device variations. The graph highlights the variability in on-resistance, V_{th}, and V_{hold} across different devices. (b) Simulation outputs from the leaky integrate-and-fire (LIF) model at an applied voltage of 4V, utilizing the device variations. (c) Spike frequency analysis illustrating spike frequency in response to device variations at 4 V.

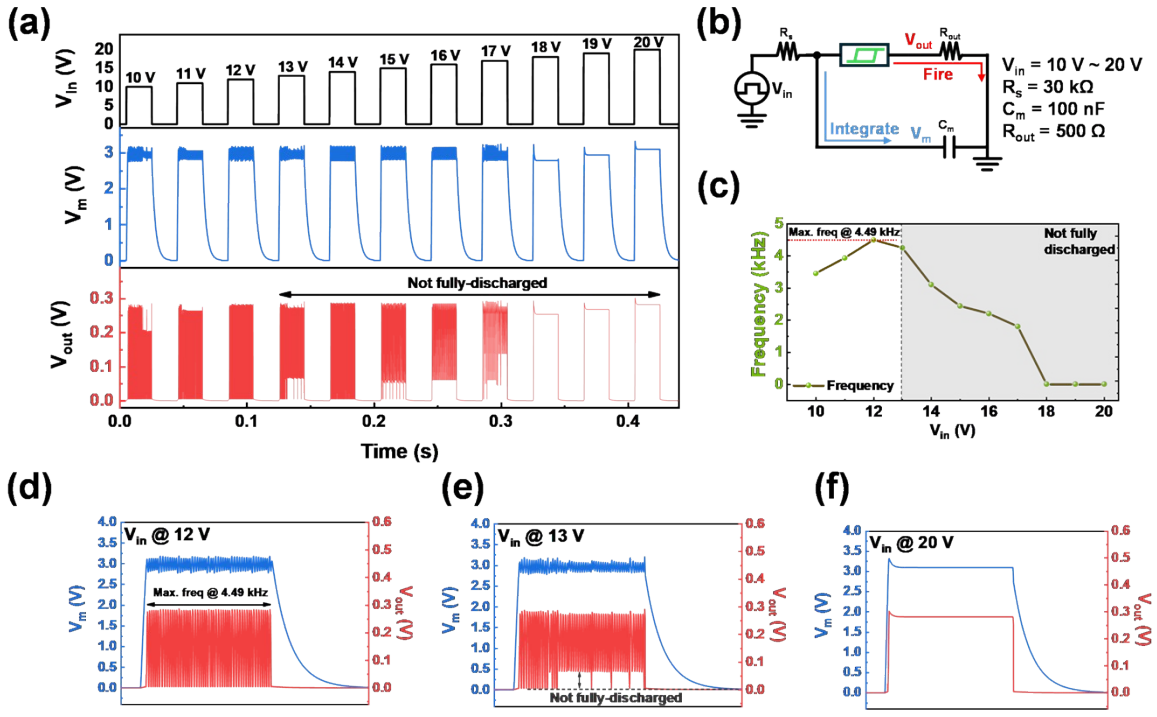


Fig. S6 Illustrating the impact of varying pulse voltages beyond 10 V on spike frequency in the LIF model. (a) Simulation results with a square pulse of 20 ms width, incrementing voltage from 10 V to 20 V in 0.5 V steps, illustrating the relationship between applied voltage, charge accumulation at C_m, and the resulting output spikes. (b) The circuit layout is used to implement the LIF model. (c) The frequency increases from an input pulse of 10 V and the maximum frequency is 4.49 kHz at an input pulse of 12 V. (d) At 12 V, maximum output spikes with a frequency of 4.49 kHz (e) At 13 V, frequency of output spikes decreases since the capacitor is not fully discharged. (f) At 20 V, output spikes are invisible since the capacitor is not discharged at all.

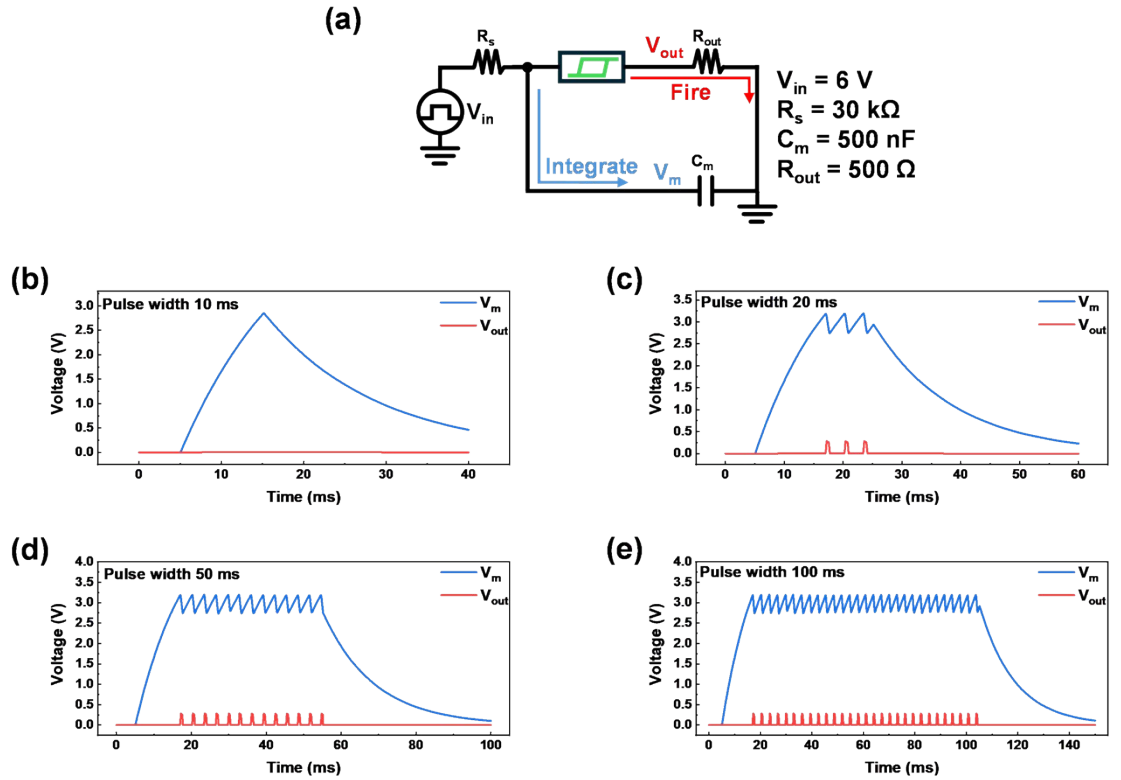


Fig. S7 (a) The circuit layout is used to implement the LIF model with 500 nF of C_m. Simulation data of C_m voltage (V_m), output voltage (V_{out}) with input pulse of 6 V, (b) 10 ms, (c) 20 ms, (d) 50 ms, (e) 100 ms width.

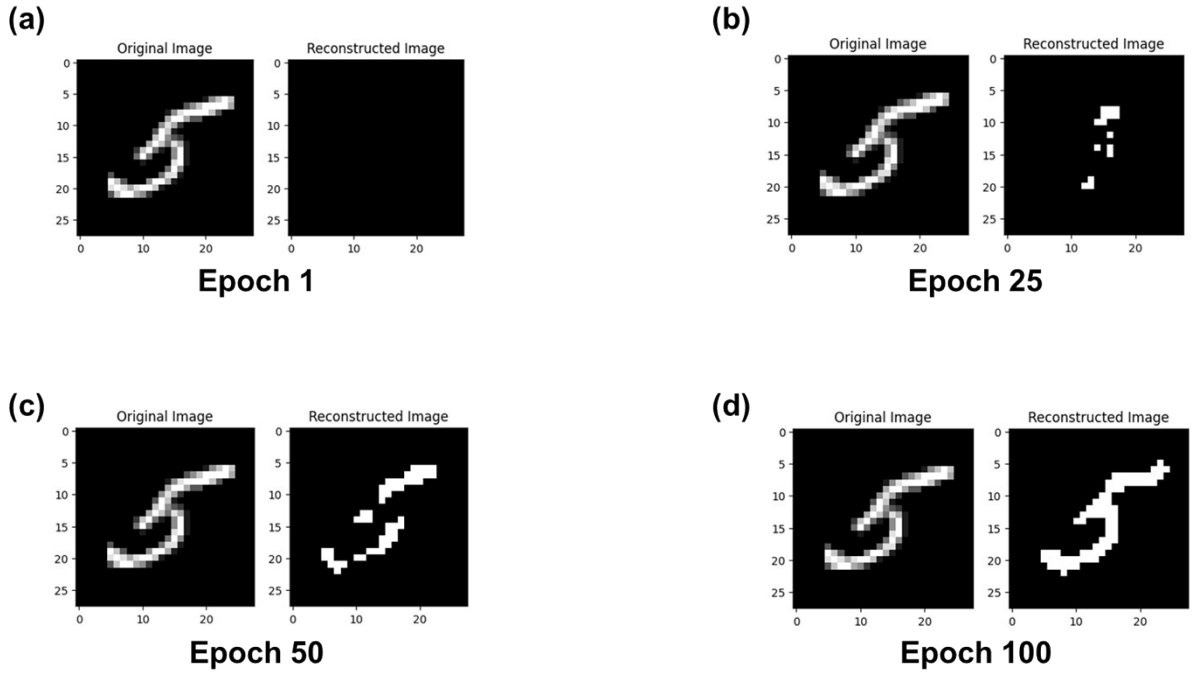


Fig. S8 The progression of image reproduction over (a) epoch 1, (b) epoch 25, (c) epoch 50, (d) epoch 100.

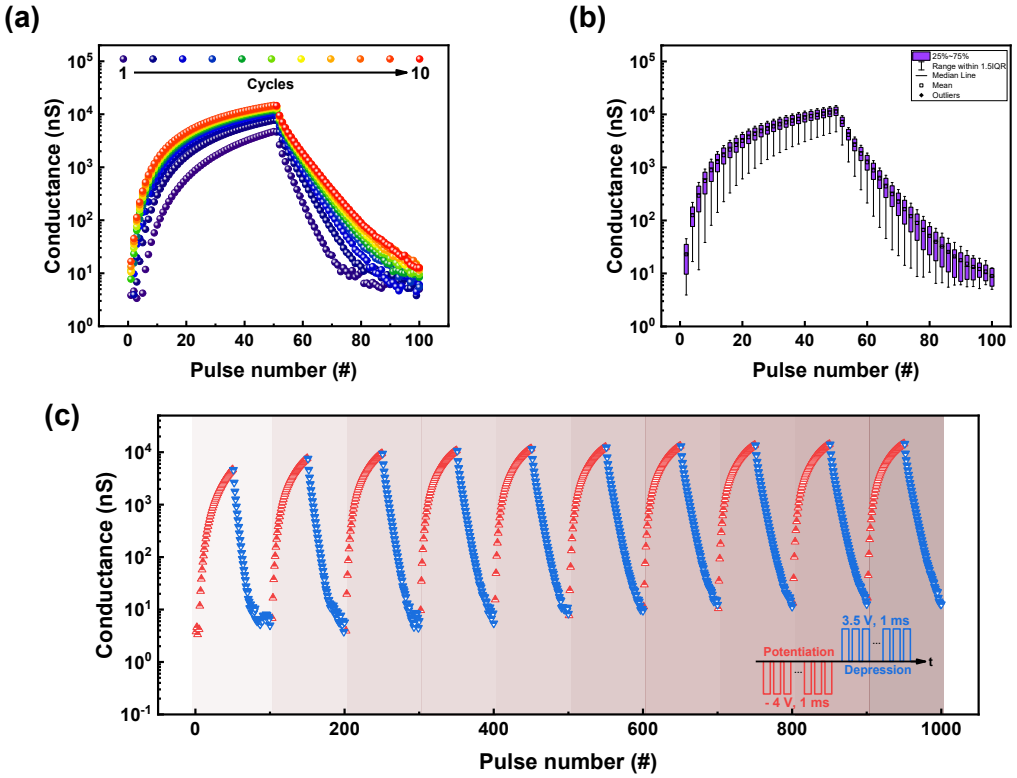


Fig. S9 (a) The conductance across 10 cycles of PD. (b) The conductance of the box plot for the PD 10 cycles. (c) Continuous plot across PD 10 cycles.

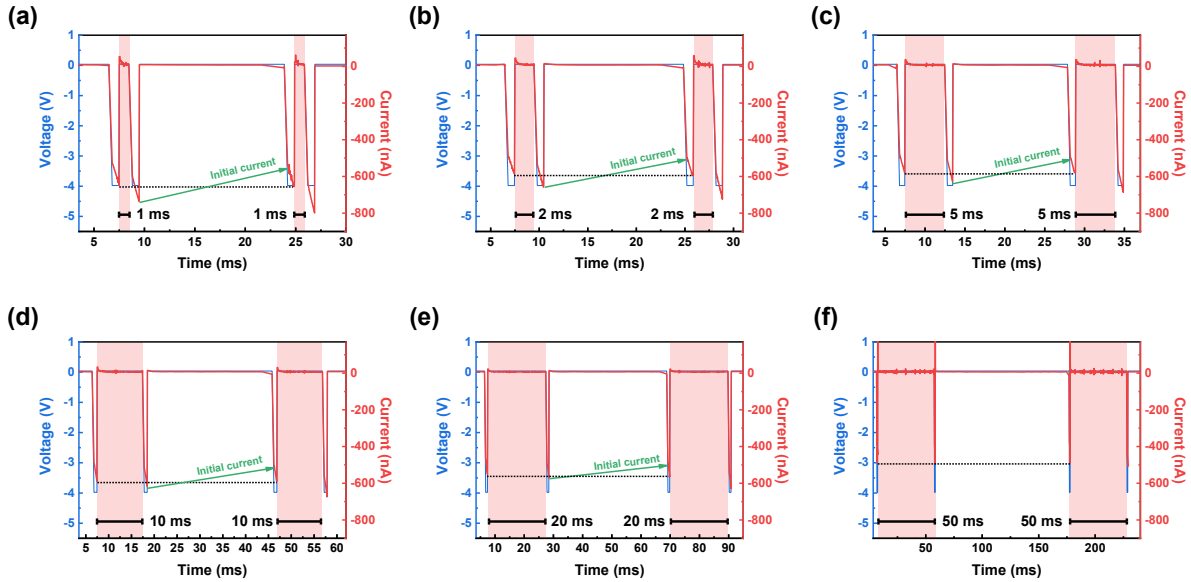


Fig. S10a-S10f Characteristics of paired-pulse facilitation (PPF) through the application of two successive pulses, followed by an identical pulse pair after a delay.

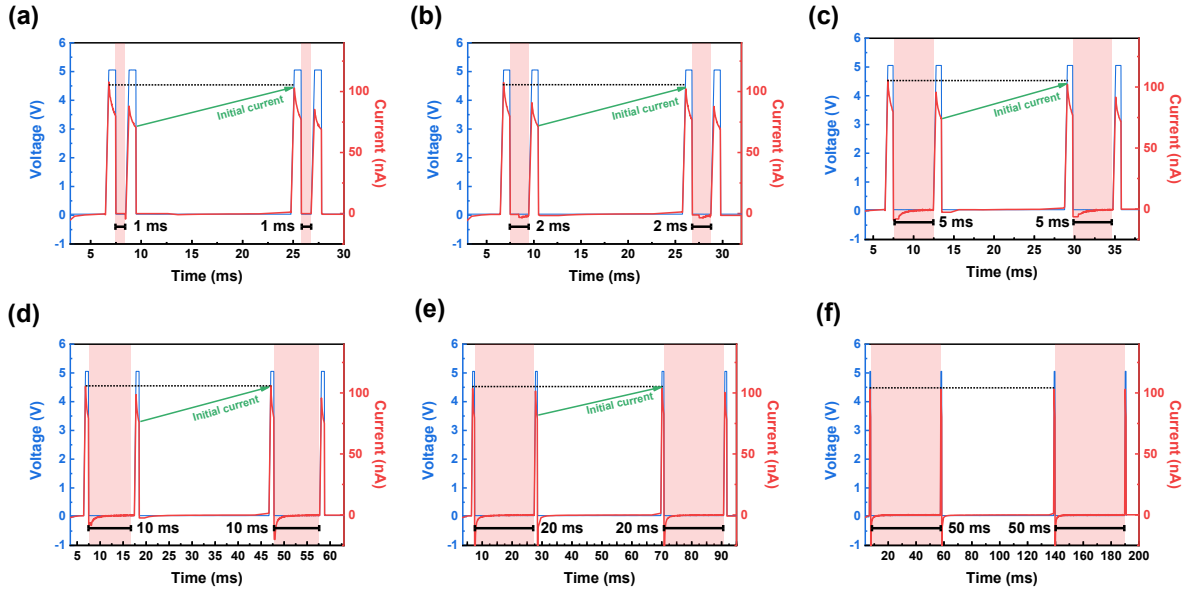


Fig. S11a-S11f Characteristics of paired-pulse depression (PPD) through the application of two successive pulses, followed by an identical pulse pair after a delay.