Supporting Information

Impact of Hydrogen-Controlled Thermal ALD SiO_2 Insulators on IGZO Channel FET to Optimize the Electrical Performance

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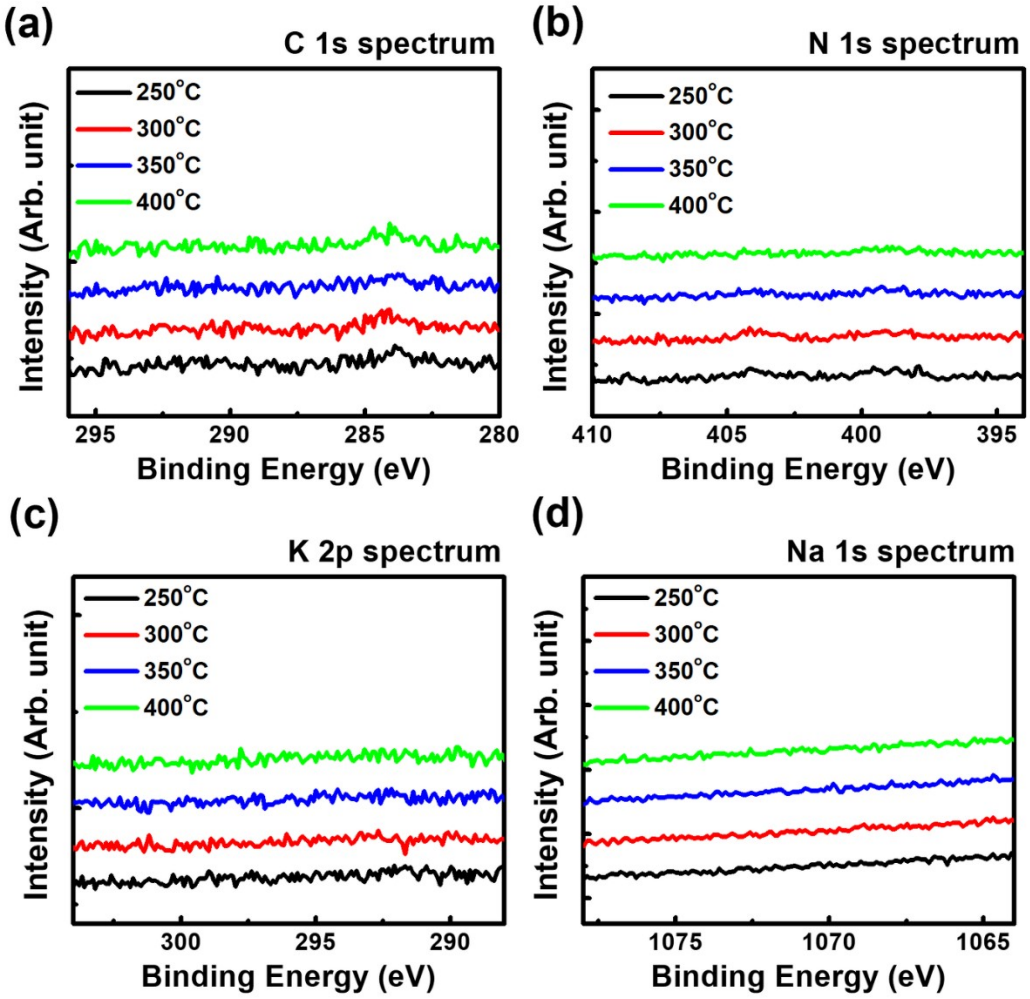


Figure S1. (a) C 1s, (b) N 1s, (c) K 2p, and (d) Na 1s XPS spectra of SiO_2/IGZO stacked films according to the SiO_2 deposition temperature.

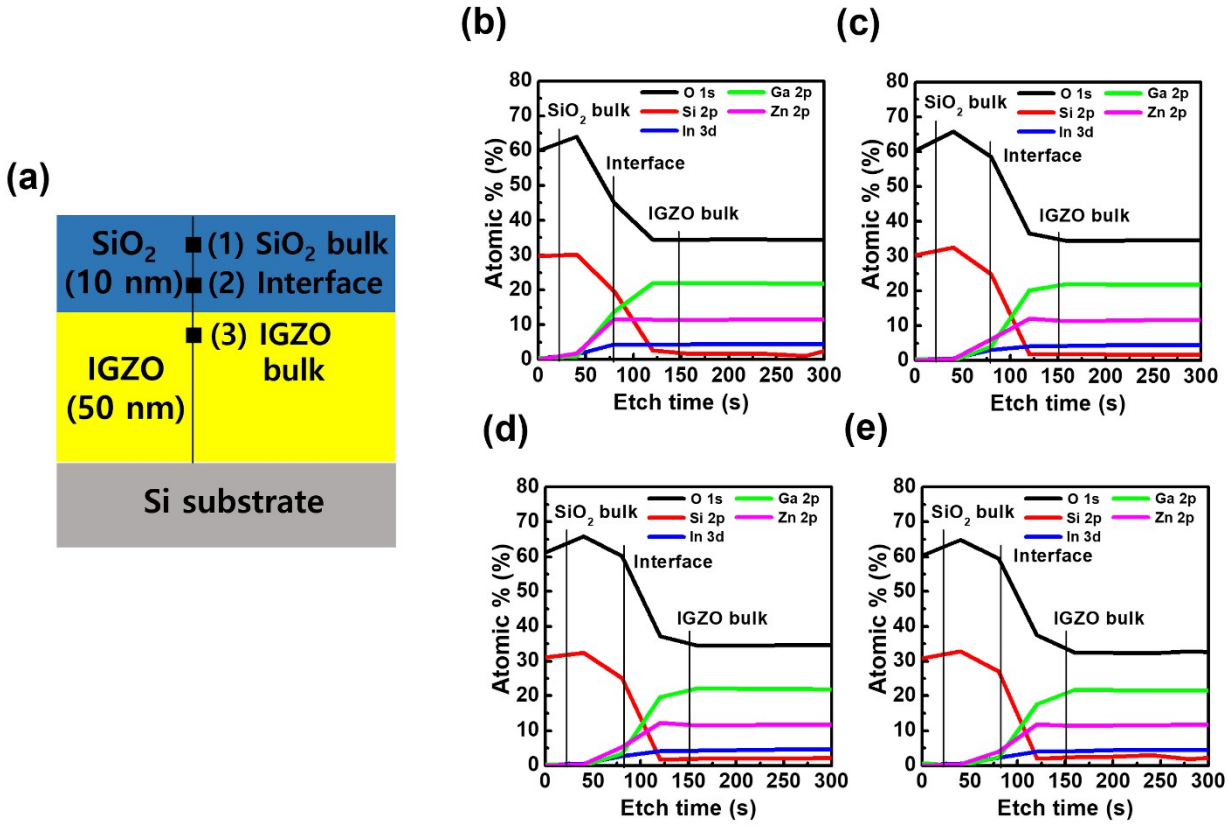


Figure S2. (a) XPS depth profile region and the XPS spectra result of stacked SiO_2/IGZO films according to the SiO_2 deposition temperature of (b) 250, (c) 300, (d) 350, and (e) 400 ^{o}C in terms of etching time.

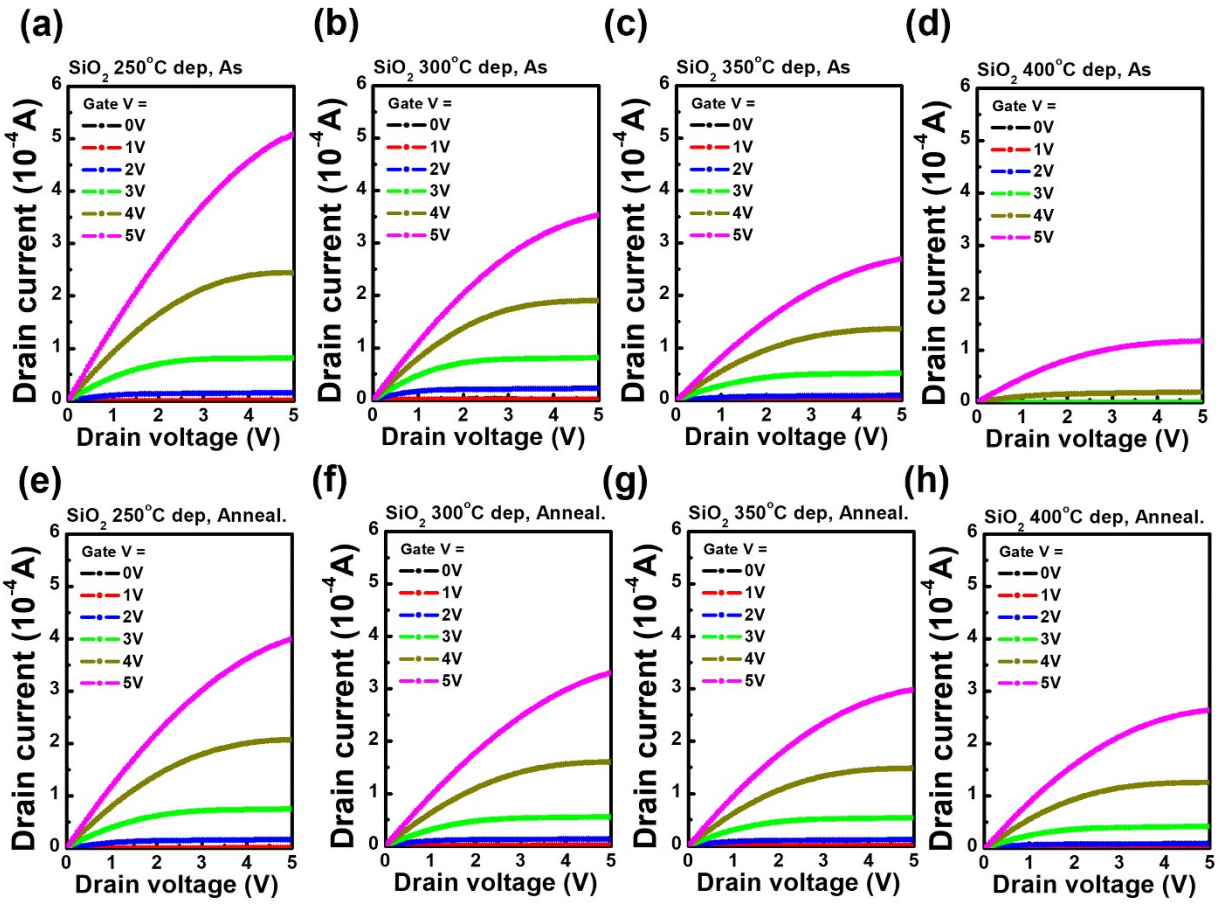
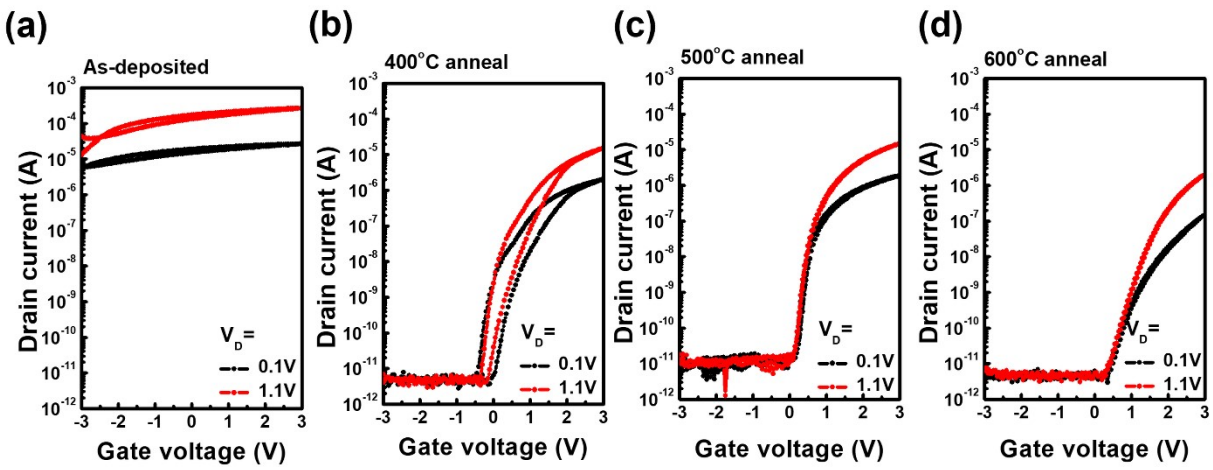


Figure S3. I–V output curves of the (a)–(d) as-deposited and (e)–(h) post-annealed TG FET devices with a SiO_2 deposition temperatures of the of (a), (e) 250, (b), (f) 300, (c), (g) 350, and (d), (h) 400 °C.

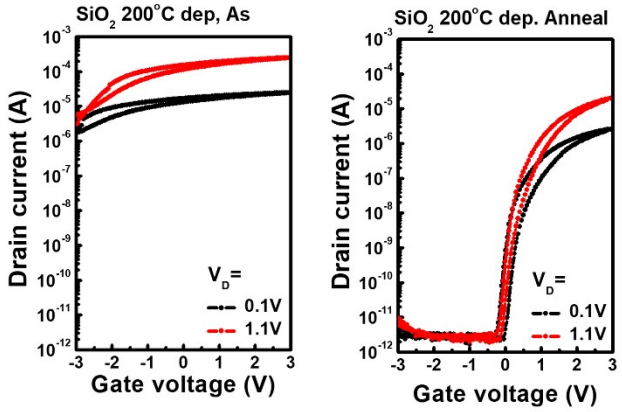


(e)

Annealing temperature	As	400	500	600
V_{th} [V]	N/A	-0.0±0.1	0.4±0.1	1.5±0.2
μ_{FE} [cm^2/Vs] @ V_D=0.1V	N/A	25.4±0.3	20.0±1.2	2.4±0.9
μ_{FE} [cm^2/Vs] @ V_D=1.1V	N/A	21.9±0.5	14.4±0.2	3.1±0.6
Hysteresis [V]	N/A	0.59±0.06	0.07±0.01	0.08±0.02
S.S. [V/dec]	N/A	0.11±0.01	0.10±0.01	0.26±0.01

Figure S4. The I–V transfer curve of (a) the as-deposited FET and after post-annealing at (b) 400, (c) 500, and (d) 600 °C. The SiO_2 GI deposition temperature of FET was 250 °C. (e) Summary of the extracted electrical properties of FET, such as threshold voltage (V_{th}), field-effect mobility (μ_{FE}), hysteresis, and subthreshold swing (S.S.).

(a) (b) (c)



	As-dep	Annealed
V_{th} [V]	N/A	0.2±0.1
μ_{FE} [cm^2/Vs]	N/A	18.0±1.5
Hysteresis [V]	N/A	0.16±0.05
S.S. [V/dec]	N/A	0.10±0.01

Figure S5. The I–V transfer curve of the (a) as-deposited and (b) after post-annealing at 500 °C. The SiO_2 GI deposition temperature of FET was 200 °C. (c) Summary of the extracted electrical properties of FET, such as threshold voltage (V_{th}), field-effect mobility (μ_{FE}), hysteresis, and subthreshold swing (S.S.).

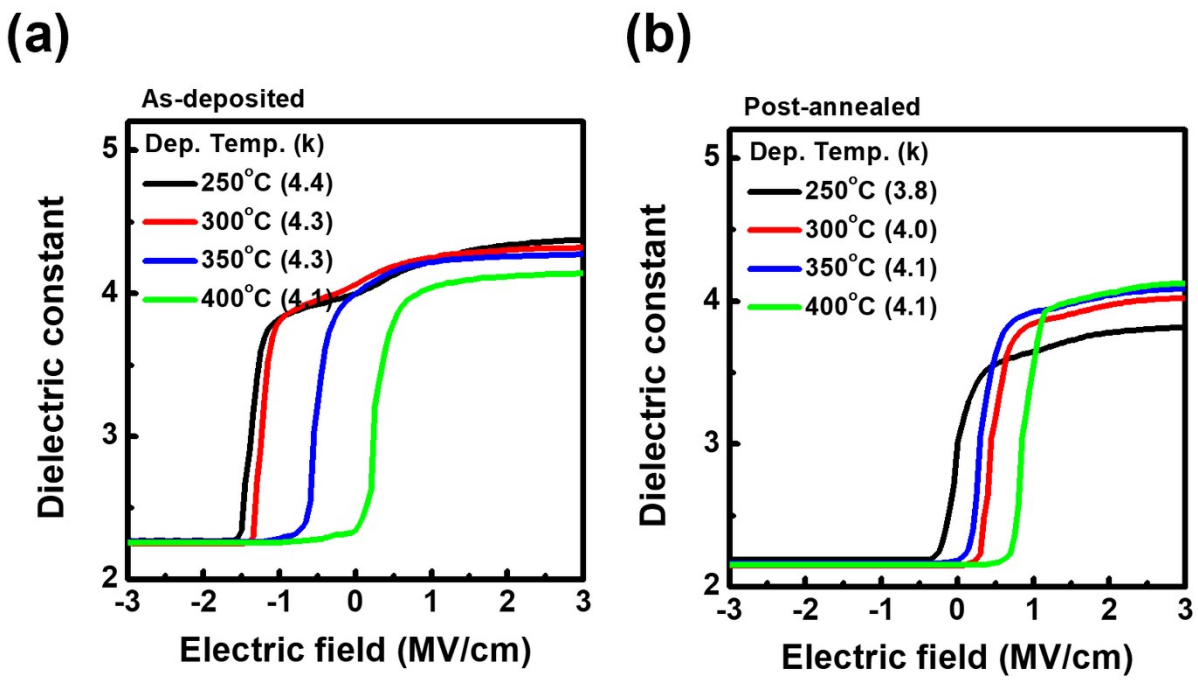


Figure S6. The C-V analysis result and dielectric constant values at the MOS region of TG FET according to the SiO_2 deposition temperature for (a) as-posited and (b) post-annealed.

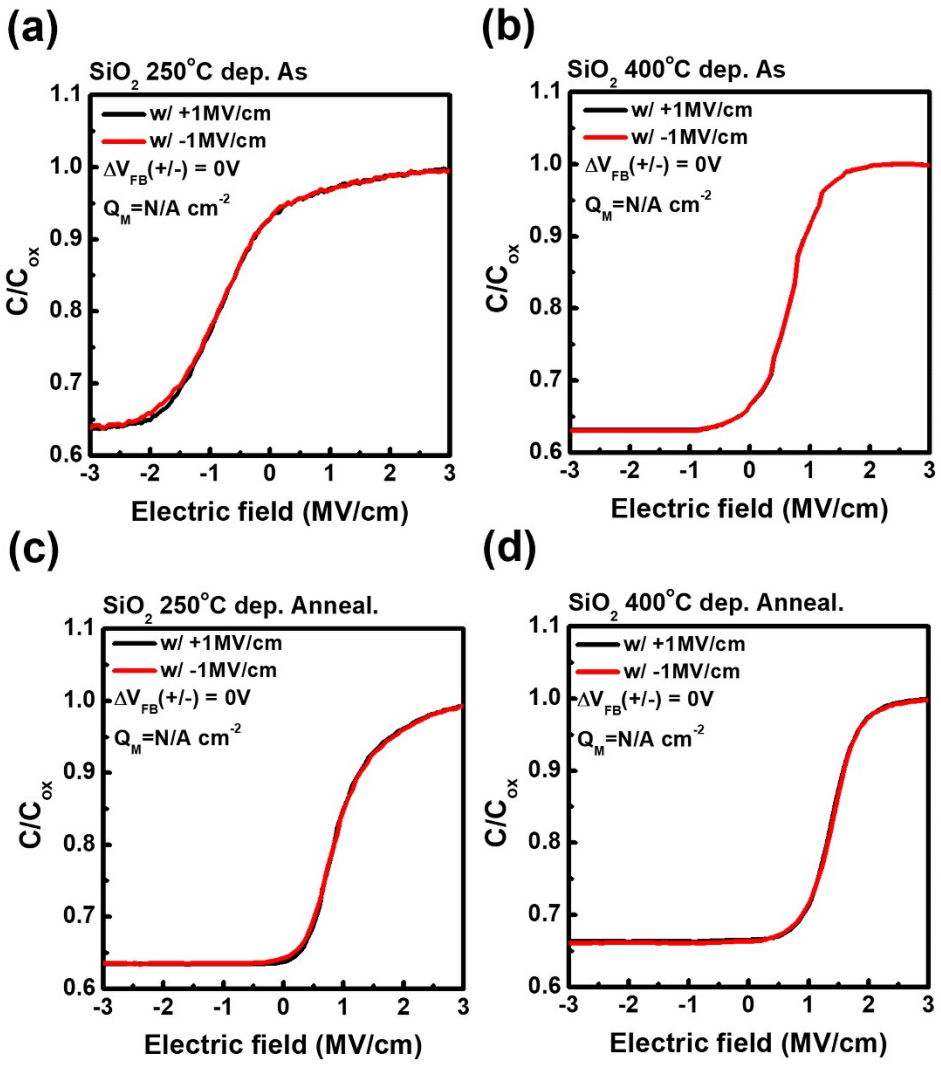


Figure S7. C–V analysis results of the (a), (b) as-deposited and (c), (d) post-annealed FETs after the ±1 MV cm^{-1} field stress at 30 °C for 2 min according to the SiO_2 GI deposition temperatures of (a), (c) 250 and (b), (d) 400 °C.

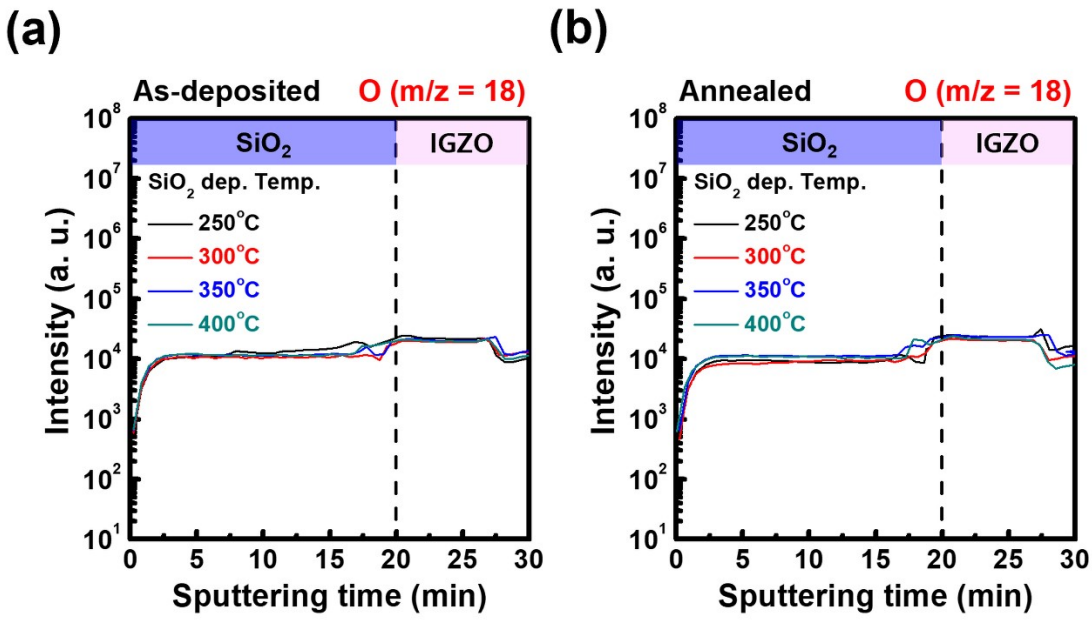


Figure S8. D-SIMS depth profiles of oxygen intensity for (a) as-deposited and (b) post-annealed SiO_2/IGZO films according to the SiO_2 deposition temperature.

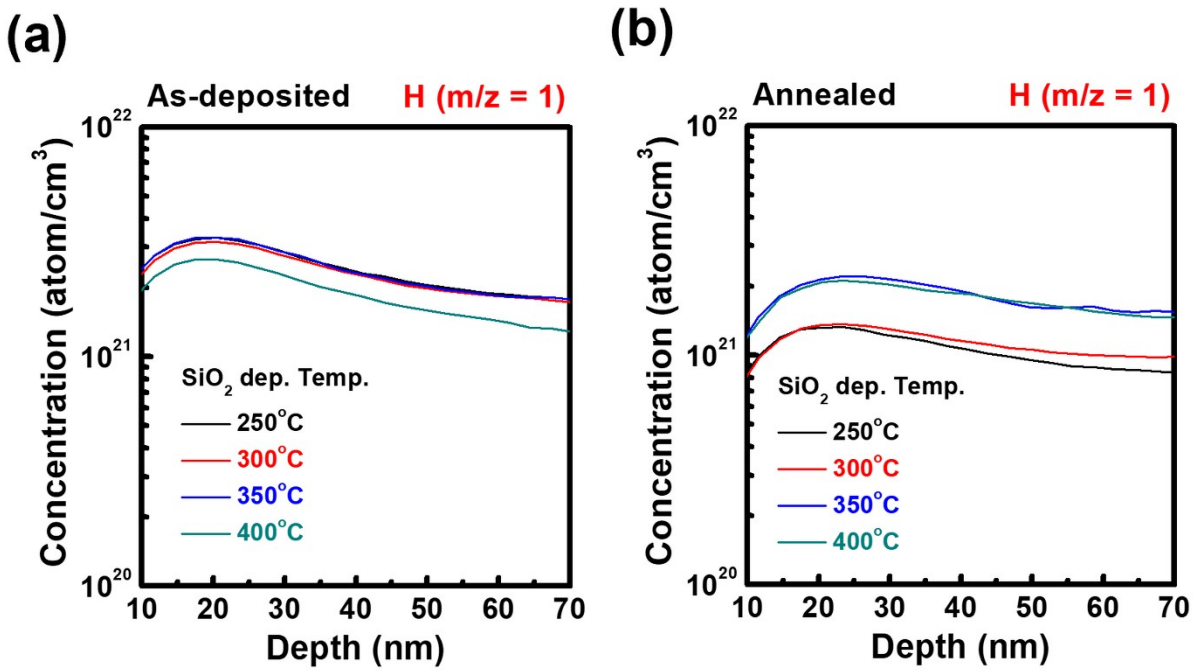


Figure S9. D-SIMS depth profiles of hydrogen concentration for (a) as-deposited and (b) post-annealed SiO_2/IGZO films according to the SiO_2 deposition temperature.

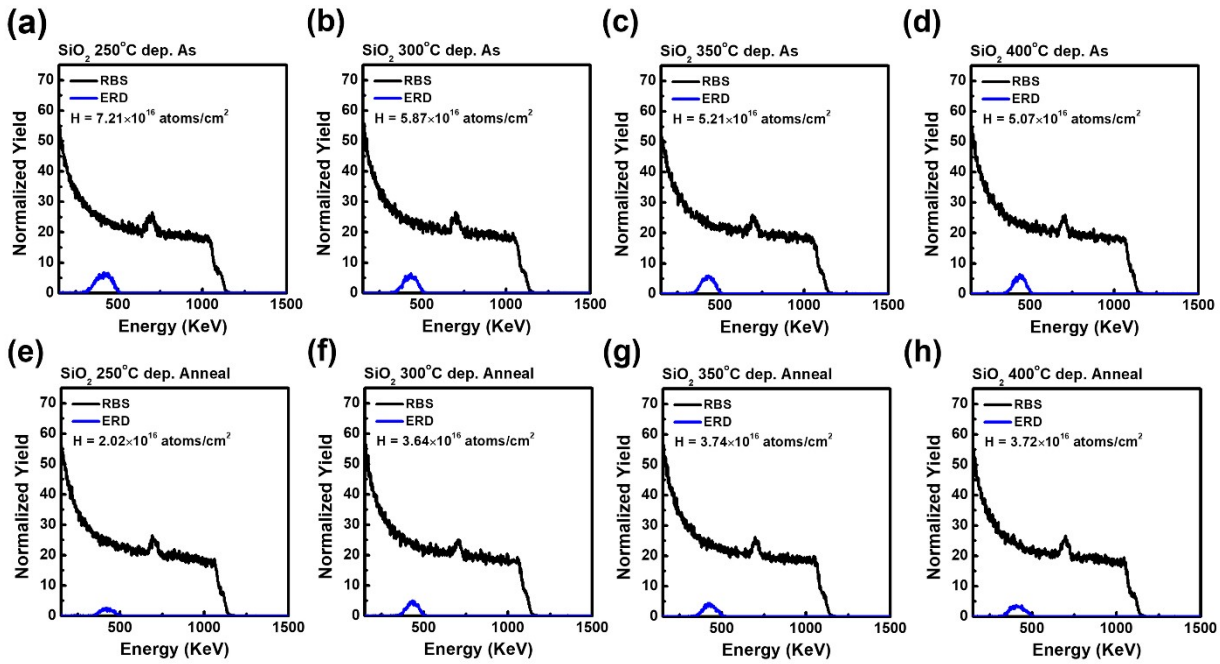


Figure S10. RBS and ERD spectra collected from (a)–(d) as-deposited and (e)–(h) post-annealed SiO_2 films with deposition temperatures of the of (a), (e) 250, (b), (f) 300, (c), (g) 350, and (d), (h) 400 °C.

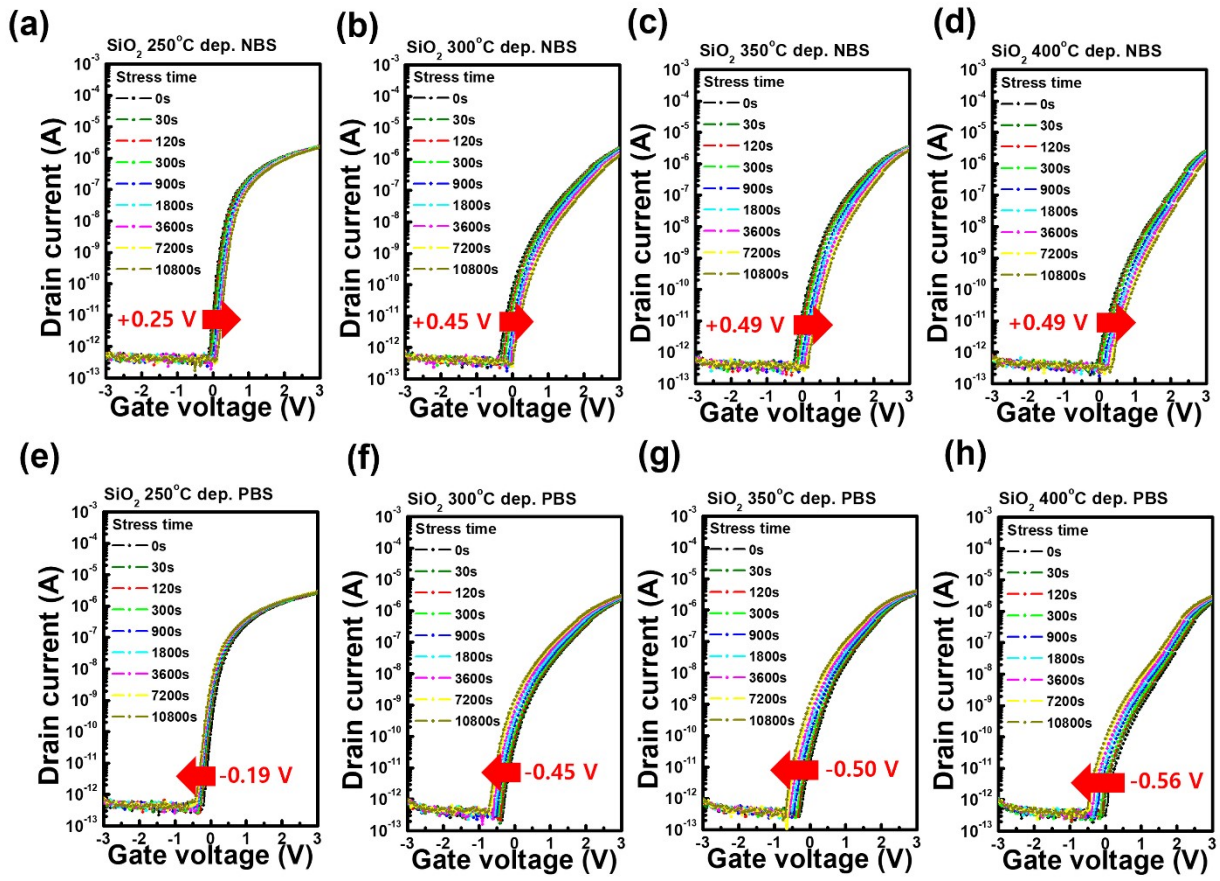


Figure S11. Transfer characteristics (I–V) during the (a)–(d) NBS and (e)–(h) PBS tests for a SiO_2 deposition temperatures of (a), (e) 250, (b), (f) 300, (c), (g) 350, and (d), (h) 400 °C.