

Supplementary Materials

Single-Molecule Nanopore Profiling of Protein Domain Fragment Dynamics and Aggregation

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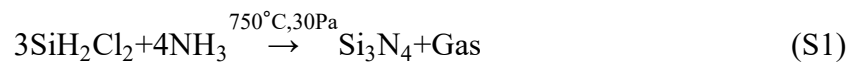
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Supplementary Note 1: MEMS Fabrication Process for Nanopore Chip Wafers

Layer Deposition

We initiated fabrication with a 220 μm -thick silicon wafer, which underwent sequential piranha ($\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2$ 3:1) and RCA cleaning to eliminate organic and ionic contaminants. A 1 μm SiO_2 layer was thermally grown at 1000 $^\circ\text{C}$ under dry oxygen to serve as an etch stop. Subsequently, a 100 nm Si_3N_4 film was deposited via low-pressure chemical vapor deposition (LPCVD) at 750 $^\circ\text{C}$ using dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) precursors (see eq S1). Stress management during Si_3N_4 deposition ensured minimal wafer curvature (<5 μm bow), verified through laser interferometry.



Front-Side Patterning and Membrane Thinning

We patterned the front-side Si_3N_4 layer by spin-coating LC100A photoresist at 2000 rpm, followed by UV exposure through a chrome mask defining 2.5 μm circular regions. After development in MF-319, reactive ion etching (RIE) with a CHF_3/O_2 plasma (20 sccm, 100 W RF power) thinned the Si_3N_4 from 100 nm to 20 nm in exposed areas. Oxygen plasma ashing and acetone rinsing removed residual resist, leaving clean, anisotropic edges critical for membrane integrity.

Back-Side Etch Window Formation

Aligning to front-side features with <1 μm tolerance, we defined a 323 $\mu\text{m} \times 323$ μm back-side etch window via photolithography. A two-step RIE process first removed Si_3N_4 , then etched the underlying SiO_2 to expose the silicon substrate. This dual-layer etch prevented unintended membrane perforation during subsequent bulk silicon removal.

Bulk Silicon Etching and Membrane Release

Potassium hydroxide (KOH, 30 wt%, 50 $^\circ\text{C}$) selectively etched the silicon through the back-side window at 11 $\mu\text{m} \cdot \text{h}^{-1}$, terminating at the SiO_2 layer after ~ 20 hr. The resulting cavity exhibited (111)-plane sidewalls with 54.7 $^\circ$ angles. We then immersed the wafer in buffered

oxide etch (6:1 $\text{NH}_4\text{F}:\text{HF}$) for 13 min to dissolve the 1 μm SiO_2 layer, releasing a 40 μm \times 40 μm freestanding Si_3N_4 membrane.

Figure S1 illustrates the MEMS fabrication process, and Figure S2 details the structure of the SiN membrane chip. Figure S3 provides a comprehensive visualization of the nanopore membrane chip. The 2.5 μm circular region is approximately 80 nm deep (characterized by previous AFM scanning¹) and will be further thinned by 10 nm using Focus Ion Beam (FIB).

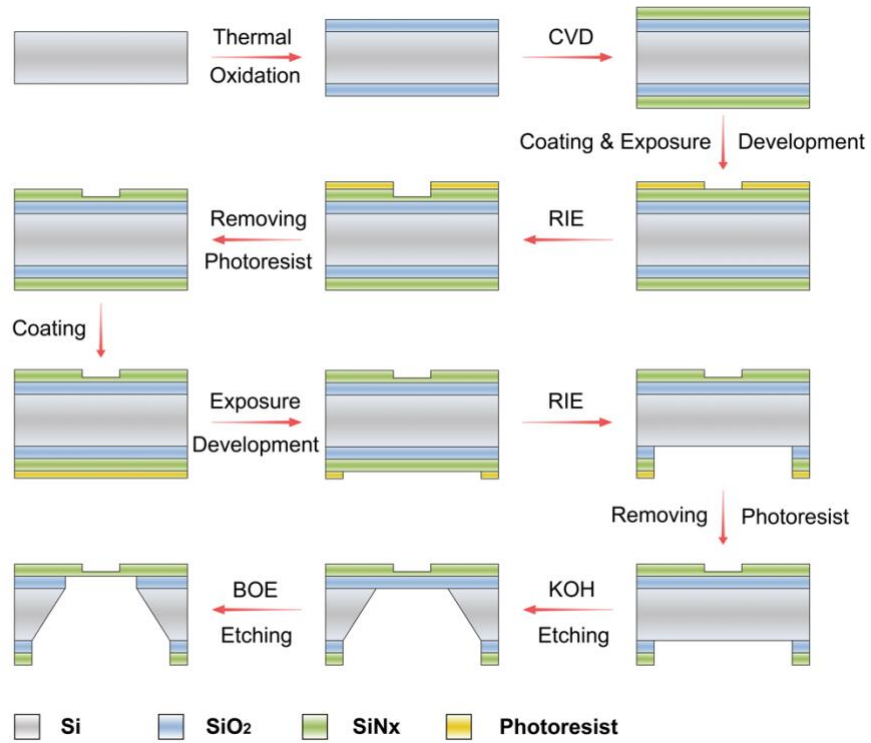


Figure S1. Wafer preparation process. The steps are as follows: thermal oxidation, chemical vapor deposition, spinning, exposure, and development of the front photoresist, front reactive ion etching, photoresist removal, spinning, exposure, and development of the back photoresist, back reactive ion etching, photoresist removal, KOH wet etching, and BOE wet etching.

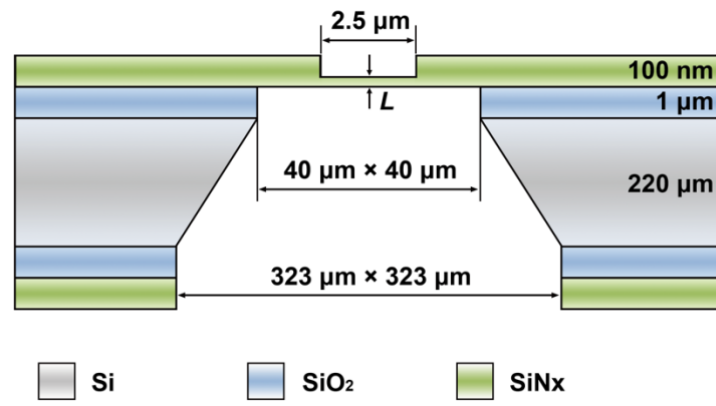


Figure S2. Schematic diagram of the silicon nitride nanopore membrane chip structure, including the silicon nitride layer, silicon oxide layer, and silicon substrate.

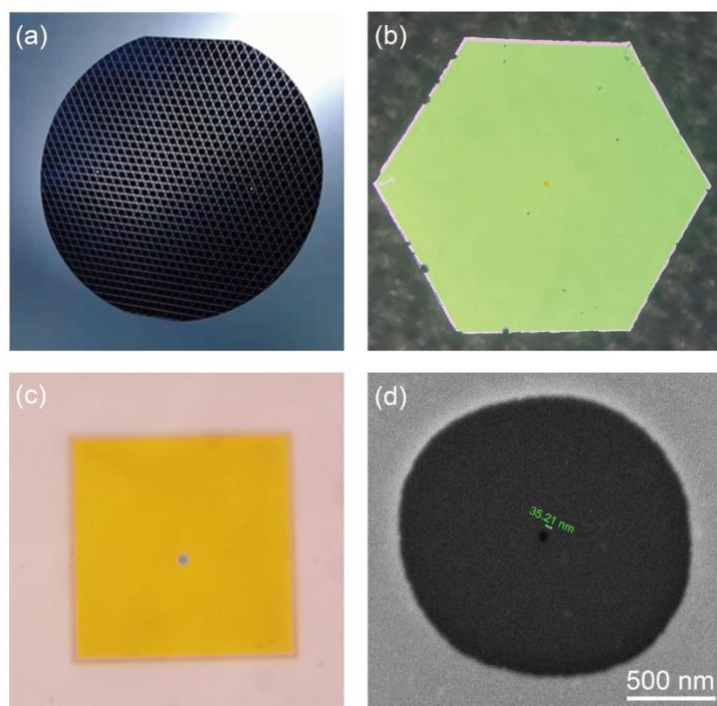


Figure S3. Characterization of fabricated wafers containing nanopore membranes. (a) Optical image of the complete wafer following laser dicing. (b) Microscopic image of an individual chip at 50× magnification. (c) Microscopic visualization of the silicon nitride membrane window at 1000× magnification, where dark regions indicate thinned areas (2.5 μm). (d) SEM micrograph of the thinned region, with dark circular features representing 35 nm diameter nanopores fabricated via FIB milling.

Supplementary Note 2: Nanopore Fabrication via Controlled Dielectric Breakdown

Figure S4a illustrates our experimental setup for CDB². We first treated the silicon nitride chip in a plasma cleaner for 30 s, then placed it in a custom-made PMMA flow cell. We filled the *cis* and *trans* side of the flow cell with degassed, filtered 1 M KCl solution buffered with 10 mM Tris-HCl at pH 8, positioning the chip between the two halves. We connected two Ag/AgCl electrodes to a Keithley 2612A source meter (Keithley Instruments, Cleveland, USA) and immersed the opposite ends in each compartment. We applied a constant or pulsed voltage and recorded the resulting current at 20 Hz. Voltages ranged from 2 V to 10 V, with thicker membranes requiring proportionally higher breakdown thresholds. For a 10 nm thick membrane, the electric field reached approximately $0.1\sim0.5\text{ V}\cdot\text{nm}^{-1}$. As the voltage applied, we observed a stable leakage current. A sudden current increase indicated dielectric breakdown, during which nanopores formed and allowed ion transport. We implemented a feedback control algorithm to define a cutoff current ($I_{\text{cutoff}}/I_{\text{leakage}}=R$) that automatically halted the voltage upon reaching R , preventing subsequent pore growth.

We attribute dielectric breakdown to pre-existing defects (holes) in the silicon nitride membrane, which enable electron tunneling from ionic species and generate leakage current. Additionally, accumulated high-energy charges at the membrane surface then promoted local energy dissipation, while Joule heating caused damage to the membrane, forming nanopores (Figure S4b). We conducted a bias sweep from -500 mV to $+500\text{ mV}$ in 100 mV increments to obtain I - V curves. Figure S4c presents the I - V curves of 5 nanopores, with diameters ranging from 5 nm to 30 nm.

We modulated the nanopore diameter by adjusting the applied voltage (electric field strength). Figure S5 plots the calculated nanopore diameter versus time under sequential increases in electric field strength. As the field ramps from $0.05\text{ V}\cdot\text{nm}^{-1}$ to $0.45\text{ V}\cdot\text{nm}^{-1}$, the nanopore diameter extends from approximately 10 nm to beyond 100 nm.

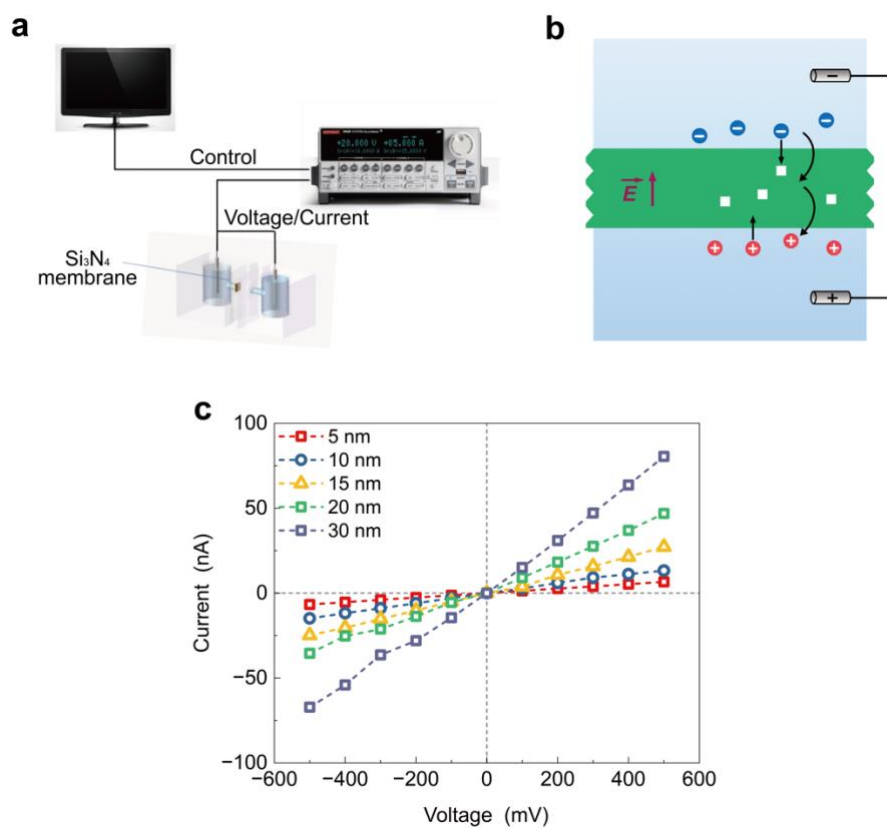


Figure S4. Nanopore fabrication via controlled dielectric breakdown (a) Schematic of the experimental setup for controlled dielectric breakdown (CDB). (b) Mechanism of nanopore formation in CDB. (c) I–V curves for five nanopores (5~30 nm in diameter), swept under bias voltages from –500 mV to +500 mV.

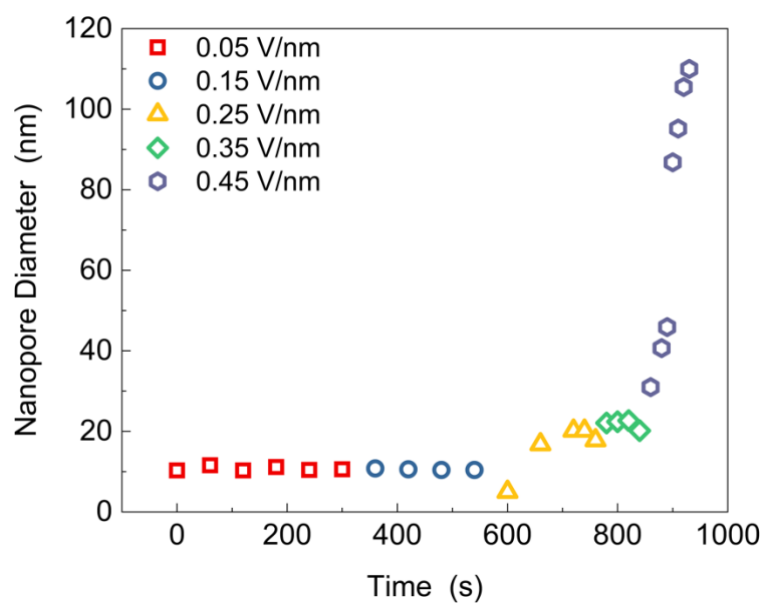


Figure S5. Calculated nanopore diameter versus time under sequential increases in electric field strength.

Supplementary Note 3: Current Traces in Nanopores of Different Diameters

We employed nanopores of different diameters to detect protein fragments, and Figure S6 illustrates their corresponding current traces. For the 5 nm nanopore, the ionic current remained at a stable open-pore level after addition of either 7CE0 or 7CDZ, and no resolvable transient blockade events were detected. We did not observe signatures of immediate clogging. Given that both peptides are smaller than the pore diameter, we attribute the absence of detectable events to a high translocation energy barrier in these small pores.

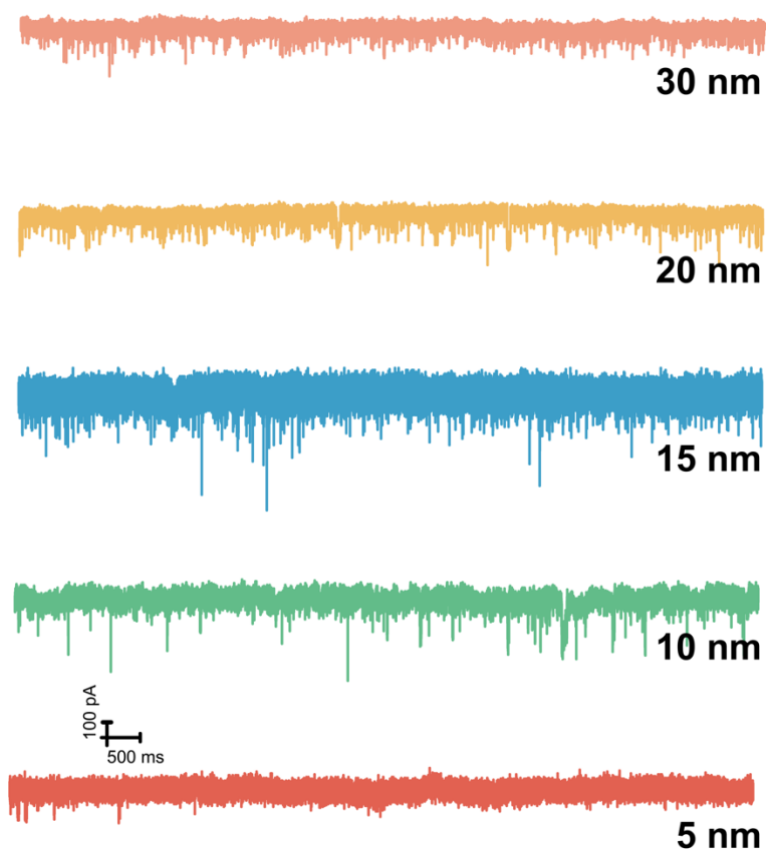


Figure S6. Current traces and translocation signals in nanopores of different diameters.

Supplementary Note 4: Volume Analysis of Protein Fragments via MD Simulations

We determined protein fragment volumes using the VolMap plugin³ in Visual Molecular Dynamics (VMD). First, each fragment's coordinate file (PDB format) was loaded into VMD. We then employed the VolMap plugin to generate a three-dimensional density map by discretizing the surrounding space into a grid, ensuring the density cutoff adequately encompassed the fragment. The VolMap plugin calculates the enclosed volume by summing volumetric elements whose density values exceed the specified threshold. Figure S7 shows the snapshots of the two fragment 7CE0 and 7CDZ in simulations, respectively. The measured volumes of 7CE0 and 7CDZ are 29.3 nm³ and 44.3 nm³, respectively.

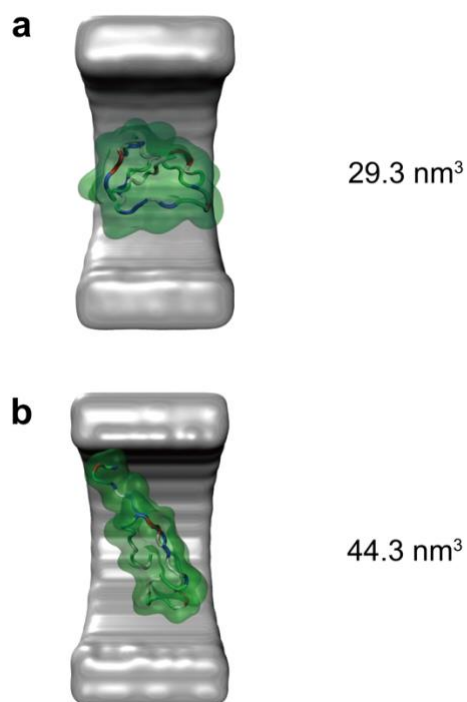


Figure S7. Snapshots of the two protein fragments 7CE0 (a) and 7CDZ (b) in simulation. Using the VolMap plugin in VMD, their volumes were measured to be 29.3 nm³ and 44.3 nm³, respectively.

Supplementary Note 5: Protein–Nanopore Surface Interactions

Throughout the translocation of the 7CDZ fragment, we observed strong interactions with the nanopore surface, which likely contributed to its prolonged translocation time. These interactions appear to be driven by positively charged residues on 7CDZ that associate with the negatively charged nanopore surface (Figure S8).

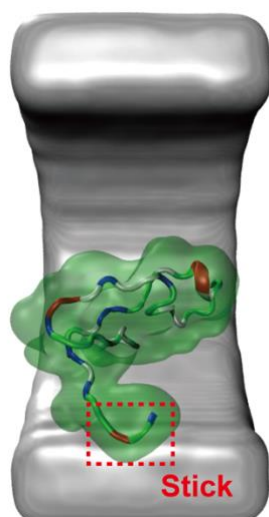


Figure S8. A representative snapshot illustrating the interactions between the 7CDZ fragment and the nanopore surface.

Supplementary Note 6: Supplementary Density Plots

Figure S9 presents the density plot ($\Delta I/I_0$ vs. dwell time) for 7CE0 fragment translocation events measured in a 15 nm nanopore. Figure S10 shows the corresponding density plot obtained with a 20 nm nanopore, and Figure S11 illustrates the density plot measured at a 600 nM fragment concentration.

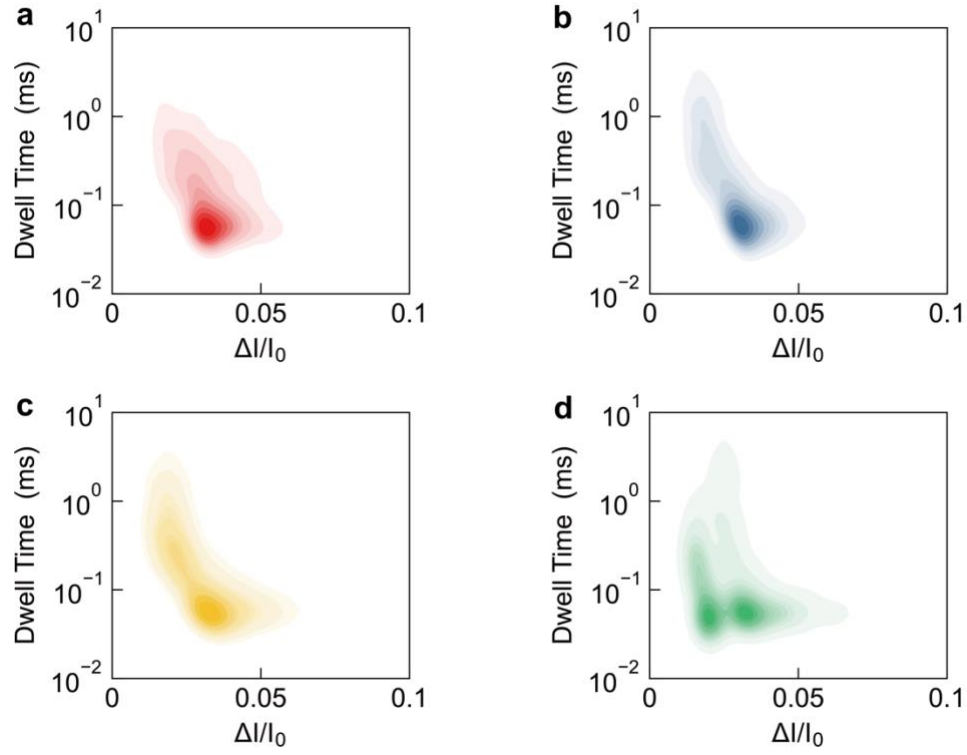


Figure S9. Density plot ($\Delta I/I_0$ vs. dwell time) for 7CE0 fragment translocation events measured in a 15 nm nanopore. (a) 70 mV. (b) 80 mV. (c) 90 mV. (d) 100 mV.

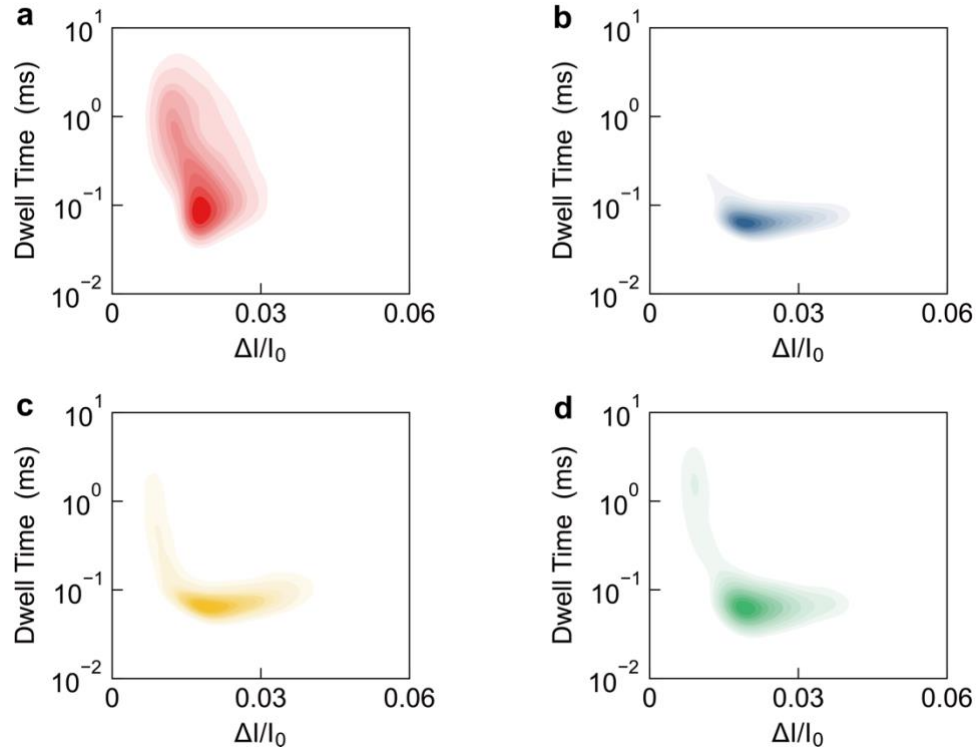


Figure S10. Density plot ($\Delta I/I_0$ vs. dwell time) for 7CE0 fragment translocation events measured in a 20 nm nanopore. (a) 70 mV. (b) 80 mV. (c) 90 mV. (d) 100 mV.

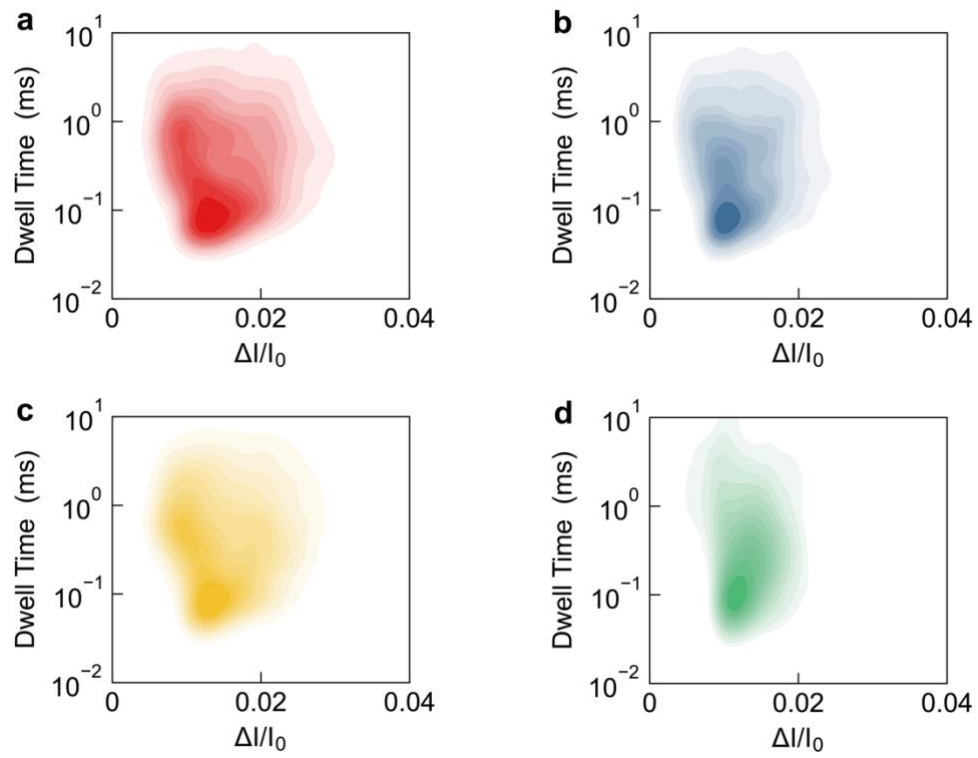


Figure S11. Density plot ($\Delta I/I_0$ vs. dwell time) for 7CE0 fragment translocation events measured at a 600 nM fragment concentration. (a) 70 mV. (b) 80 mV. (c) 90 mV. (d) 100 mV.

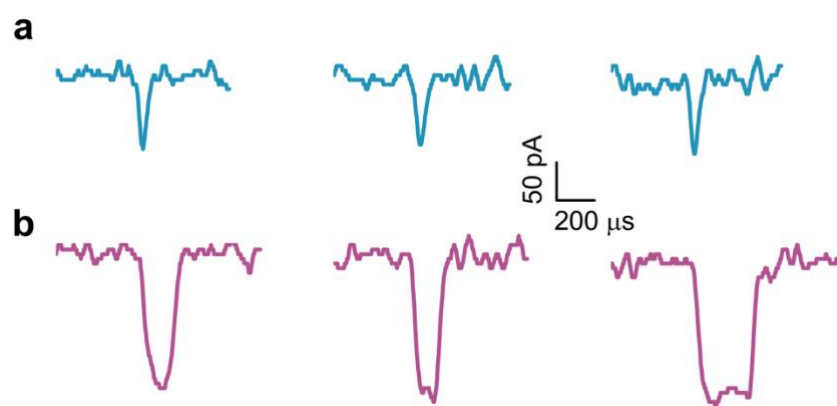


Figure S12. Representative current traces for (a) 7CE0 monomer and (b) 7CE0 dimer translocation events through a solid-state nanopore at +80 mV.

References:

1. Liu, W.; Zhang, Y.; Gu, Z.; et al. *IEEE Sens. J.* **2024**, *24* (3), 2405–2412.
2. Zhan, L.; Zhang, Z.; Zheng, F.; et al. *J. Phys. Chem. Lett.* **2023**, *14* (50), 11536–11542.
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