Supplementary Information

A Universal Self-Triggered Passive Management Strategy for Output Power of Triboelectric Nanogenerator

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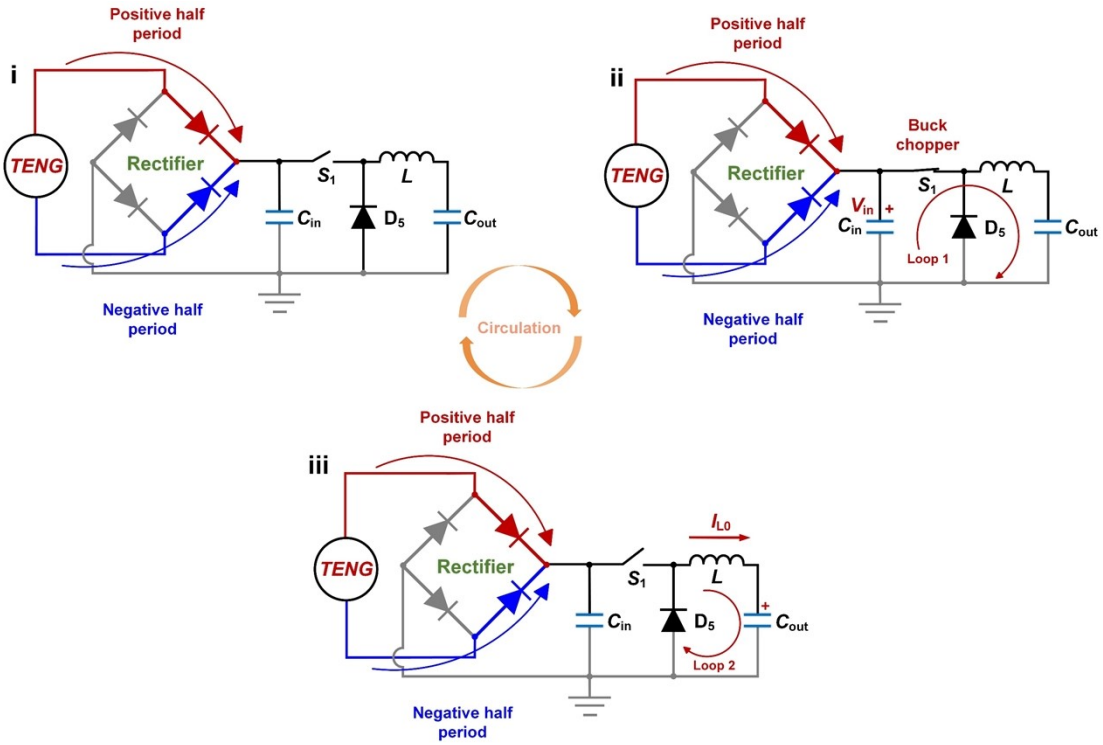
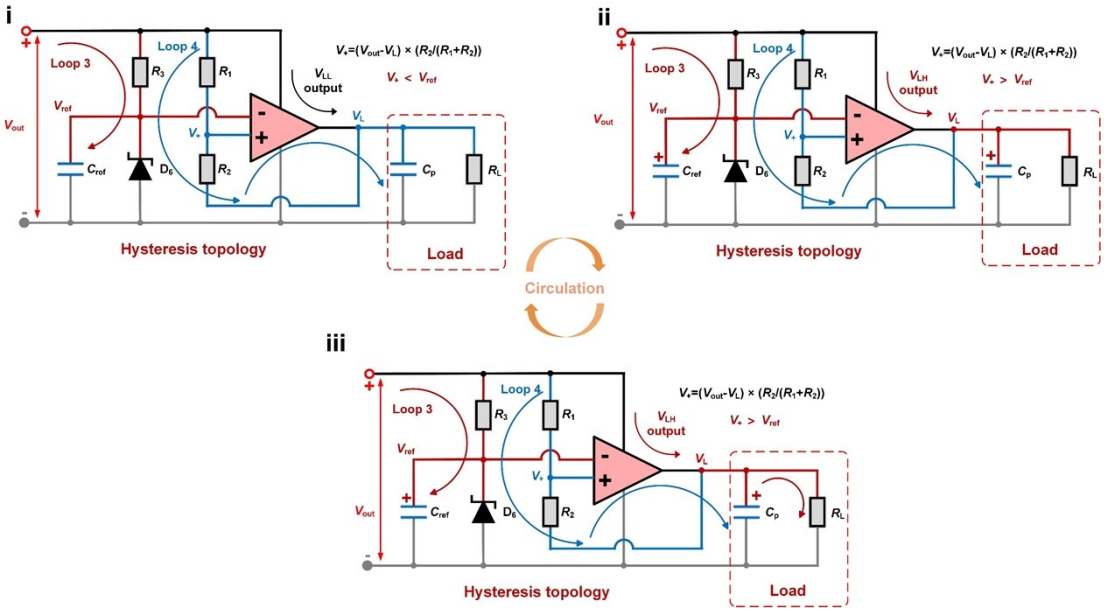
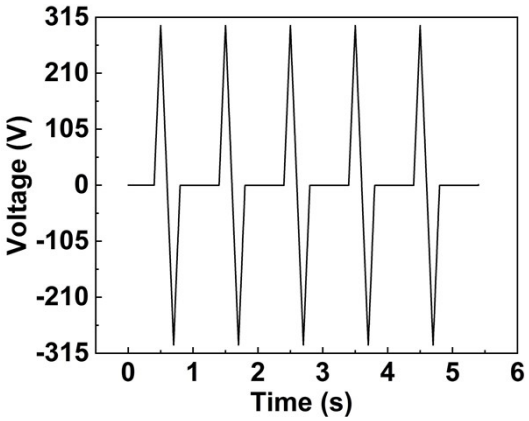


Supplementary Fig. 1. Schematic diagram of the buck circuit operation.



Supplementary Fig. 2. Schematic diagram of the hysteresis comparator circuit operation.



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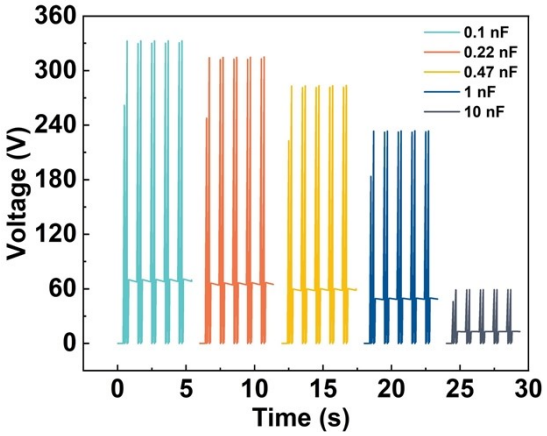

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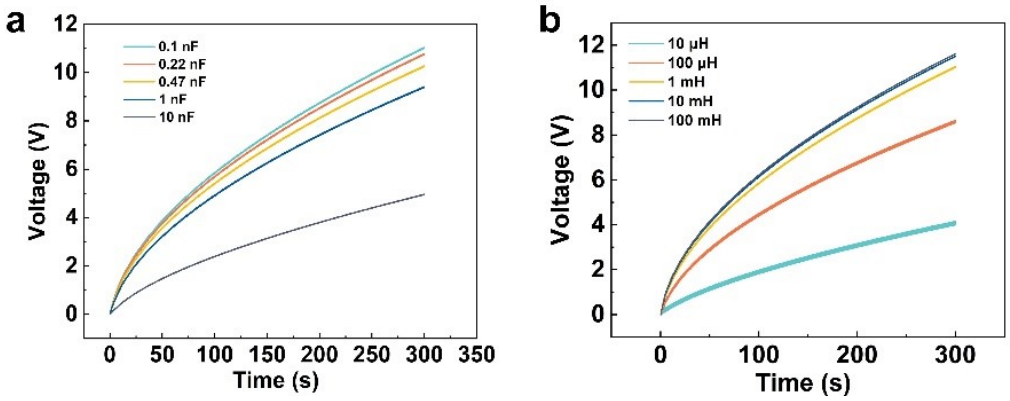

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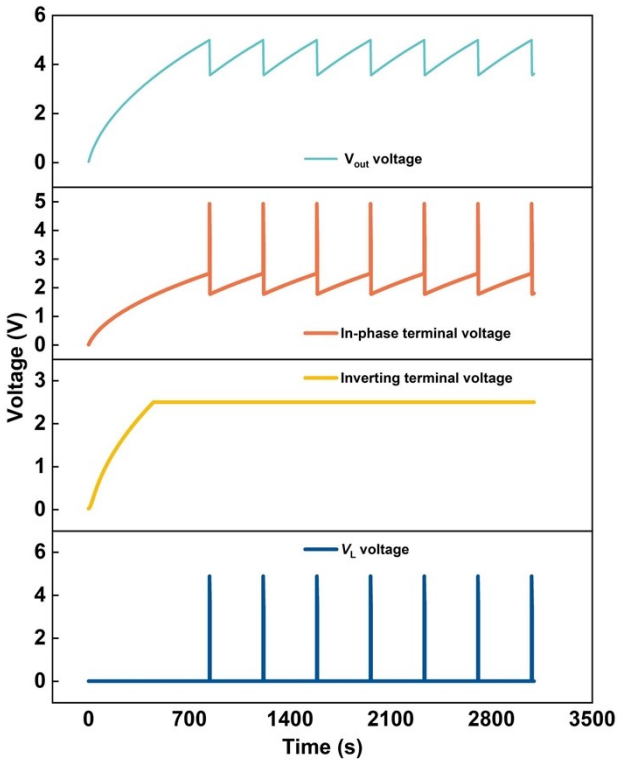

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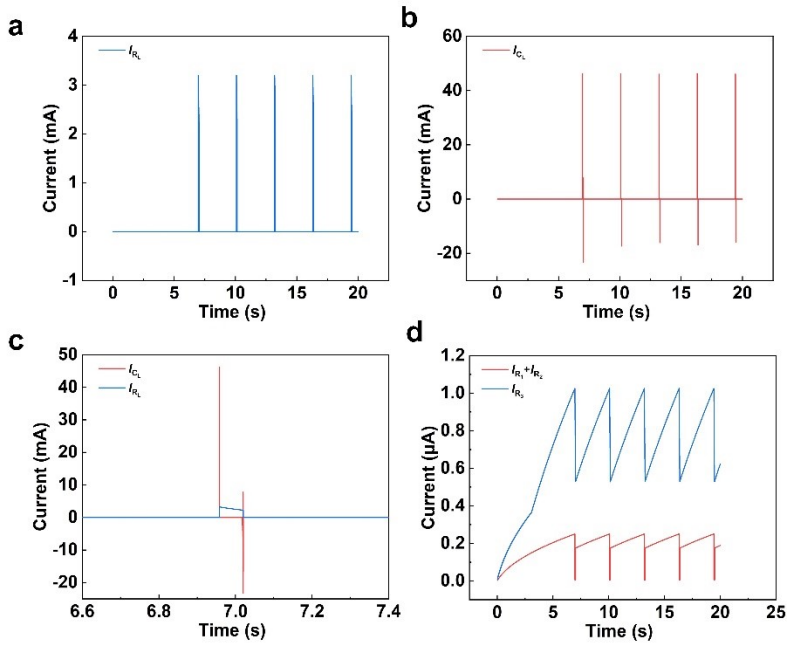

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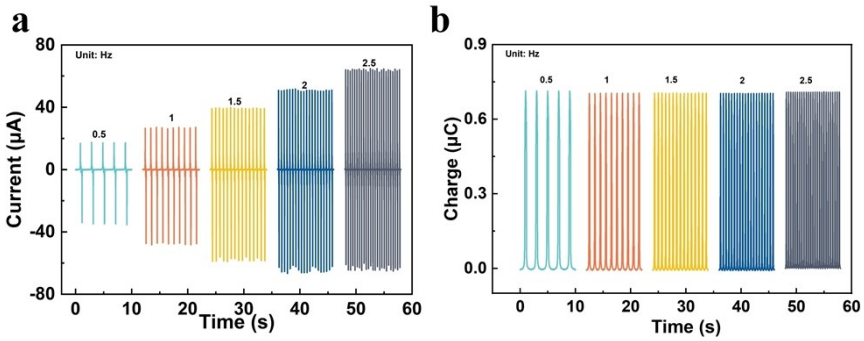

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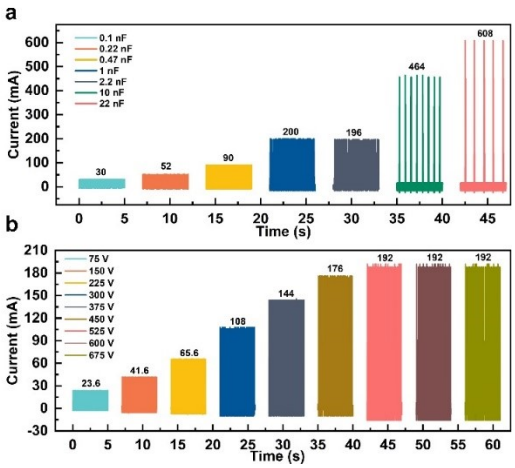

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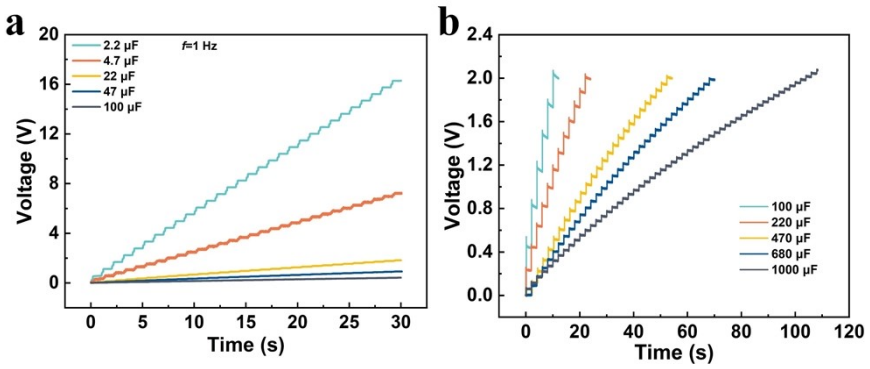

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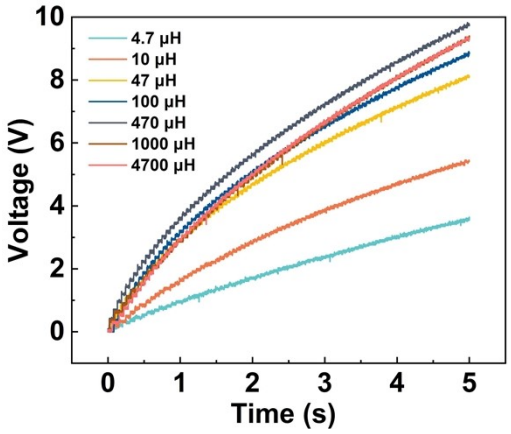

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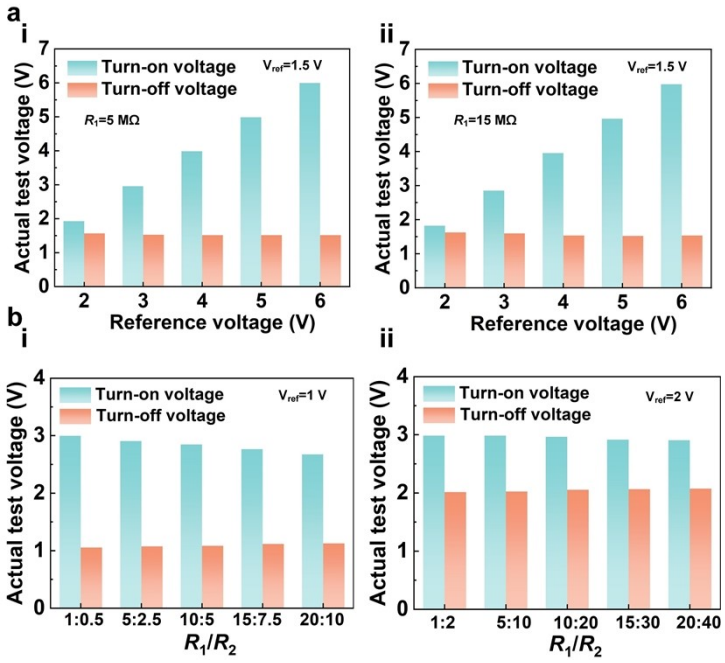

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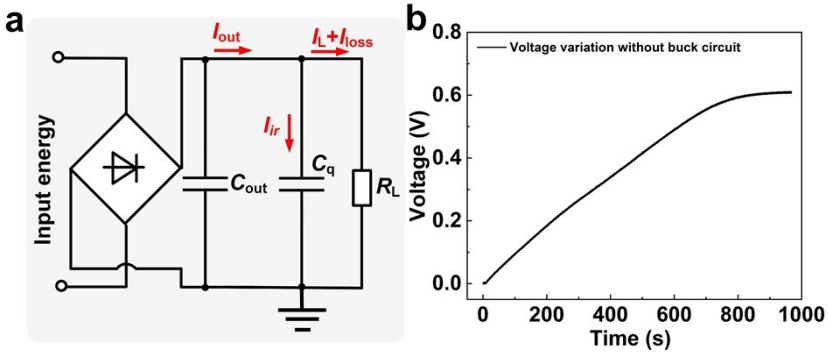
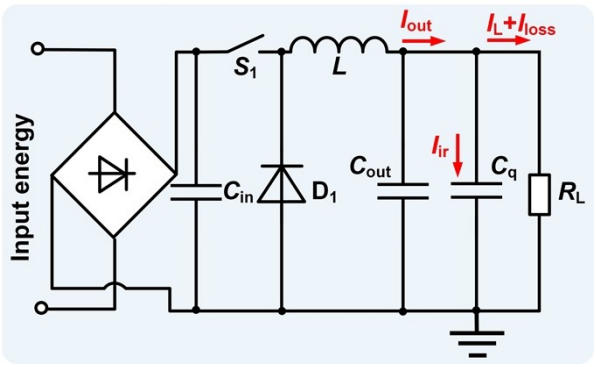


Supplementary Fig. 13. TENG directly powering the load after rectification. **a** Circuit diagram. **b** Output voltage waveform.



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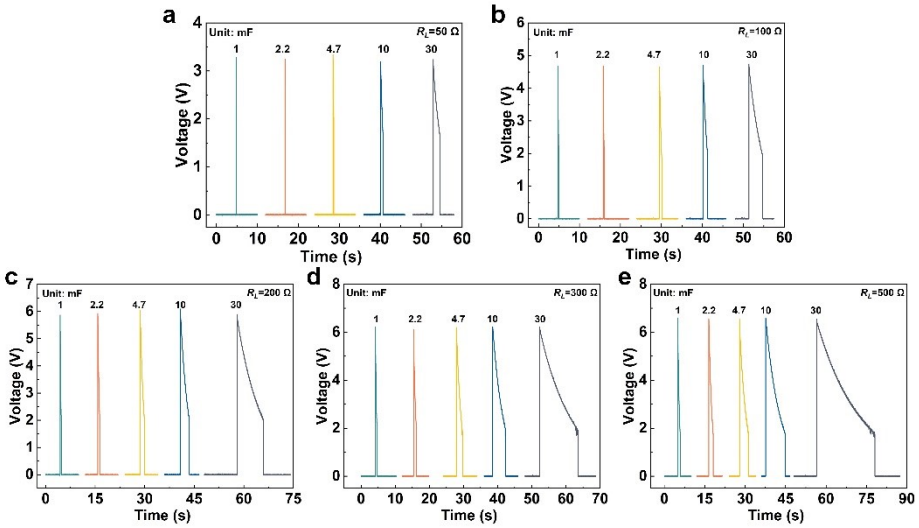

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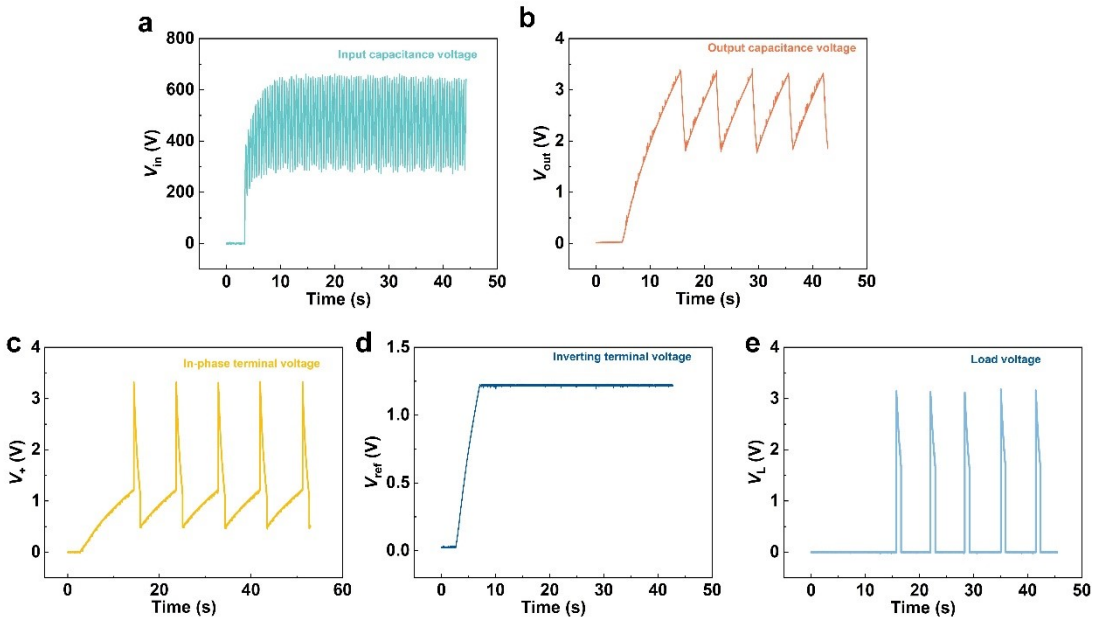

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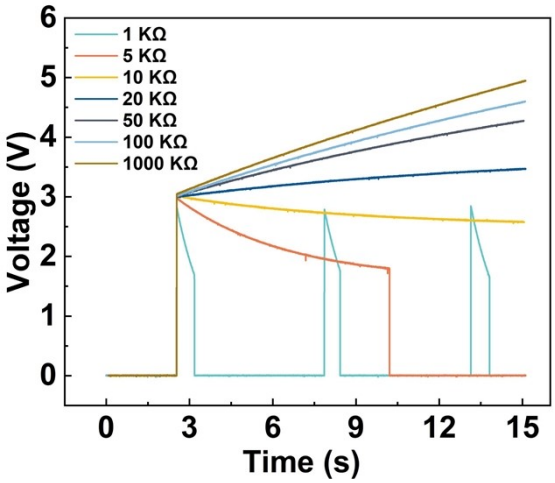

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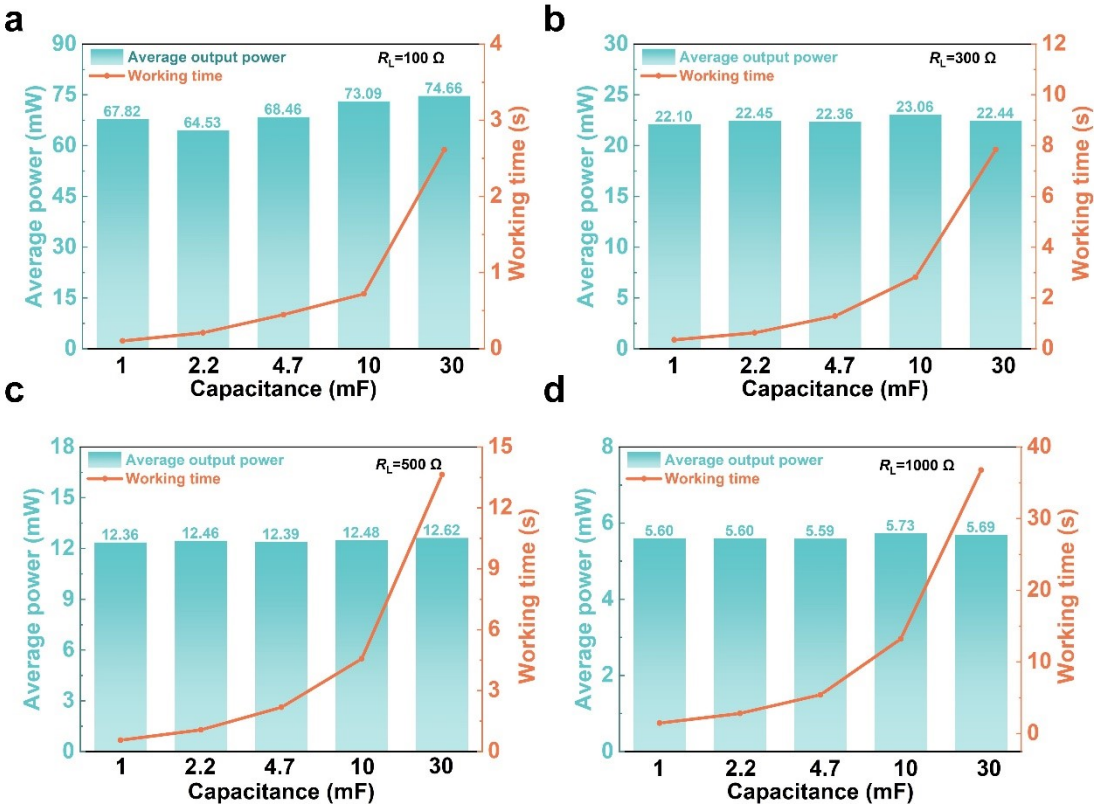
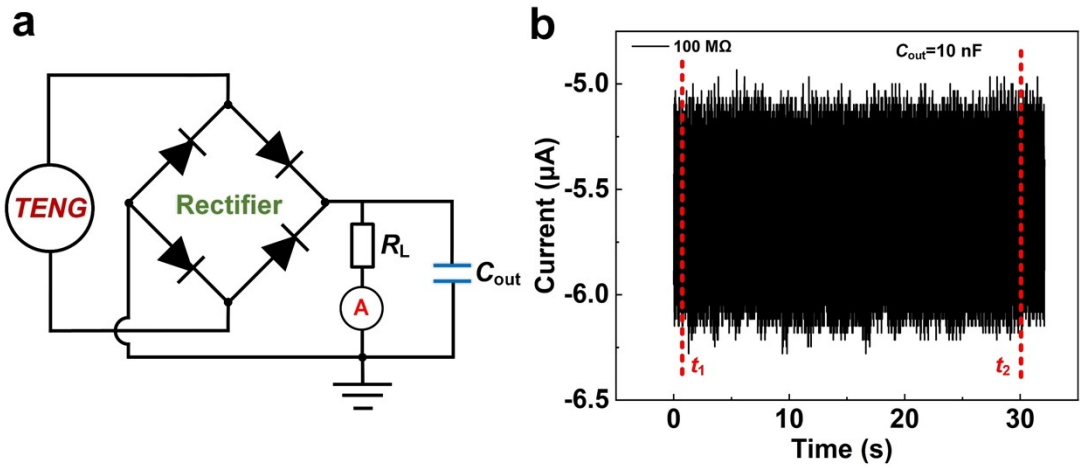


Supplementary Fig. 18. Output power and duration variation with different loads. **a** 100 Ω. **b** 300 Ω. **c** 500 Ω. **d** 1000 Ω.



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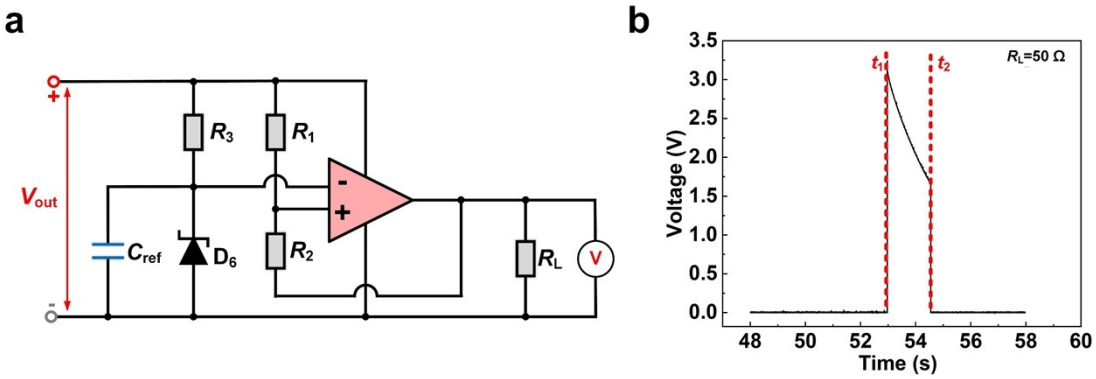

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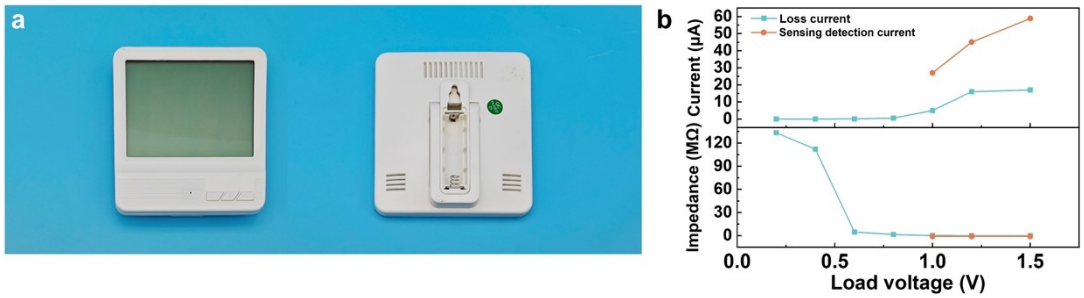

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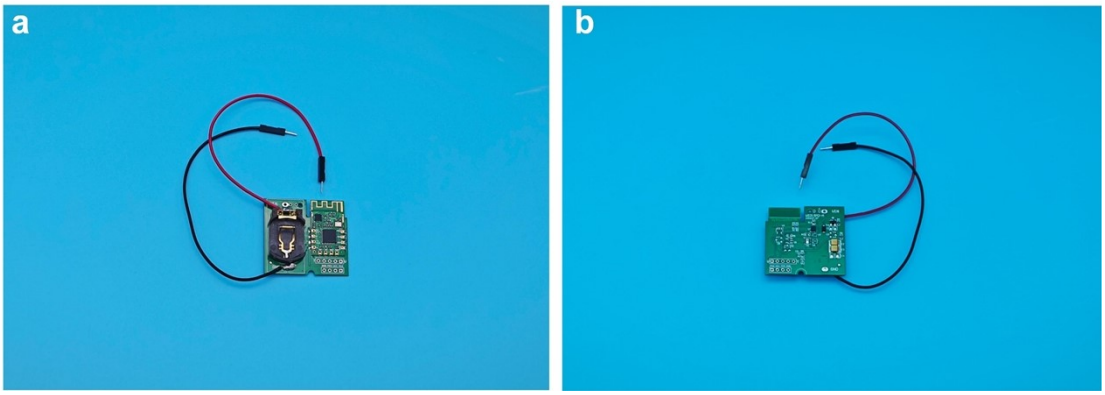

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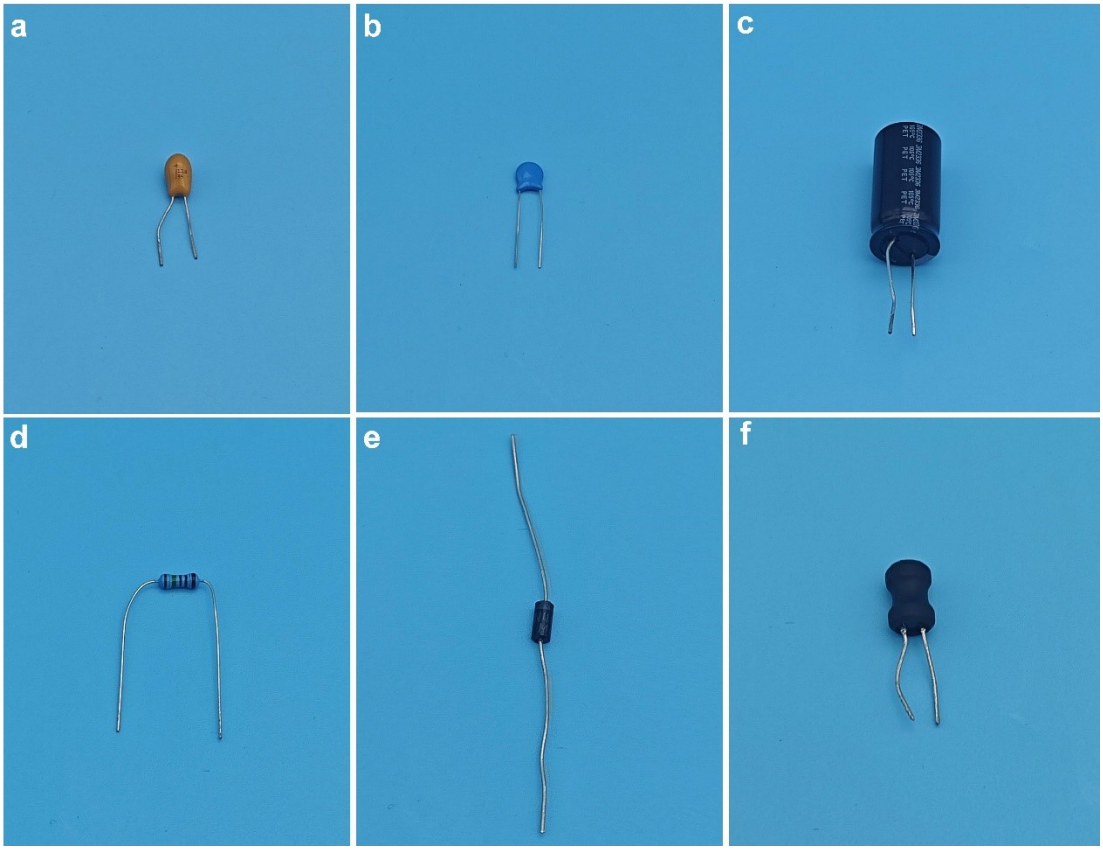
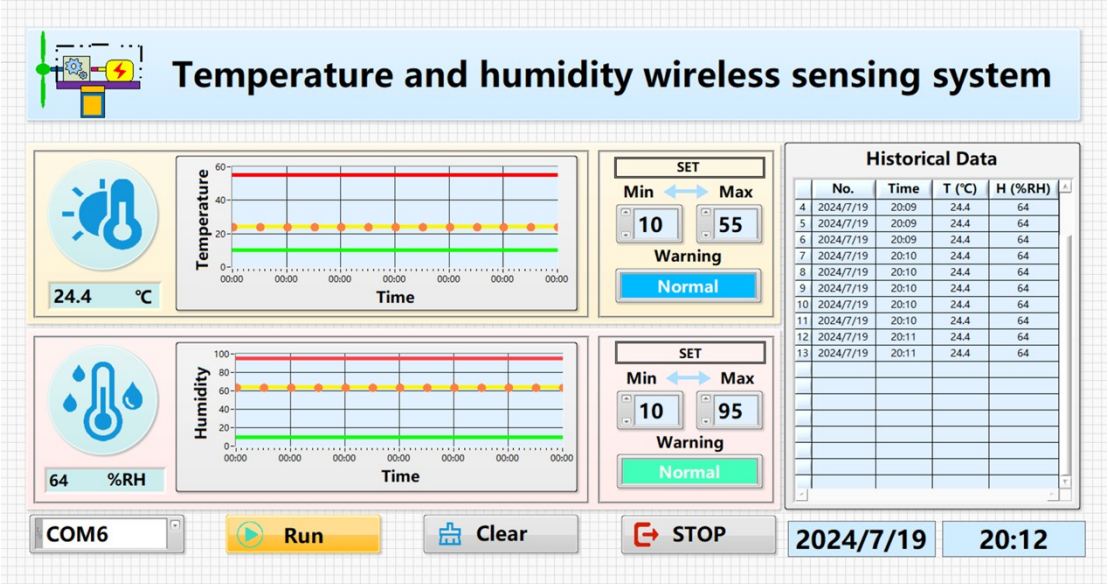


Supplementary Fig. 23. Photographs of passive components used. **a** Tantalum capacitor. **b** Ceramic capacitor. **c** Electrolytic capacitor. **d** Metal film resistor. **e** Diode. **f** Drum core inductor.



Supplementary Fig. 24. Application test host computer display interface.

Supplementary Note 1. Buck circuit workflow and principal analysis.

Figure S1 shows the basic working principle of the Buck module in the system. As the electrodes in the Triboelectric Nanogenerator move back and forth, they generate an AC signal. This AC signal is rectified into DC by a rectifier circuit, and the energy is stored in the input capacitor C_{in}, as shown in Figure S1(i). The design allows the TENG output to be processed smoothly and efficiently, providing a stable energy supply to the subsequent circuits.

The switching mechanism S_1 uses a silicon controlled rectifier (SCR) and a zener diode connected in reverse parallel. When V_{in} rises to the Zener diode's breakdown voltage, the diode breaks down, triggering the SCR to turn on, and allowing the charge stored in C_{in} to transfer to the rear inductor, as shown in Figure S1(ii). Input capacitance C_{in}, the switching device, inductor L, and output capacitor C_{out} form a circuit loop. The SCR is a semi-controlled device, and when the current drops below the holding current, the SCR turns off. At that point, L, C_{out}, and the freewheeling diode D_5 form a loop. In order to maintain the current direction, L generates a back electromotive force, and the stored energy is transferred to C_{out}, as shown in Figure S1(iii). This process converts the high-voltage, low-current signal from the TENG into a low-voltage, high-current output, which is better suited for powering downstream circuits or loads.

Supplementary Note 2. Hysteresis circuit workflow and principal analysis.

Figure S2 illustrates the basic working principle of the hysteresis module. The hysteresis circuit is connected in parallel with C_{out}, and V_{out} serves as the input voltage for the hysteresis module. The input side forms a loop with R_3, the reference capacitor $C_{ref,}$ and the voltage divider reference source D_6. R_1, R_2, and the load form another loop. C_{ref} provides a reference voltage V_{ref} to the inverting terminal of the comparator, while V_{out} is divided by R_1 and R_2 to provide the non-inverting terminal voltage V_+. When V_+ is lower than V_{ref}, the comparator outputs a low-level signal V_{LL}, as shown in Figure S2 (i). When V_+ exceeds V_{ref}, the comparator outputs a high-level signal V_{LH}, as shown in Figure S2 (ii). For the load model used in this study, the system first charges the capacitor C_p to the input voltage, and then both the capacitor and the input power supply the load, as shown in Figure S2 (iii).

In hysteresis circuit, the front-end buck circuit transfers the input energy from the TENG to the C_{out}. When the energy in the storage capacitor accumulates to a certain level and the voltage reaches the load's operating voltage, the comparator outputs a high level and powers the load. Notably, during the power supply process, both the energy storage capacitor and the TENG contribute to the output power, rather than relying entirely on the real-time output of the TENG, which effectively enhances the system's average output power.

Supplementary Note 3. System simulation test.

Figure S3 illustrates the input parameters set for the source during the system simulation test, which are referenced based on the output characteristics of the TENG. The TENG model utilizes an existing voltage source series capacitor model to simulate its real-world behavior. Specifically, the voltage signal is set as an AC signal with a peak-to-peak value of 600 V, an inherent capacitance of 2 nF, and a signal frequency of 1 Hz. These parameters are designed to accurately reflect the operating characteristics of the TENG, ensuring the reliability of the simulation results.

The simulation primarily focuses on analyzing and validating the performance of the Buck circuit and the hysteresis comparator circuit. Figure S4 shows the voltage variation during the buck conversion process with different C_{in}. The input capacitor values tested are 0.1 nF, 0.22 nF, 0.47 nF, 1 nF, and 10 nF, selected to analyze the effect of capacitance on voltage regulation. The results indicate that the choice of different capacitor values significantly impacts the stability of the output voltage and the charging speed.

Figure S5 further details the impact of capacitance and inductance on the output voltage during the simulation. Figure S5(a) shows the charging voltage variation over the same time period for an C_{out} of 1 mF under different C_{in}. Figure S5(b) illustrates the charging voltage of C_{out} (still 1 mF) under varying inductance values during the same charging time. Through the buck conversion, the TENG signal is converted from high voltage and low current to low voltage and high current, which significantly improves the system's energy transfer efficiency.

The timing diagram of the hysteresis comparator module is shown in Figure S6. In this part of the simulation, 10 mF output capacitor C_{out} is selected to effectively power the subsequent circuits. The hysteresis circuit's turn-on voltage is set to 5 V, with a reference voltage V_{ref} of 2.5 V. During the operation of the buck module, energy is transferred from C_{in} to C_{out}, causing the voltage V_{out} across C_{out} to gradually increase over time. Due to the influence of the voltage divider resistors, the voltage at the non-inverting terminal V_+ remains lower than V_{ref} during the charging process. As V_{ref} rises with the increase in V_{out}, it stabilizes once it reaches the set reference voltage of 2.5 V.

To verify the system's load response, a 1 K resistor and a 47 μF capacitor in parallel were used as a simulated load. The power loss caused by resistors in the hysteresis circuit and the current variation at the load are shown in Figure S7. Figure S7(a) displays the current flowing through the resistive load, while Figure S7(b) shows the significant surge current generated by the capacitive load at the initial power-up. To better illustrate the difference between the two, Figure S7(c) presents the magnified waveforms of both currents. Figure S7(d) shows the current loss through resistors R_1, R_2, and R_3, further verifying the energy management performance of the circuit design.

Supplementary Note 4. Component Selection Explanation.

Figure S23 illustrates the passive components used in the circuit: (a) tantalum capacitor, (b) ceramic capacitor, (c) aluminum electrolytic capacitor, (d) metal film resistor, (e) freewheeling diode, and (f) drum core inductor.

In the Universal Self-Triggered Passive Output Power Management Strategy (USPT-PMS), the input capacitor Cin is a ceramic capacitor. Since the signal from the TENG after the rectifier is a high-voltage signal, and to match the inherent capacitance of the TENG, a small-capacity, high-voltage ceramic capacitor is chosen. According to the derating guidelines, the ceramic capacitor should have a voltage rating of at least 2 kV to ensure safety and stability.

Tantalum capacitors are used in USTP-PMS due to their low equivalent series resistance (ESR), high stability, and excellent frequency characteristics, making them ideal for filtering applications. Therefore, a tantalum capacitor is selected for C_{ref}, with a common voltage rating of 16 V. The value of C_{ref} is selected based on the following considerations: since R_3 and C_{ref} form a series circuit, the voltage on V_{ref} is affected by the time constant τ. Therefore, C_{ref} should not be too large, while still providing sufficient filtering to ensure stable V_{ref} output. The capacitance value is selected to be 1 μF.

To store more energy for powering the rear-end load, the output capacitor C_{out} requires a high capacitance value. Aluminum electrolytic capacitors are an effective choice for large capacitance. Since the supply voltage to the load is relatively low, a 16 V-rated electrolytic capacitor is chosen for C_{out}.

Metal film resistors are commonly used in circuit designs related to triboelectricity. Resistors with at least MΩ-level resistance should be selected to minimize potential current losses. However, special attention must be paid when designing R_3; while a higher R_3 can reduce current loss, it can also increase the rise time of V_{ref}, affecting system responsiveness. Similarly, excessively high R_1 and R_2 values can impact the turn-on voltage of the hysteresis module.

Comparator Selection: A low-power comparator is required to minimize the impact on input energy. In this study, the comparator used is the MCP6541, with a maximum quiescent current of 1μA. Other low-power comparators can also be used in USPT-PMS, such as the LTC1540 (quiescent current of 300 nA) and the TLV3491 (quiescent current of 1.2 μA).

Similarly, the reference voltage source must offer precision while maintaining low power consumption. The reference voltage source used in this study is the MAX6006, which provides a 1.25 V reference voltage (this reference is particularly suitable for applications with space constraints and low power requirements, with a minimum operating current of less than 1 μA). For higher reference voltages, MAX6007, MAX6008, and MAX6009 can be used, offering outputs of 2.048 V, 2.5 V, and 3 V, respectively. Some comparators, like the LTC1540, have built-in reference sources and can directly provide the reference voltage. Additionally, external power sources can also serve as reference sources, and due to the very high input impedance of the inverting terminal of the comparator (up to TΩ), the resulting power loss is negligible.

Supplementary Note 5. Layout of circuit.

In the circuit layout of USTP-PMS, attention should be paid to the accuracy of analog circuits. In order to reduce the noise interference of the input power supply and ensure that the comparator can work stably and reliably, a ceramic capacitor is added to the power pin of the comparator (between the power supply terminal and the ground) for filtering, which is used to filter out high-frequency noise and prevent the fluctuation of the front-end input voltage from interfering with the comparator, thereby avoiding the occurrence of false triggering of the comparator judgment.

In addition to adding filter capacitors to the power pins, ceramic capacitors are also added on the load side. This capacitor is mainly used to further reduce power supply noise and ground bounce (ground voltage changes caused by power supply current fluctuations).

In addition to selecting appropriate filter capacitors, the lead lengths of the input and output terminals should be shortened as much as possible. Long leads will introduce additional parasitic inductance and capacitance, which may cause unnecessary parasitic feedback around the comparator and interfere with the normal operation of the comparator.

Supplementary Note 6. Formula calculation.

Buck module

The current through the inductor at the instant the switch is turned on is equal to the sum of the output current i_L from the TENG source i_o and the current i_{in} through the input capacitor C_{in}.

$$i_L(t) = i_{in}(t) + i_o(t) \tag{1}$$

Voltage across the inductor:

$$V_L(t) = L\frac{di_L(t)}{dt} = V_{in}(t) - V_{out}(t) \tag{2}$$

Current through the inductor:

$$i_L(t) = \frac{C_o C_{in}}{C_o + C_{in}}\frac{dV_{in}(t)}{dt} \tag{3}$$

When the switch is off, neglecting the diode forward voltage drop, the relationship between the inductor current and the output voltage is as follows:

$$i_L(t) = -i_{out}(t) + i_R(t) \tag{4}$$

$$V_L(t) = L\frac{di_L(t)}{dt} = -V_{out}(t) \tag{5}$$

Hysteresis module

i_R is the total current flowing into the subsequent hysteresis circuit.

The output voltage of the hysteresis module is as follows. which includes:

$$i_R(t) = i_{R_3}(t) + i_{R_1+R_2}(t) + i_c(t) \tag{6}$$

Among them, i_{R_3} is the current in the voltage divider reference source branch, $i_{R_1+R_2}$ is the current in the voltage divider resistor branch, and i_c is the input current of the comparator. When the voltage does not reach the limit set by the voltage divider reference source, the reference voltage V_{ref} is:

$$V_{ref}(t) = V_{out}(t) - i_{R_3}(t)R_3 \tag{7}$$

When V_{ref} reaches its maximum value, the voltage across R_3 both ends are as follows:

$$V_{R_3}(t) = V_{out}(t) - V_{ref}(t) \tag{8}$$

Non-inverting input voltage V_+:

$$V_+(t) = \left[V_{out}(t) - V_L(t)\right] \times \frac{R_2}{R_1 + R_2} \tag{9}$$

Among them, V_L is the voltage across the load.

When condition $V_+ < V_{ref}$ is met, the comparator outputs low level signal, denoted as V_{LL}.

$$V_L(t)=V_{LL}(t) \tag{10}$$

When condition $V_+ > V_{ref}$ is met, the comparator outputs high level signal, denoted as V_{LH}.

$$V_L(t)=V_{LH}(t) \tag{11}$$

Performance calculation

The output power calculation of the TENG is shown in Figure S19. After passing through the rectifier bridge, the current flowing through the load is measured, with the average current I_{rms}:

$$I_{rms}(t)=\sqrt{\frac{\int_{t_1}^{t_2} I^2 d(t)}{t_2-t_1}} \tag{12}$$

Average power P_{rms}**:**

$$P_{rms}(t)=I_{rms}{}^2(t)\times R=\frac{R\times\int_{t_1}^{t_2} I^2 d(t)}{t_2-t_1} \tag{13}$$

The output power calculation of the TENG connected to the PMS is shown in Figure S20. Figure S20(a) presents the test circuit diagram, which omits the front-end buck circuit section following the rectification of the TENG. Considering the range limitations of the 6514 Electrometer, as shown in Figure S20 (b), the average voltage V_{rms} across the resistive load is:

$$V_{rms}(t)=\sqrt{\frac{\int_{t_1'}^{t_2'} V^2 d(t)}{t_2'-t_1'}} \tag{14}$$

Average power P'_{rms} :

$$P'_{rms}(t)=\frac{V_{rms}{}^2(t)}{R}=\frac{\int_{t_1'}^{t_2'} V^2 d(t)}{(t_2'-t_1')\times R} \tag{15}$$

Load end loss calculation

The test load is a commercial wireless temperature and humidity sensor, with the specific physical image shown in Supplementary Fig. 22. Without using the hysteresis module, the buck circuit is employed for voltage step-down and current boosting. After connecting the load, as shown in Fig. 4b (ii) and (iii), the load current gradually stabilizes after 13 s. At this point, the voltage across the load V_L equals the voltage across the output capacitor V_{out}.

$$V_L(t)=V_{out}(t) \tag{16}$$

V_{L}=1.3 V**,** the current flowing through the load is I_{L}, Since the operating voltage of the load has not been reached, the current flowing through the load at this time can be considered as a loss current I_{loss},

$$I_{\mathrm{L}}(t)=I_{\mathrm{loss}}(t) \tag{17}$$

I_{loss}=3.8 mA, the loss is represented as P_{loss}:

$$P_{\mathrm{loss}}(t)=V_{\mathrm{L}}(t)\times I_{\mathrm{loss}}(t)=4.94\ \mathrm{mW} \tag{18}$$

Since the output signal gradually increases and fluctuates, the calculated loss represents the maximum loss.

After connecting the USTP-PMS, the comparator outputs a low-level voltage V'_{LL} :

$$V'_{\mathrm{L}}(t)=V'_{\mathrm{LL}}(t) \tag{19}$$

$$V'_{\mathrm{L}}(t)=0 \tag{20}$$

At this point, the loss caused by the load is negligible. However, the addition of the hysteresis module introduces additional loss. The voltage across the resistor V_{R_3} is**:**

$$V_{R_3}(t)=V_{\mathrm{out}}(t)-V_{\mathrm{ref}}(t) \tag{21}$$

The voltage across the series-connected resistors R_1 and R_2 is $V_{R_1+R_2}$:

$$V_{R_1+R_2}(t)=V_{\mathrm{out}}(t)-V'_{\mathrm{L}}(t) \tag{22}$$

$$V_{R_1+R_2}(t)=V_{\mathrm{out}}(t) \tag{23}$$

The power supply voltage V_{DD} of the comparator is the same as the output voltage V_{out}:

$$V_{\mathrm{DD}}(t)=V_{\mathrm{out}}(t) \tag{24}$$

When the voltage V_{out} is set to 3.3 V and the hysteresis circuit is conducting, the maximum loss, across resistor R_1, R_2, R_3 is:

$$P_{R_1+R_2}(t)=\frac{V^2_{\mathrm{out}}(t)}{R_1+R_2}=0.825\ \mu\mathrm{W} \tag{25}$$

$$P_{R_3}(t)=\frac{V^2_{R_3}(t)}{R_3}=\frac{\left[V_{\mathrm{out}}(t)-V_{\mathrm{ref}}(t)\right]^2}{R_3}=2.1\ \mu\mathrm{W} \tag{26}$$

where is $R_1=8.2\ \mathrm{M\Omega}$, $R_2=5\ \mathrm{M\Omega}$, $R_3=2\ \mathrm{M\Omega}$, $V_{\mathrm{ref}}=1.25\ \mathrm{V}$.

The loss generated by the reference voltage source is P_{ref}:

$$P_{\text{ref}}(t) = V_{\text{ref}}(t) \times I_{\text{ref}}(t) = 1.25\ \mu\text{W} \tag{27}$$

Where I_{ref} is the current flowing through the reference voltage source, the maximum current for the MAX6006 shunt reference voltage source is $1\ \mu\text{A}$.

The loss generated by the comparator is:

$$P_{\text{o}}(t) = V_{\text{out}}(t) \times I_{\text{o}}(t) = 3.3\ \mu\text{W} \tag{28}$$

where the quiescent current of the MCP6541 comparator is $1\ \mu\text{A}$.

Therefore, the loss after adding the hysteresis module is P'_{loss}:

$$P'_{\text{loss}}(t) = P_{R_1+R_2}(t) + P_{R_3}(t) + P_{\text{ref}}(t) + P_{\text{o}}(t) = 7.475\ \mu\text{W} \tag{29}$$

Supplementary Table 1. Abbreviations and meanings appearing in the paper.

Order	Full title	Abbreviation
1	Triboelectric nanogenerator	TENG
2	Universal self-triggered passive output power management strategy	USPT-PMS
3	Vertical contact-separation mode triboelectric nanogenerator	CS-TENG
4	Freestanding mode triboelectric nanogenerator	FS-TENG
5	Output capacitor	C_{out}
6	Input capacitor	C_{in}
7	Parasitic capacitance in the load	C_p
8	Output capacitor terminal voltage	V_{out}
9	Low level output	V_{OL}
10	High level output	V_{OH}
11	Inherent capacitance	C_o
12	Freewheeling diode	D_5
13	Non-inverting terminal	V_+
14	Reference voltage	V_{ref}
15	Load terminal voltage	V_L
16	Loss current	I_{loss}
17	Inrush current	I_{ir}
18	Load current	I_L
19	High level output	V_{LH}
20	Low level output	V_{LL}