Supplementary Information

Colour neutral photovoltaic windows with performance linearly tuneable with transmittance

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Colour rendering index and electrical performance data

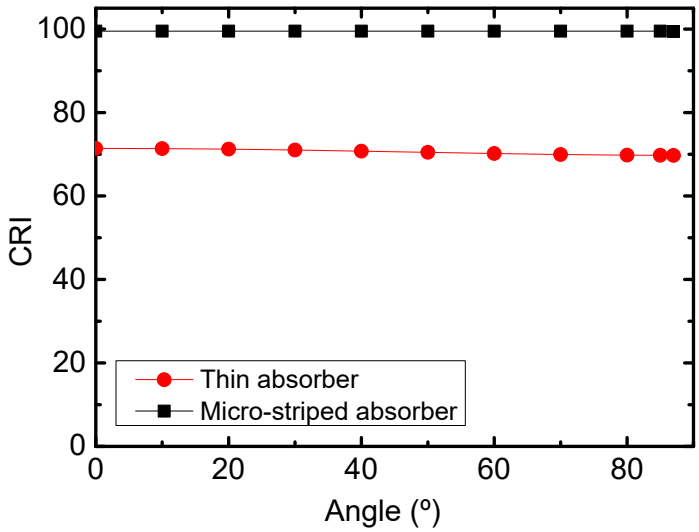

Figure S1. Comparison of CRI as a function of the sunlight's incident angle to the STPV for thin-absorber and micro-striped CIGSe STPV devices.

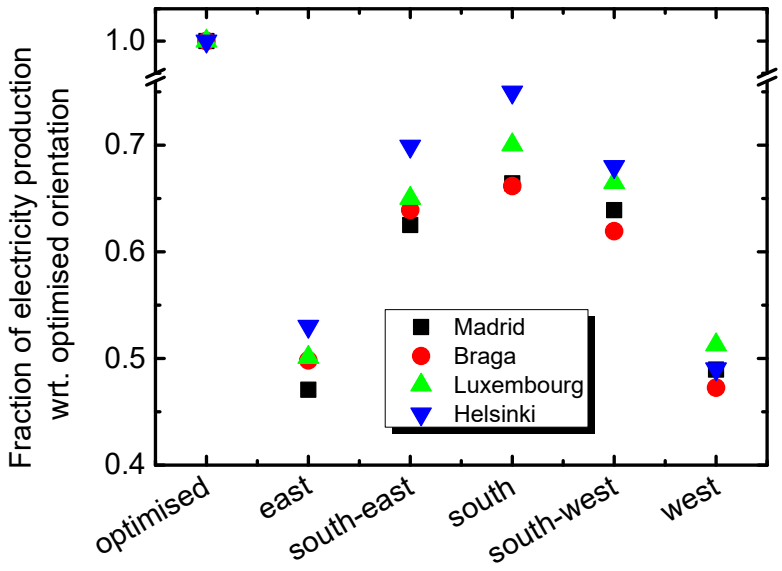

Figure S2. Fraction of yearly electricity production for vertically-mounted STPV systems facing east to west with respect to a system with optimised orientation, considered for four locations. In southern Europe (Madrid and Braga), a south-facing window PV system delivers only 66% of that with optimised orientation, in northern Europe (Helsinki), this fraction increases to 75%.

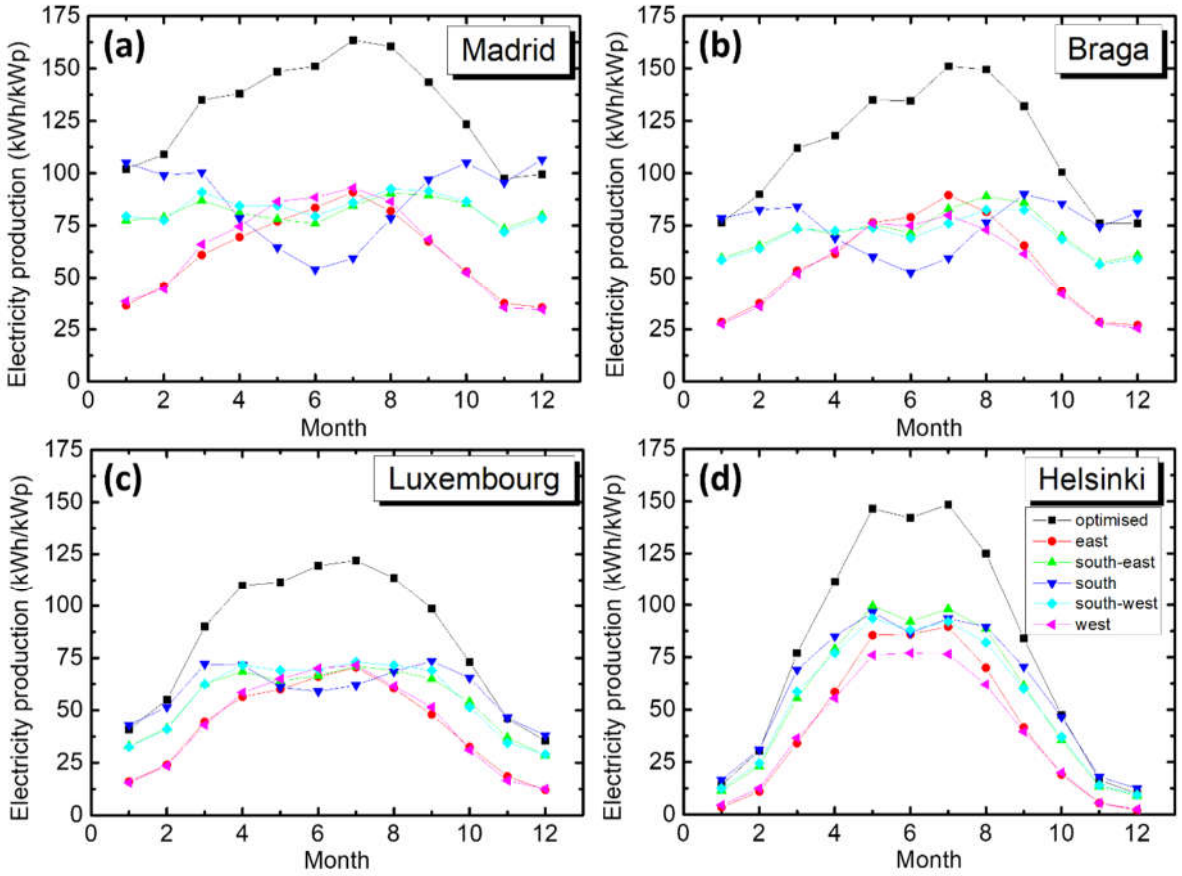

Figure S3. Monthly electricity production for PV systems installed in (a) Madrid (ES), (b) Braga (PT), (c) Luxembourg (LX), and (d) Helsinki (FI). Black squares represent a standard PV system with optimised orientation and coloured symbols a vertical window installation with different orientations ranging from east to west, according to the legend in panel (d).

Simulation and optimisation of current collection in STPV devices

Solar cell stripe model

The micro-striped semi-transparent photovoltaic (STPV) devices comprise a glass substrate (soda lime glass), with Cu(In,Ga)Se_2 solar cell stripes in parallel to one another and bare substrate between them. Perpendicular to the cell stripes at either end of the device are the back and front contacts with metal top contact "grid fingers" running the length of each stripe (Fig. S4). These grid fingers are wider at the front grid and get narrower towards the back contact, ending before reaching the back contact. The simulation followed the workflow shown in Fig. S5. We modelled each element as a single-diode solar cell. We discretised the simulation domain and modelled each discrete element as a single-diode solar cell with three additional lumped series resistances. These resistances represent three lateral current pathways: (i) through the ZnO:Al window layer parallel to the grid, (ii) through the ZnO:Al window layer toward the metal grid, and (iii) through the Ni/Al grid fingers. We did this to facilitate optimisation of current collection by varying them. The equivalent electrical circuit diagram of the solar cell stripe and the metal grid finger is shown in Fig. S4c, with I1, D1, R1, R5 being the current source, diode, shunt resistance and series resistance through the junction of the solar cell. R3 (Mo), R2 and R6 (ZnO:Al) are the lumped resistances, whilst R4 is the metal grid finger resistance. Because of symmetry (see Fig. S4), we only considered half of a single cell stripe and adjacent transparent gap and discretised it into tiny elements.

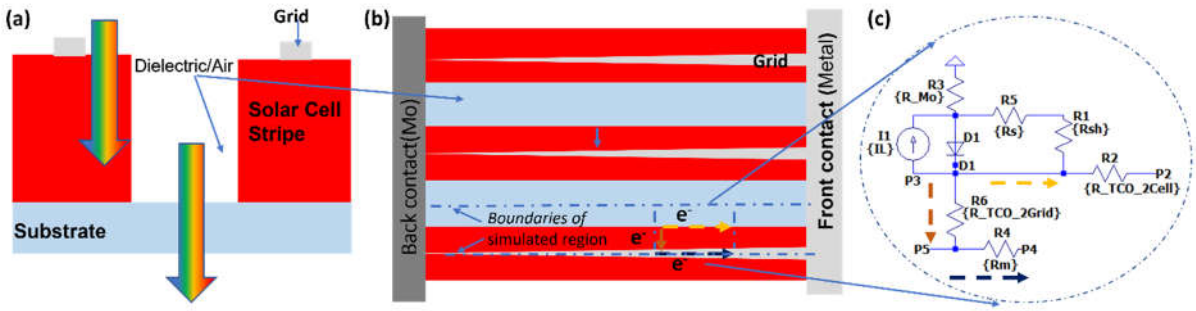

Figure S4. (a) Side and (b) top view of the STPV device design. The back contact is made of Mo, the solar cell stripe comprises Mo/CIGSe/CdS/i-ZnO/ZnO:Al whilst the grid fingers and top metal contact are made from Ni/Al. (c) Equivalent electrical circuit diagram of the metal stripe and grid finger, where I1, D1, R1, R5 are the current source, diode, shunt resistance and series resistance through the junction of the solar cell. R3 (Mo), R2 and R6 (ZnO:Al) are the lumped resistances, whilst R4 is the metal grid finger resistance.

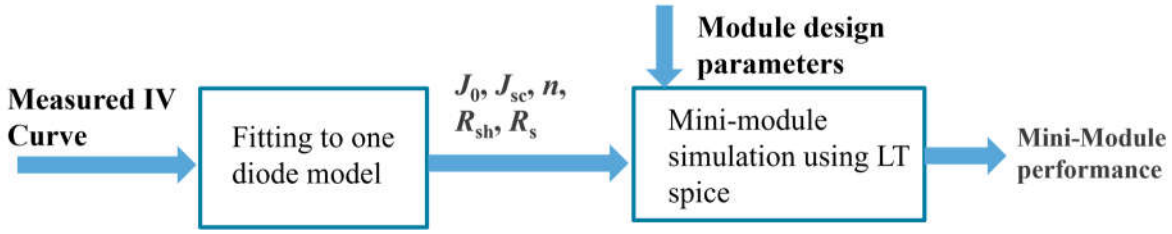

Figure S5. Workflow for the STPV device simulations.

Input parameters

The source of most of the input parameters is given in the main manuscript. The value of the lumped resistances discussed in the previous paragraph was obtained in the following way: the experimental current-voltage curve from our median 0.5 cm^2 reference solar cell (Table S1) was fitted with a one-diode model[1]. Then we constructed a 2D LTSpice model of the reference device using those parameters, except for the series resistance. The series resistance of the reference solar cell was assumed to have two components, one from lateral transport in the window layer (since there were no metal grid lines), and the other from the rest of the layers that constitute the solar cell. The second part of the series resistance was varied until the resulting current-voltage curve from the simulation matched that of the reference device. The series resistance of the lateral transport in the window layer and the rest of the device were found to be 0.17 and 0.27 Ω cm^2, respectively, similar to those reported in literature[2].

We calculated the first part of the series resistance from the sheet resistance of the TCO window layer. When we divide the transparent conductive oxide into N segments along the current-flow direction, the equivalent series resistance of each segment (R_{eq}) results from lateral transport in a layer with sheet resistance R_s (Ω/□) and is given by[3]:

$$R_{eq} = \frac{2N^2}{(N+1)(2N+1)} R_s \qquad \text{Eq. (S1)}$$

Table S1. Experimental reference cell parameters taken from the median 0.5 cm^2 area device of eight devices.

PCE_{TIA} (%)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF	J_0 (A/cm^2)	R_s (Ω cm^2)	R_{sh} (Ω cm^2)	n
17.1	32.1	697	0.76	1.5×10^{-9}	0.44	1943	1.57

STPV device simulation and optimisation

The series resistance for simulating the cell stripe profile for different STPV devices used the lumped diode model discussed above. We used these inputs along with device parameters to carry out the device simulations in LTSpice[4]. We generated the input netlists for Spice using the Python *PyLTSpice* library[5]. All the data processing and visualisation was done using Origin.

To maximise device efficiency η, we optimised by balancing improvements in short-circuit current density (J_{sc}) against fill factor (FF) losses caused by wider grid fingers. Because the efficiency landscape contains multiple local maxima, we used a genetic algorithm implemented with the Python library *Pygad*[6]. After calculating the optimum current-voltage characteristics of the half-stripe model, we reconstructed the electrical performance parameters and average visible transmittance (AVT) properties of the complete STPV device by applying symmetry. Figure S6 shows the impact of variation of a tapered Ni/Al grid finger dimensions on a 1000 µm-wide micro-striped STPV device and the simulated impact of grid width parameters on J_{sc}, FF, and PCE_{TIA}, with V_{oc} being constant at ~691 mV.

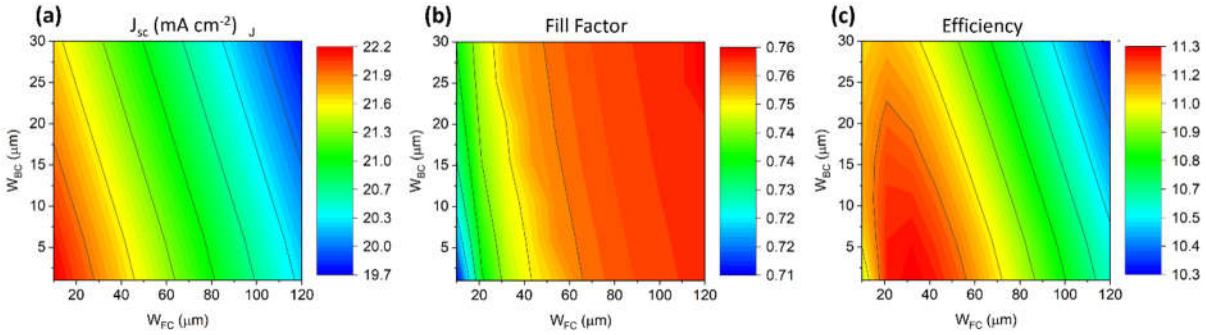

Figure S6. Optimisation of 2 µm high grid finger geometry for 1000 µm wide micro-striped STPV device with 30% AVT. (a) J_{sc}, (b) FF, and (c) PCE_{TIA} as a function of grid width parameters using the reference cell data of Table S1. The V_{oc} of all stripes is similar with an average value of (691 ± 3) mV.

Preliminary experiments

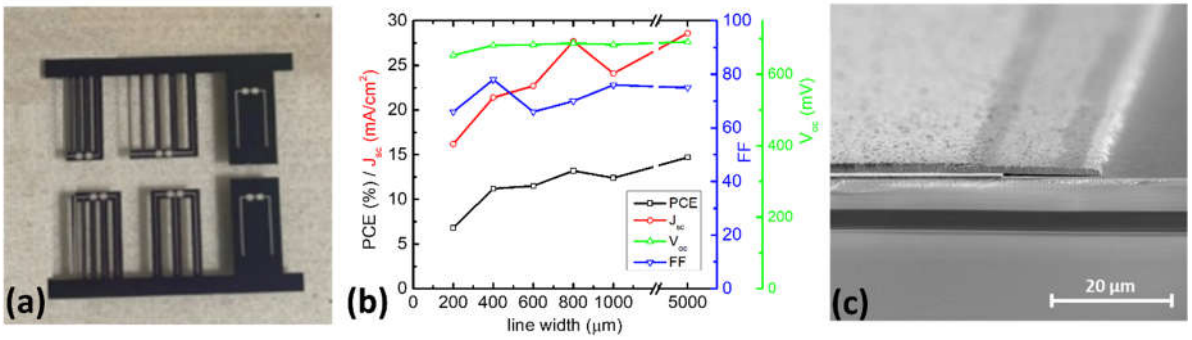

Figure S7. Test structures to assess the fabrication process. (a) Photo of test structure with stripes of between 200 and 1000 µm width and 0.8 cm length fabricated with the process illustrated in Fig. 7 of the main manuscript. Two additional standard-sized cell areas (0.5 cm^2) were added as reference structures. (b) Solar cell parameters extracted from JV analysis, showing that the J_{sc} increases with larger solar cell widths, where the power conversion efficiency here is for the solar cell collection area, PCE_{SCA}. (c) Scanning electron microscopy image of a solar cell edge revealing damage to the ZnO:Al window layer; thus, current collection is unlikely there. As the solar cells get narrower, the relative damaged-to-undamaged area increases, thus decreasing the J_{sc}. The complete findings of this study are published elsewhere [2].

Measurement and calculation of areas related to the experimental STPV devices by confocal microscopy

To measure the different types of areas of the devices, we used a confocal laser scanning microscope (CLSM, Keyence VK-X1000) equipped with a UV laser (404 nm) and Nikon lenses with magnifications of 5X, 20X and 150X. Multiple images, and respective height maps, are measured along the length of the stripes, both from the front and the back side of the device. For reference, a side view schematic of the layers that make up a CIGSe device is shown in Fig. S8a. An example front side coloured microscopy image of a 400 µm stripe just below the front contact is shown in Fig. S8b, and a back side view in Fig. S8d. Ideally all the layers in the stack would have the same width, and a uniform colour would be expected across the stripe viewing from the back side, and similarly on the front side except at the centre for the grid line. Although the back side view (Fig. S8d) clearly shows the stripe to have a single colour which we identify to be the Mo layer, the front side view (Fig. S8b) shows the stripe having differently coloured areas which we identify from left to right as glass, Mo, CIGSe (absorber), window (i:ZnO/Al:ZnO) and grid. The CdS layer is very thin and cannot be distinguished by the confocal microscope; therefore, it is not discussed further. The height profile across the solar cell stripe (Fig. S8c) allows to interpret that the etchant laterally attacks the layers under the lithographic mask, reducing the window layer area the most, and the Mo area the least. In the case of Mo, the measurements from the back side allow to cross-check the measurements from the front side and estimate the degree of lateral etching.

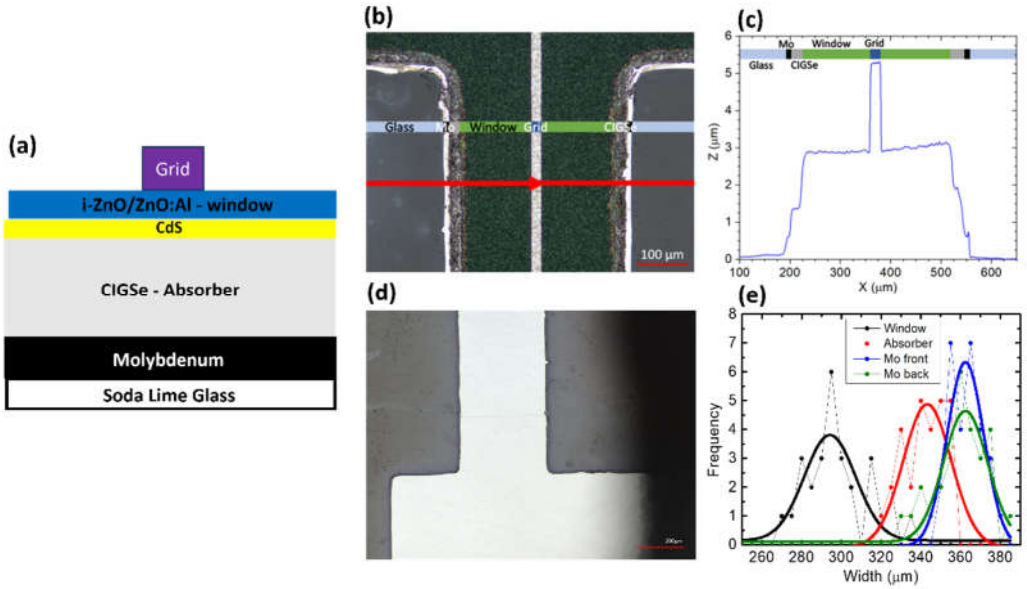

Figure S8. (a) Schematic of the layers that comprise a CIGSe device stack. (b) Confocal microscope optical image of the front side of a 400 µm stripe where areas at different vertical heights are coloured coded to help visualize the distinct layers of the stack. (c) Average line profile taken along the red solid line shown in (b). (d) Confocal microscope optical image from the back side of the same strip as in (b). (e) Width distribution of window, absorber (CIGSe) and Mo layers along the length of the solar cell stripe. The thick solid lines are simple Gauss fits to these distributions.

Averaging along the length of the 400 μm stripe, the width distribution for each layer is plotted in Fig. S8e. This confirms that, on average, the width of the window layer is the smallest whereas the Mo layer is the widest. These differences in layer widths have an impact on the detailed analysis of the devices' electrical and optical properties, i.e. the width of the Mo determines the aperture area ratio, while the width of the window layer determines the current collection area, as shown schematically in Fig. S9.

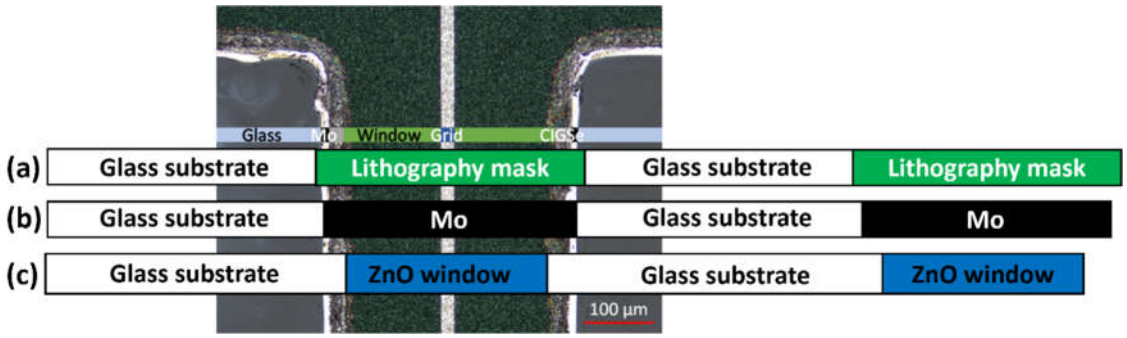

Figure S9. Schematic of the different types of areas in the micro-striped STPV devices that can be defined as seen from the front view. Two solar cell stripes are schematically illustrated with two empty substrate areas. Underneath one of the stripes is the front view image of a stripe repeated from Fig. S8 for reference. (a) The lithographic mask width defines the nominal aperture area, (b) the Mo layer width defines the measured solar cell stripe aperture area, and (c) the window layer is the smallest layer and defines the electrical current collection area.

The total area of the device is considered to be the width defined as from the outside edge of the first stripe on the left, to the outside edge of the last stripe on the right, multiplied by the length of the stripe. The area of the solar cell next to the busbars is less than one percent of the solar cell striped area and can be safely ignored. The aperture area ratio is defined as the area of the transparent substrate divided by the total substrate area and is expressed as a percentage. We define two different types of aperture area ratio – nominal and measured. The nominal aperture area ratio is calculated from the lithographic mask width (Fig. S9a). However, some horizontal etching resulted in narrower stripes than expected. The measured solar cell stripe aperture area ratio is then given by the Mo width (Fig. S9b). The current collection area is defined by the width of the remaining window layer (Fig. S9c). We summarise in Table S2 the different apertures and current collection areas for all the micro-striped solar cell configurations.

Table S2. Average single stripe areas and aperture area ratios calculated for the different micro-striped solar cell configurations.

	50AA400S	**50AA1000S**	**70AA400S**	**30AA400S**
Nominal stripe width (μm)	400	1000	400	400
Nominal single stripe area (cm^2)	0.096	0.240	0.096	0.096
Current collection area (cm^2)	0.071 ± 0.005	0.226 ± 0.007	0.068 ± 0.004	0.072 ± 0.006
Solar cell stripe area (cm^2)	0.087 ± 0.006	0.235 ± 0.007	0.084 ± 0.005	0.087 ± 0.005
Percentage of solar cell stripe area collecting current (%)	82	96	81	83
Nominal STPV device aperture area ratio (%)	50	50	70	30
Measured STPV device aperture area ratio (%)	56 ± 2	52 ± 2	74 ± 3	36 ± 1

Optical microscopy evidence for broken grid lines

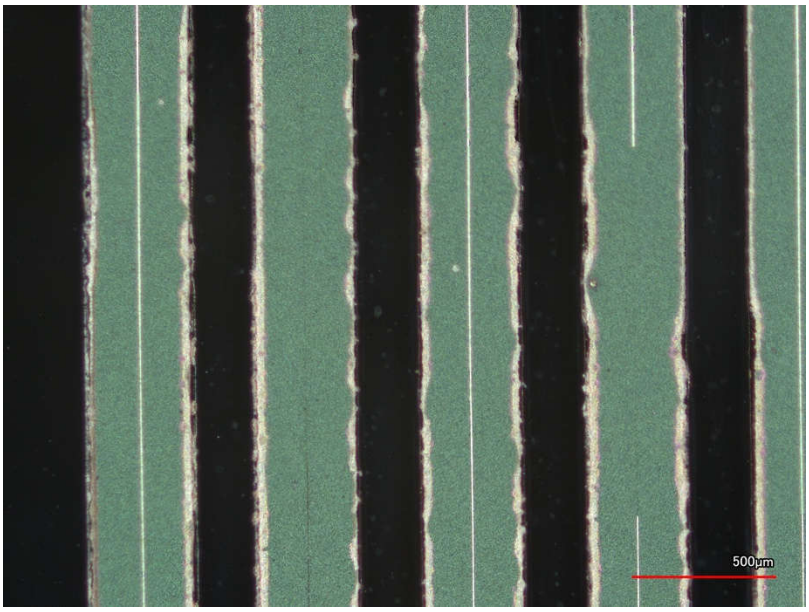

Figure S10. Optical microscope image of sample 30AA400S showing the partial absence of grid lines on the second and fourth solar cell stripes from the left. These interruptions in the grid line likely explain the reduced fill factor of this device compared to all other STPV devices. The absence of the grid line means that the current can only flow through the window layer in these parts. Since the window layer has a higher resistance compared to the grid line, the fill factor reduces.

Uncertainty of the transmission measurements

The transmission measurements were taken with a beam spot size of 5 mm × 3 mm (the maximum in our equipment). Each sample was measured three times, moving the sample to a random position in the beam each time. Fig. S11a shows the average of the three measurements as a continuous line, and the highest and lowest measurements as dotted lines. For the 30AA400S sample with the smallest transparent spaces between the stripes the data lie on top of one another. Contrarily, for 70AA400S which has wider transparent spacing, and the 50AA1000S, with wider stripes, there is some variance in the data. Since the gaps/stripes are 19-20% of the beam diameter, this variance cannot be avoided easily.
Although the average transmission for the 50AA1000S and 50AA400S are close, the measurement uncertainty for 50AA1000S is larger. Fig. S11b and c illustrate the measurement uncertainty. The blue rectangles indicate the solar cell stripes with the transparent gaps (white) in between. The beam spot is illustrated in orange. For the 50AA1000S sample, with nominally 1000 µm wide stripes and 1000 µm wide gaps, the maximum transmission that might be measured is T_{max} = 60% and the minimum is T_{min} = 40%. For the narrower lines and gaps, these values are lower, with 52% and 48%, meaning that the reliability of the obtained average value of three measurements is higher.

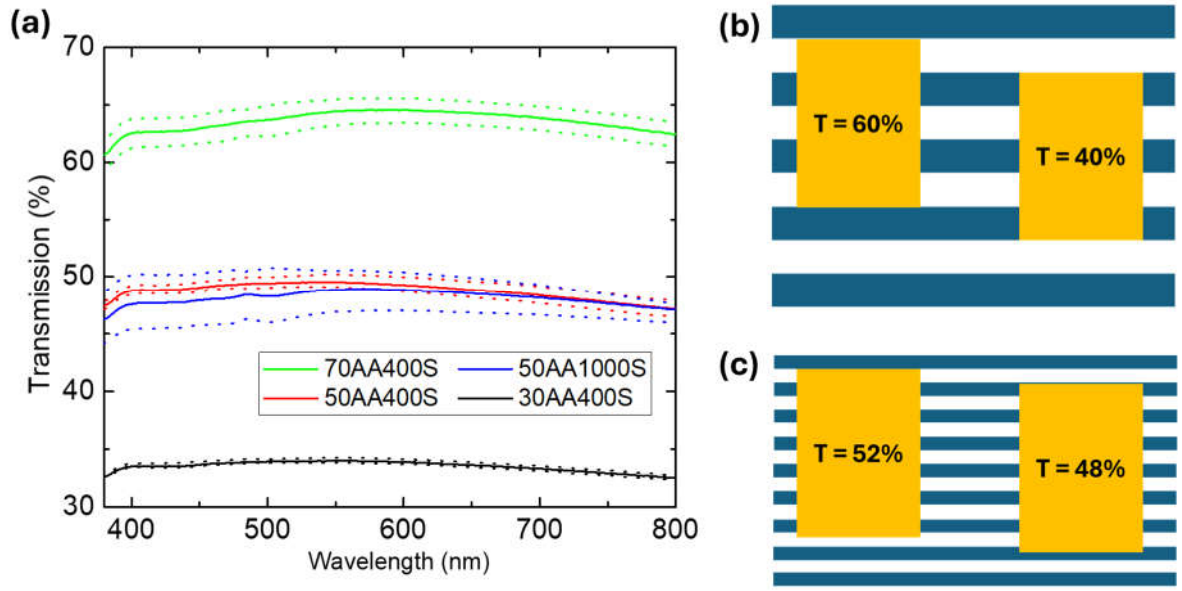

Figure S11. (a) Transmission of the micro-striped STPV devices (solid lines) calculated from the average of three measurements (the maximum and minimum transmission curves are shown as dotted lines. (b-c) Depending on the width of the solar cell stripes, the obtained transmission can vary more or less strong, depending on where the random positioning of the beam spot hits the solar cell stripes. This affects the uncertainty and reliability of the measured transmission values.

Literature references used for comparison of optical and electrical performance

Table S3. Comparison of average visual transmission (AVT), colour rendering index (CRI), total illuminated area power conversion efficiency (PCE_{TIA}), light utilization efficiency (LUE), and CIELAB colour coordinates for different CIGSe STPV devices from the literature. The AVT, CRI, and colour coordinates were calculated by digitizing the transmission curves from the respective references and then using them with the spreadsheet from[7]. The website[8] was used to convert the colour coordinates into RGB values to colour the data points of Figures 5f, g and h in the main manuscript.

Technology Type	AVT (%)	CRI	PCE_{TIA} (%)	LUE (%)	L*	a*	b*	Reference
Continuous thin film CIGSe	3.6	65.0	4.0	0.14	22.1	5.1	11.1	[9]
	4.0	54.0	11.6	0.46	23.5	9.0	16.5	[10]
	7.5	32.4	9.8	0.73	32.4	15.2	46.2	[11]
	8.2	37.0	10.6	0.87	34.0	13.0	40.8	[12]
	11.6	39.2	9.0	1.04	37.7	11.3	51.1	[13]
	12.7	42.6	9.0	1.14	41.1	10.2	55.2	[13]
	17.7	50.0	6.5	1.15	48.8	9.7	52	[11]
	18.8	52.8	6.5	1.22	50.1	8.7	48.8	[12]
	25.5	56.5	5.9	1.51	49.5	8.4	44.8	[14]
	35.1	67.9	4.9	1.72	65.6	4.0	39.8	[12]
	50.3	75.3	2.8	1.41	76.0	7.3	36.4	[12]
	56.3	79.3	1.7	0.96	79.6	0.6	39.5	[12]
Segmented CIGSe	18	90	9.4*	1.69	49.5	-0.1	11.2	[15]

* Note that the PCE for the segmented CIGSe [15] is stated for a series-interconnected mini-module, which suffers from reduction in PCE related to the dead area of the series interconnect. Therefore, a direct comparison with the PCE of solar cells (without interconnect) is not possible. Ref [16] also takes a segmented approach on the millimeter scale but unfortunately could not be included since the transmission data were not published.

Comparison of high CRI photovoltaic technologies

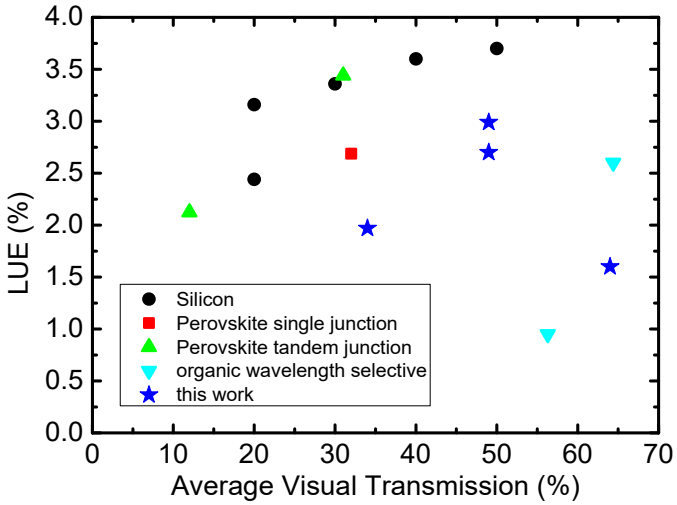

Figure S12. Literature comparison of different neutral view technologies. Light utilization efficiencies (LUE) as a function of average visual transmission (AVT) for devices that show a colour rendering index above 95, i.e. colour neutral. All devices selectively transmit light through openings except for the continuous thin film organic devices which selectively allow visible light to pass. The silicon device openings are fabricated through a combination of photolithography and deep reactive ion etching. The perovskite openings are made by linearly laser scribing the material away inside of a glovebox. The data for the figure can be found in Table S4.

Table S4. A comparison of AVT, PCE_{TIA}, and LUE for different colour neutral semi-transparent solar cells reported in the literature.

Technology Type	AVT (%)	PCE_{TIA} (%)	LUE (%)	Reference
Silicon	50	7.4	3.7	[17]
	40	9	3.6	[17]
	30	11.2	3.4	[17]
	20	12.2	2.4	[17]
	20	15.8	3.2	[18]
Perovskite single junction	32	8.4	2.7	[19]
Perovskite tandem junction	12	17.7	2.1	[19]
	31	11.1	3.4	[19]
Organic wavelength selective	56.3	1.7	0.95	[20]
	64.4	4.0	2.6	[20]

Theoretical considerations for making larger STPV device sizes

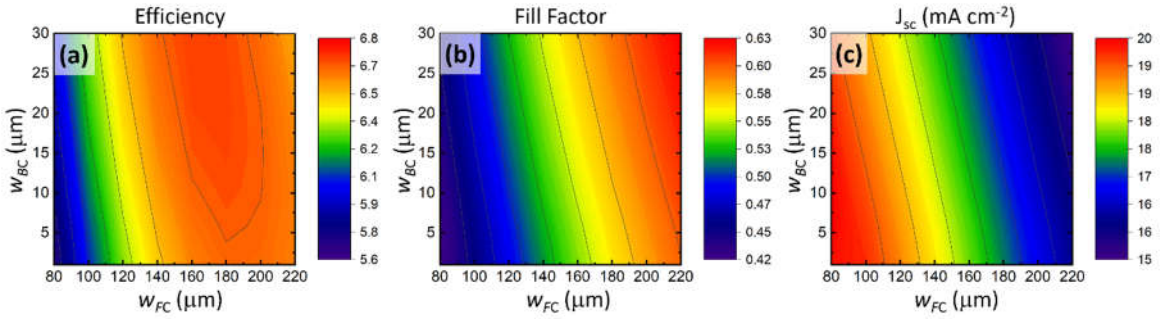

Figure S13. Calculated JV parameters for a STPV device with 400 µm wide and 25 cm long solar cell stripes with 2 µm thick tapered grid lines with variation of width at the front contact, w_{FC}, and near the back contact, w_{BC}: (a) PCE_{TIA}, (b) fill factor, and (c) short-circuit current.

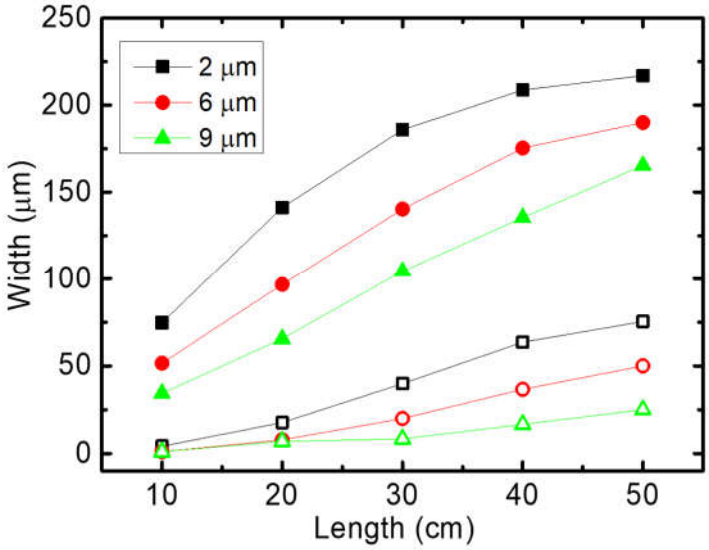

Figure S14. Optimised widths of the tapered grid fingers at the front (FC, solid symbols) and near the back contact (BC, open symbols) for grid lines with three different thicknesses (legend) for 400 µm wide solar cell micro-stripes of between 10 and 50 cm length. These optimised grid finger geometries were used for the simulation of the STPV performance shown in Fig. 6 of the main manuscript.

Method for assessing performance of continuous and segmented thin-film STPV

Calculation of power conversion efficiency (PCE_{TIA}) and average visual transmittance (AVT)

As a starting point for comparing continuous thin film absorber layers and segmented micro-striped Cu(In,Ga)Se_2 (CIGSe) device concepts for STPV, the initial properties of the continuous full thickness devices are reported here and were taken from reference[21].

Table S5. CIGSe device performance of the solar cell whose properties were used as the basis to compare the power conversion efficiency total illuminated area (PCE_{TIA}) and AVT of continuous and segmented STPV devices.

PCE_{TIA} (%)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)
21.7	36.6	746	0.79

To calculate the PCE_{TIA} and AVT for CIGSe continuous thin film devices under AM1.5G illumination we used the transfer matrix method [22,23]. The workflow is shown in Fig. S14 with the device stack and the references to the wavelength dependent optical properties given in Table S6.

The total number of photons absorbed at each wavelength in the CIGSe absorber layer was summed to determine the electron-hole pair generation. The J_{sc} was calculated assuming a 90% charge collection efficiency. The PCE_{TIA} was then determined by multiplying the calculated J_{sc} with the V_{oc} and FF values provided in Table S5. The AVT was calculated as Eq. (S2)[7].

$$AVT = \frac{\int T(\lambda)\cdot V(\lambda)\cdot AM1.5G(\lambda)d\lambda}{\int V(\lambda)\cdot AM1.5G(\lambda)d\lambda} \qquad \text{Eq. (S2)}$$

where $T(\lambda)$ is the transmission spectrum of the light passing through the solar cell and $V(\lambda)$ is the photopic response.[7]

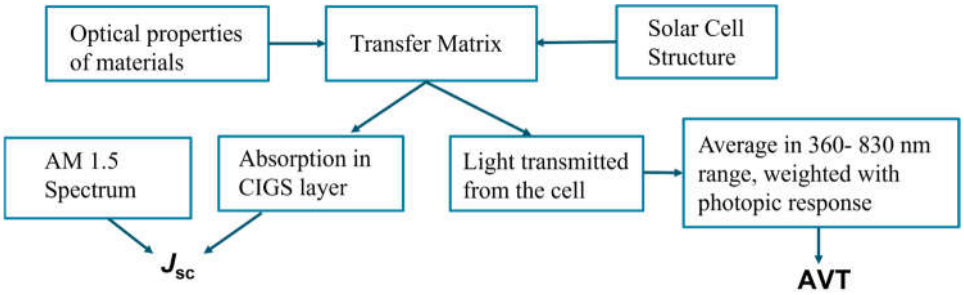

Fig. S15. Workflow to calculate the PCE_{TIA} and AVT for different thickness CIGSe absorbers.

Table S6. Device stack, material thicknesses, and references to the optical data used.

Material	Thickness (nm)	Optical data reference
MgF_2	110	[24]
ZnO:Al	170	[25]
i-ZnO	90	[26]
CdS	50	[25]
CIGSe	Variable	[27]
$In:SnO_2$	90	[23]

The colour of the light coming through both continuous film and segmented micro-striped devices was calculated from converting the transmission spectra into L* a* b* colour coordinates using the methodology from[7] and then converting these to RGB values using[8].

Method for electrical energy yield calculation for segmented micro-striped STPV

All calculations were run using the Joint Research Center's (JRC) Photovoltaic Geographical Information System (PVGIS).[28] PVGIS utilizes satellite-based and ground-measured data to estimate solar radiation levels, including global horizontal irradiation (GHI) and direct normal irradiation (DNI) for various locations. It then uses this irradiance data with simple models like one-diode models and nominal operating cell temperature (NOCT) models to calculate module performance parameters for given orientations.

Calculations were carried out for four locations in Europe: Madrid (Spain), Braga (Portugal), Luxembourg, and Helsinki (Finland). For the energy yield calculation, a CIGSe solar cell system was simulated using the PVGIS-SARAH2 solar radiation database with a module power of 0.2 kWp. This value corresponds to a regular 1 m^2 module with 20% efficiency, or a STPV module with 50% AVT of 2 m^2. The monthly and annual electricity production were extracted and normalised to the installed kWp, to facilitate comparison of opaque and semi-transparent PV modules. Note that the area required to obtain the same nominal installed capacity scales with the AVT as $(1\text{-AVT})^{-1}$. STPV windows were considered vertically mounted with different orientations, ranging from East to West. For comparison, a fixed-mounted system with optimal orientation was also calculated.

References

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5 N. Brum, PyLTSpice (version 5.2) https://github.com/nunobrum/PyLTSpice.
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