Supplementary Information

Active-Matrix Digital Microfluidic Device Based on Surfactant-Mediated Electro-Dewetting

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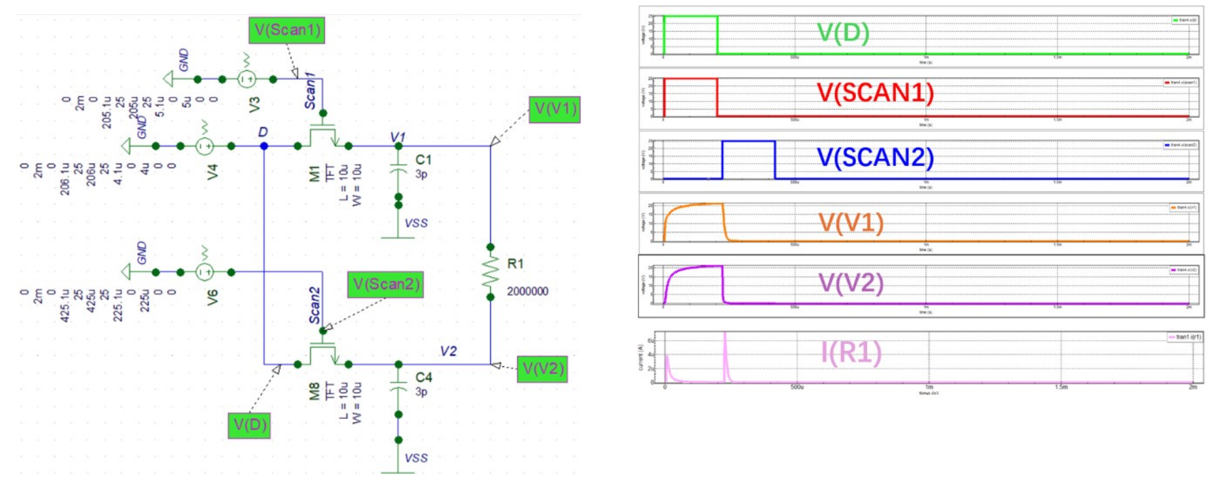
1. 1T1C configuration simulation for electro-dewetting

The simulation of node potentials during switching in a 1T1C configuration for a 2×1 AM electro-dewetting application is illustrated in Figs. S1A (schematic) and S1B (resulting waveform). In the electro-dewetting DMF device, which lacks a dielectric layer, the adjacent electrodes are connected through the droplet, represented as resistor R1 in Fig. S1A. The voltages at the electrodes of two cells are denoted as V(V1) and V(V2).

Fig. S1B shows the simulation results during AM operation. To set the upper electrode voltage V(V1) to "HIGH", a "HIGH" data voltage V(D) is applied to upper electrode when the first scan signal V(Scan1) goes "HIGH". Because upper electrode and lower electrode are connected through R1 (the droplet), this also causes the V(V2) signal to rise. Next, to set the lower electrode voltage V(V2) to "LOW", a "LOW" data voltage V(D) is applied to lower electrode when the second scan signal V(Scan2) is activated. Since 2 electrodes remain connected through R1, the V(V1) signal also drops to zero.

As a result, the capacitor of traditional 1T1C cell circuit has difficulty effectively storing charges in the electro-dewetting process. Consequently, the current I(R1) flowing through resistor R1 (the droplet) during the 1T1C AM operation cannot be maintained in electro-dewetting.



A **B**

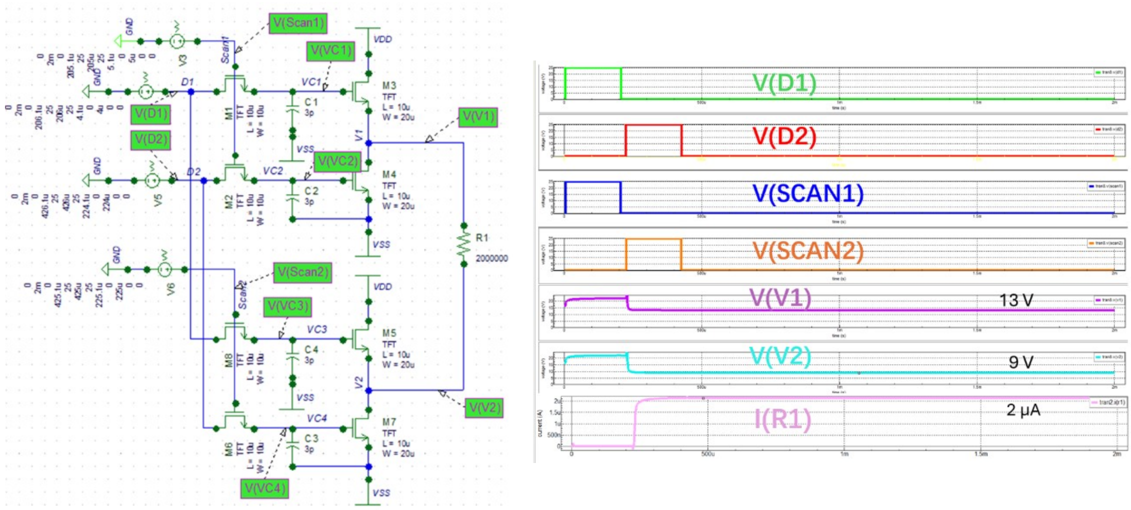
Fig. S1 The conventional 1T1C configuration for a 2×1 AM electro-dewetting application A) schematic and B) the simulation result.

2. 4T2C configuration simulation for electro-dewetting

The simulation of node potentials and the current across the droplet in a 4T2C configuration for a 2×1 AM electro-dewetting application is illustrated in Fig. S2A (schematic) and Fig. S2B (resulting waveform), where resistor R1 represents the droplet. In Fig. S2A, the voltages at the electrodes of two cells are denoted as V(V1) and V(V2).

Fig. S2B presents the simulation results during AM operation. To set the upper electrode voltage V(V1) to “HIGH”, the first scan signal V(Scan1) is activated. At this point, the “HIGH” data voltage V(D1) is stored in capacitor C1 as V(VC1), while the “LOW” data voltage V(D2) is stored in capacitor C2 as V(VC2). The voltage V(VC1) at capacitor C1 turns on the TFT M3, while the voltage V(VC2) at capacitor C2 turns off transistor M4. Consequently, upper electrode is connected to VDD through M3, causing the V(V1) signal to rise. With transistor M7 turned off, the lower electrode is connected to VDD through the resistor (representing the droplet) and M3, which also results in the V(V2) signal turning “HIGH”.

To set the lower electrode voltage V(V2) to “LOW”, the second scan signal V(Scan2) is activated. During this process, the “LOW” data voltage V(D1) is stored in capacitor C3 as V(VC3), and the “HIGH” data voltage V(D2) is stored in capacitor C4 as V(VC4). The voltage V(VC3) at capacitor C3 turns off TFT M5, while the voltage V(VC4) at capacitor C4 turns on transistor M7. This configuration allows V(V1) to decrease to 13 V and V(V2) to drop to 9 V, thereby sustaining the current I(R1) across the resistor (the droplet).



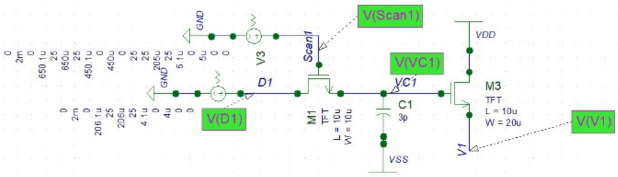
A **B**

Fig. S2 The conventional 4T2C configuration for a 2×1 AM electro-dewetting application A) schematic and B) the simulation result.

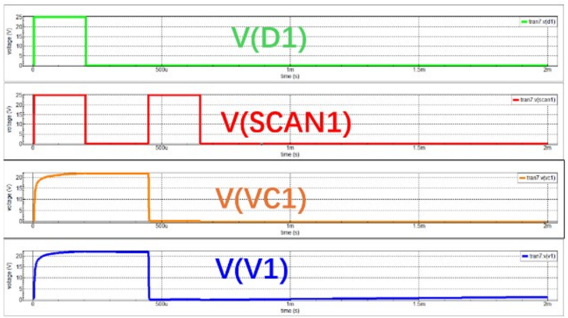
3. 2T1C configuration simulation for capacitor charging and discharging time

Figs. S3A and S3B illustrate the 2T1C configuration for simulation and the resulting switching waveform, respectively. The discharging time of the 3-pF capacitor from 20 V to 0 V is significantly faster, at approximately 5 μs, while the charging time to increase from 0 V to 20 V is about 47 μs. To ensure adequate charging, the pulse width of the scan signal was set to 200 μs, which exceeds the minimum required width of 50 μs.

The 3-pF capacitor offers sufficient charge storage capacity, maintaining stable gate voltages for the ITZO driving TFT, with a gate current of approximately 1 pA during operation. This configuration enables the capacitor to retain the necessary charge to sustain the gate voltage over time without significant droop. As a result, the voltage V(V1) at the electrode effectively tracks the charging and discharging of V(VC1), ensuring reliable actuation.



A



B

Fig. S3 A) The 2T1C configuration and B) the switching simulation result.