Supplementary Information (SI) for Materials Horizons.

Supporting Information

Bioelectronics Building Block: Low-Voltage Integratable Organic Thin-Film Transistors with a Tri-layer Gate Dielectric Design

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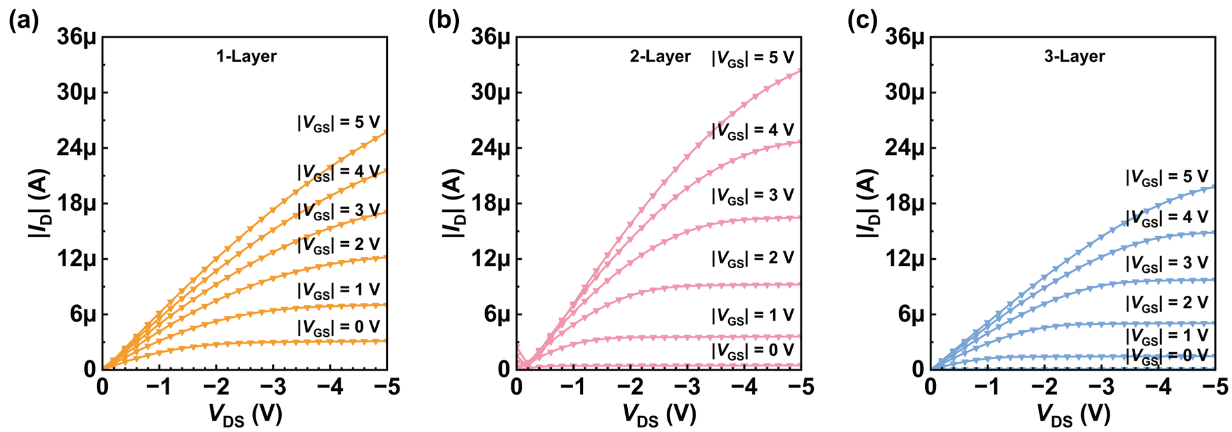

Fig S1 Measured output characteristics of OTFTs with different gate dielectric configurations: (a) mono-layer, (b) bi-layer, and (c) tri-layer designs.

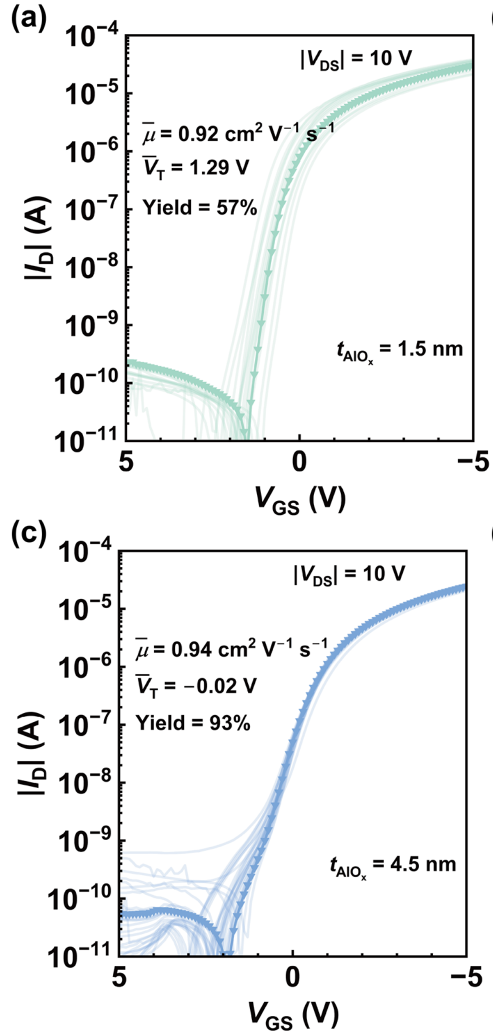

Fig S2 Measured transfer characteristics of functional OTFTs with the tri-layer dielectric design, illustrating variations in AlO_x thickness: (a) 1.5 nm, (b) 3.0 nm, (c) 4.5 nm, and (d) 6.0 nm. All devices have a width-to-length ratio of 1500 μm / 50 μm.

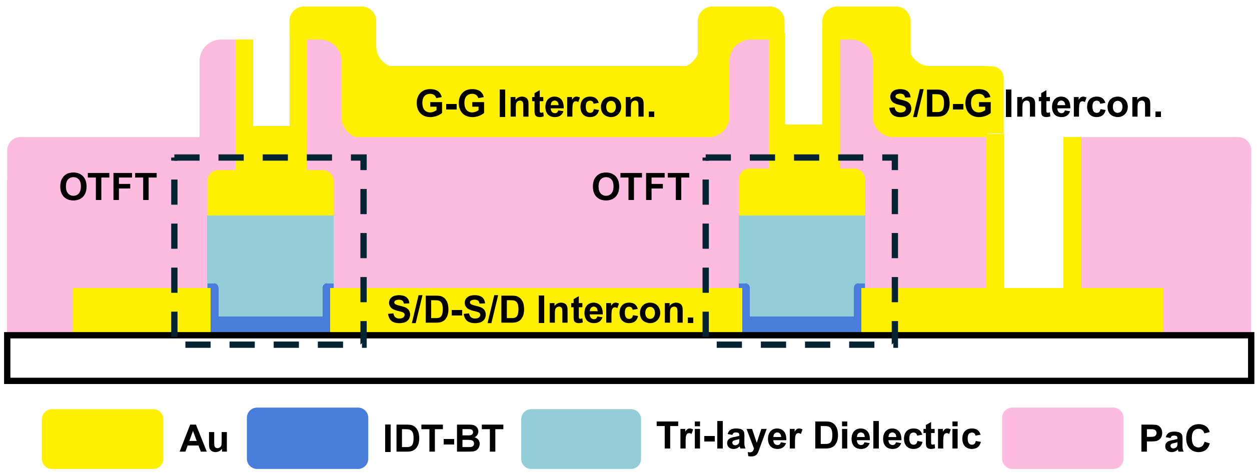

Figure S3 Cross-sectional schematic of the integration of different metal layers for OTFTs into circuits. Intercon.: interconnection; PaC: parylene-C.

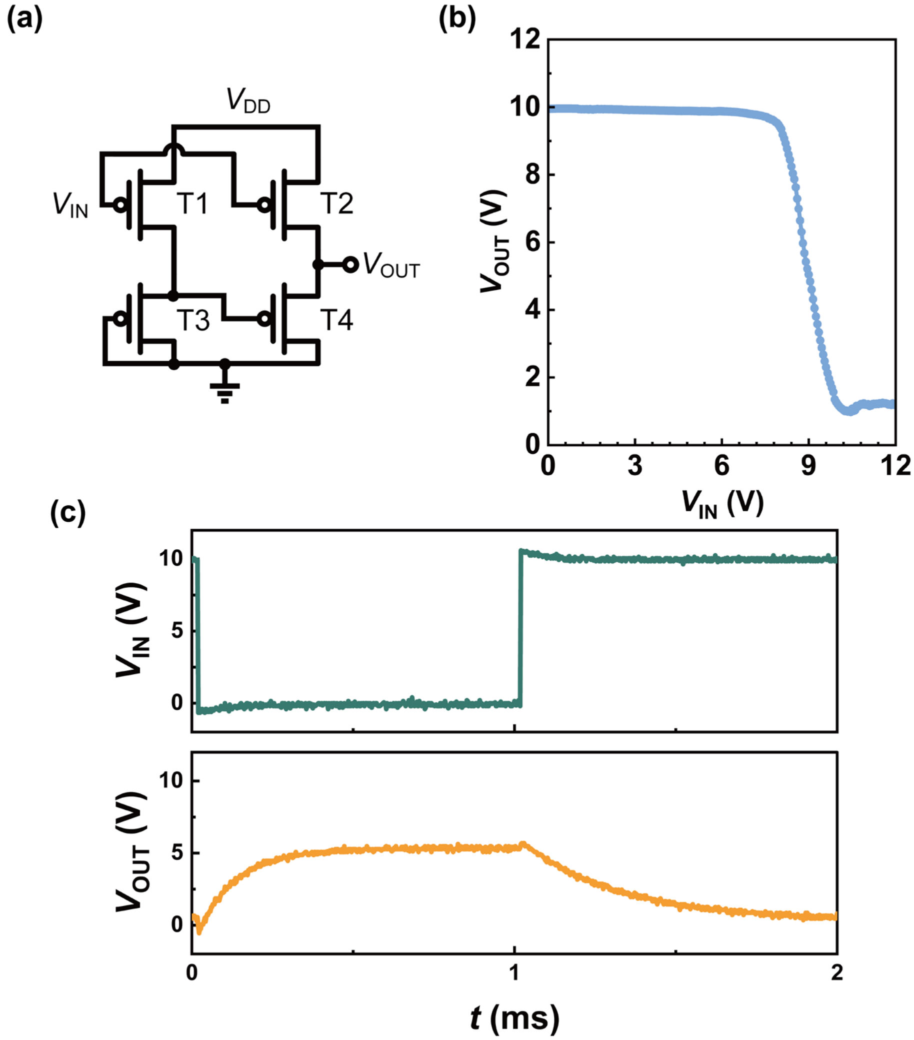

Figure S4 (a) Circuit schematic of the p-type pseudo-CMOS inverter. (b) Measured output voltage (V_{OUT}) as a function of input voltage (V_{IN}) for a supply voltage (V_{DD}) of 10 V. (c) Dynamic response of the inverter.

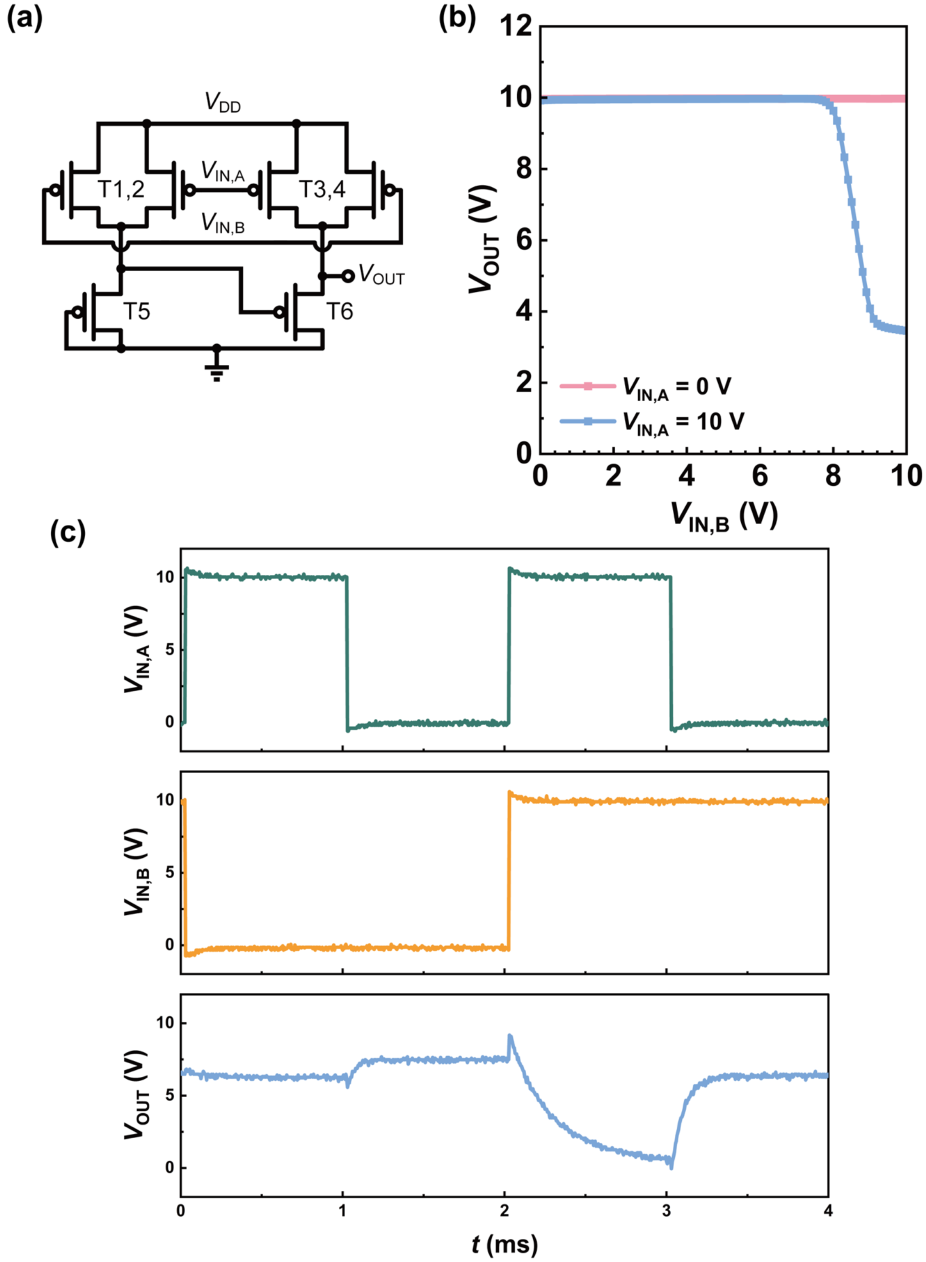

Figure S5 (a) Circuit schematic of the NAND gate with a p-type pseudo-CMOS design. (b) Measured output voltage (V_{OUT}) as a function of input voltages ($V_{IN,A}$ and $V_{IN,B}$) for a supply voltage (V_{DD}) of 10 V. (c) Dynamic response of the NAND gate.

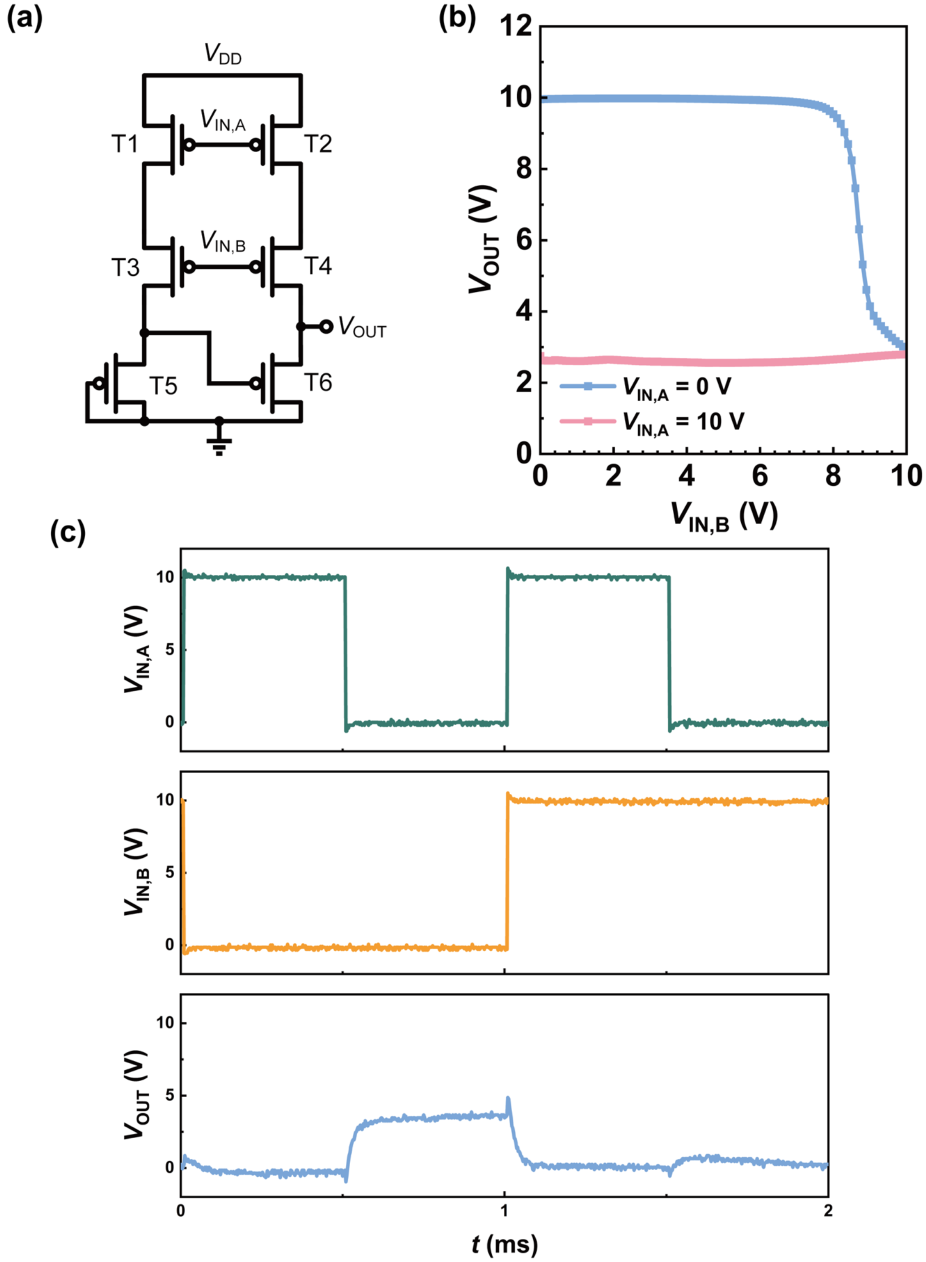

Figure S6 (a) Circuit schematic of the NOR gate with a p-type pseudo-CMOS design. (b) Measured output voltage (V_{OUT}) as a function of input voltages ($V_{IN,A}$ and $V_{IN,B}$) for a supply voltage (V_{DD}) of 10 V. (c) Dynamic response of the NOR gate.

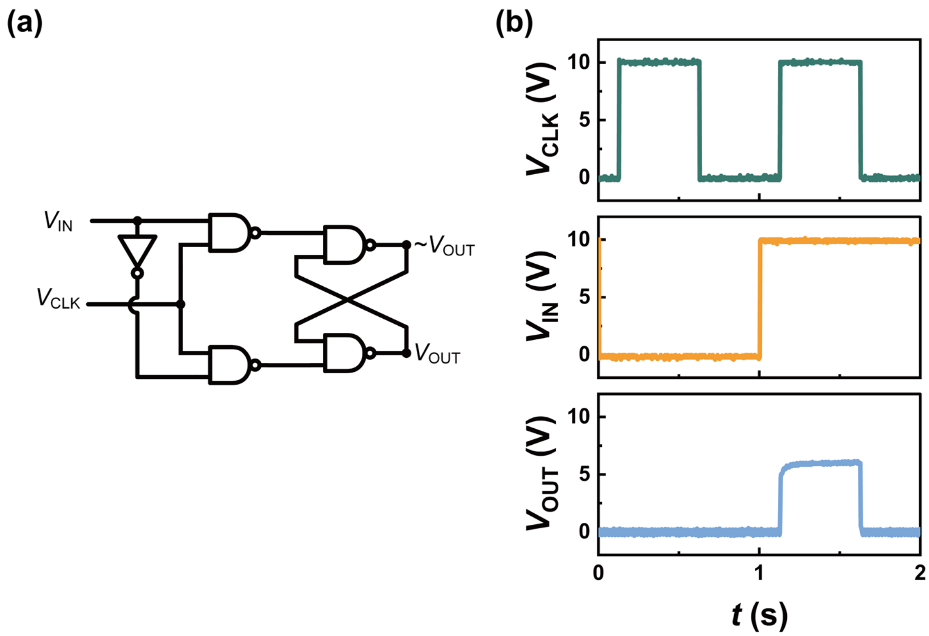

Figure S7 (a) Circuit schematic of the D flip-flop with a p-type pseudo-CMOS design. (b) Dynamic response of the D flip-flop.

Dielectric Type	1-Layer	2-Layer	3-Layer	3-Layer	3-Layer	3-Layer
t_{AlOx} (nm)	/	/	1.5	3.0	4.5	6.0
C_i (nF/cm^2)	154	90	84	83	81	80
Mobility ($cm^2V^{-1}s^{-1}$)	0.23 (0.01)	0.94 (0.15)	0.92 (0.13)	0.93 (0.13)	0.94 (0.07)	0.92 (0.12)
V_T (V)	2.29 (0.33)	0.73 (0.21)	1.29 (0.52)	−0.40 (0.01)	−0.02 (0.06)	−0.20 (0.21)
ON/OFF	10^3~10^4	10^3~10^4	10^5~10^6	10^5~10^6	10^5~10^6	10^5~10^6
Yield	47%	37%	50%	57%	93%	90%

Table S1 Summary of the electrical performance of OTFTs across 30 devices for each gate dielectric configuration.

	Dielectric	$\|V_{DS}\|$ (V)	Mobility ($cm^2V^{-1}s^{-1}$)	V_T (V)	Processing Method	Integrated Circuits
This work	CYTOP/AlO_x /P(VDF-TrFE-CFE)	10	0.94	−0.02	Photolithography	2-inch Array Logic Gates
[1]	CYTOP/Parylene	10	1.18	−3.07	Printing	AND Gate
[2]	PS/Parylene	25	0.47	−3.7	Printing	/
[3]	SiO_2	1	0.0035	~1	Printing	Inverter
[4]	CYTOP	60	1.5	-3	Shadow Mask	/
[5]	PMMA	60	0.25	−5.67	Shadow Mask	/
[6]	PMMA /P(VDF-TrFE-CFE)	5	0.62	~−1	Shadow Mask	/
[7]	CYTOP /P(VDF-TrFE-CFE)	5	1.5	−1.52	Shadow Mask	/

Table S2 Comparison of electrical performance between the presented OTFTs and previously reported IDT-BT-based TFTs.

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