

### **S1 Reversible micro AND gate propagation**

A micro-scale AND gate is connected to two 90 degree input bistable elements and one output bistable element. The bistable memory bit are preloaded, then the logic operation of the AND is demonstrated. The logic gate is reversible, as the inputs are changed from one back to zero, thus changing the output gate.

### **S2 Demonstrating reversible bistable memory bit propagation**

Real time signal propagation from input to output in a 10 element chain. Slow-motion highlights the signal transitioning between each bistable element. Demonstrates reversibility of the full chain by actuating the input from '1' back to '0'. Shows how reversibility is different than back-drivability because the full chain does not reverse when the output is actuated.

### **S3 Macro memory bit actuation and signal propagation**

Actuation of a macro-scale bistable element. The close-up shows the operation of the motion stage, cross-pivot flexures, and coupling linkage. The 10 element chain shows the primary transition wave travel from left to right. The secondary vibrations do not affect the bistable state of the elements. The red dots were used to collect experimental data on the propagation dynamics.

### **S4 Micro memory bit actuation and signal propagation**

The micro bistable element chain is fabricated using two photon lithography. First, each element in the chain is preloaded by applying a transverse displacement and locking in place with a ratchet lock mechanism, to engage the bistable behavior. The transition wave is then propagated through the chain. Reversibility is demonstrated by consecutively propagating the signal, reversing, and propagating again.

### **S5 Macro AND gate propagation**

A macro AND gate propagates a signal through a chain of bistable elements connected to the input and output of the and gate. The first input is pre-actuated and held at the 1 position, the second input is actuated sending the transition wave propagating through three input bistable elements, through the AND gate, and out through an impedance matched output chain.