Supplementary information (SI) for

A Thermally Engineered NbO_x Memristor with $CdTe_2$ Interlayers for High-Accuracy ECG Arrhythmia Detection

Yunlai Zhu [a], Chaotong Xie [a], Zhongren Ye [a], Tao Jiang [a], Yong Zhang [a], Ke Wang [a], Xiaoling Wu [a], Haotian Tang [a], Junjie Zhang [a],Yang Hu [a], Ying Zhu [a], Zhe Feng [a*], Zuyu Xu [a], Lihua Xu [a], Wendong Lu [a], Zuheng Wu [a*], Yuehua Dai [a*]

[a] School of Integrated Circuits, Anhui University, Hefei, Anhui, 230601, China.

Corresponding Authors

*E-mail: zack@ahu.edu.cn (Z. Feng), wuzuheng@ahu.edu.cn (Z.-H. Wu), daiyuehua@ahu.edu.cn (Y.-H. Dai)

Supplementary Note 1: Rationale for Selecting 2D $CdTe_2$ as the Interlayer Material

The selection of two-dimensional (2D) cadmium telluride ($CdTe_2$) as the interlayer material is supported by several key material properties documented in the literature. First, $CdTe_2$ exhibits excellent thermodynamic stability under operational conditions, with theoretical studies confirming its structural integrity up to 900 K[1]—significantly exceeding the Poole-Frenkel (P-F) transition temperature of 390 K relevant for device operation. Regarding electronic properties, 2D materials typically exhibit carrier concentrations in the range of 10^{12}-10^{13} cm^{-2}.[2-6] N-type 2D $CdTe_2$ specifically demonstrates carrier concentrations within this range,[7] supporting an electrical conductivity value of approximately 5×10^3 S/m used in our simulations. Furthermore, the material exhibits an ultralow in-plane lattice thermal conductivity of 0.33 W/(m·K) at 300 K, which aligns with reported values.[7] Furthermore, this thermal conductivity demonstrates a negative temperature coefficient, decreasing further with rising temperature. This combination of low thermal conductivity and temperature-dependent behavior makes $CdTe_2$ particularly effective for thermal confinement in threshold-switching devices. Moreover, from a fabrication standpoint,

the complete device structure can be realized via sputtering and lift-off processes,[8-10] with the 2D $CdTe_2$ interlayer material can be fabricated through methods such as electrodeposition combined with Chemical vapor deposition (CVD).[11-13] Collectively, these properties establish $CdTe_2$ as a highly suitable thermal management interlayer for threshold-switching memristors.

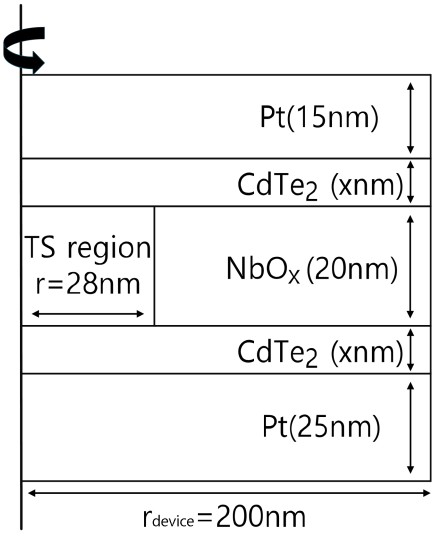

FIG.S1 Geometric schematic diagram of the memristor model in COMSOL Multiphysics simulations.

Based on the models reported in previous studies,[14-17] in order to make the model match the experimental data, as shown in **Figure S2**, the radius and thickness of the NbO_x-TSM conductive filament were set to 28 nm and 20 nm respectively.

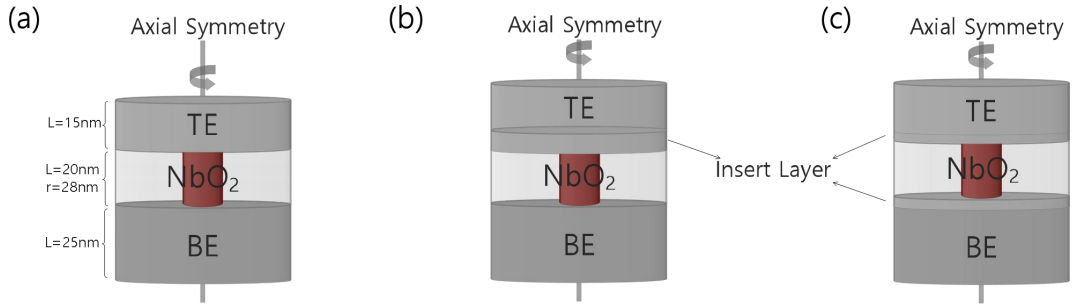

FIG.S2 2D axisymmetric simulation models of NbO_x-TSM. (a) N-IL device. (b) S-IL (10 nm) device. (c) D-IL (5 nm + 5 nm) device.

Utilizing the finite-element model, we simulated the threshold switching (TS) dynamics of the NbO_x-TSM by applying a nanosecond-scale voltage pulse. As shown in **Figure S3(a)**, at a temperature of T_{amb} = 301 K, the switching transient was captured effectively. **Figure S3(b)** demonstrates that the TS time for the N-IL TSM is approximately 2 ns, which agrees well with experimentally reported values.[18] Meanwhile, **Figure S3(c)** reveals that the D-IL TSM exhibits a slightly longer but still ultrafast TS time of approximately 5 ns. These results confirm that the incorporation of an interlayer structure successfully reduces both the threshold voltage and threshold current while maintaining an extremely fast switching speed—a critical combination for high-performance neuromorphic applications.

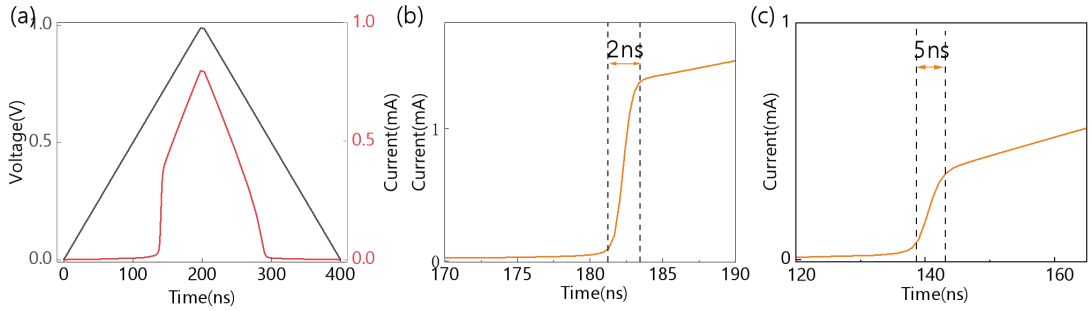

FIG.S3 (a) A pulse voltage of 400 ns and 1 V was applied to NbO_x-TSMs. (b) TS time of the N-IL device. (c) TS time of the D-IL device.

To account for experimental non-idealities such as thermal fluctuations and oxygen redistribution—known to cause threshold voltage variations[19, 20] —we incorporate a stochastic term into the thermal dynamics. The governing equation is:

$$\frac{dT}{dt} = \frac{i_m \cdot v_m}{C_{th}} - \frac{T\text{-}T_{amb}}{R_{th} \cdot C_{th}} + T\left(\frac{k_b}{C_{th}}\right)^{\frac{1}{2}} \frac{4\pi}{R_{th}C_{th}} cos\left[\frac{2\pi t}{R_{th}C_{th}}\right]$$

This modified model introduces a thermal noise component to simulate intrinsic fluctuations. We implemented this model in LTspice to emulate device behavior under realistic conditions. As shown in **Figure S4**, the LTspice model was first calibrated against experimental DC sweep data. Subsequently, the system was simulated under the influence of thermal noise for 500 switching cycles to extract the threshold voltage V_{th} distribution. The resulting V_{th} distributions for the N-IL and D-IL devices, shown in **Figures S4(b)**, **(c)**, and **(d)**. The N-IL device has a mean V_{th} of 0.834 V with a standard deviation of 0.015 V, while the D-IL device shows a lower mean of 0.656

V and a reduced standard deviation of 0.012 V. These Gaussian-distributed fluctuations are consistent with variability mechanisms reported in prior studies, [10, 21, 22] validating our modeling approach.

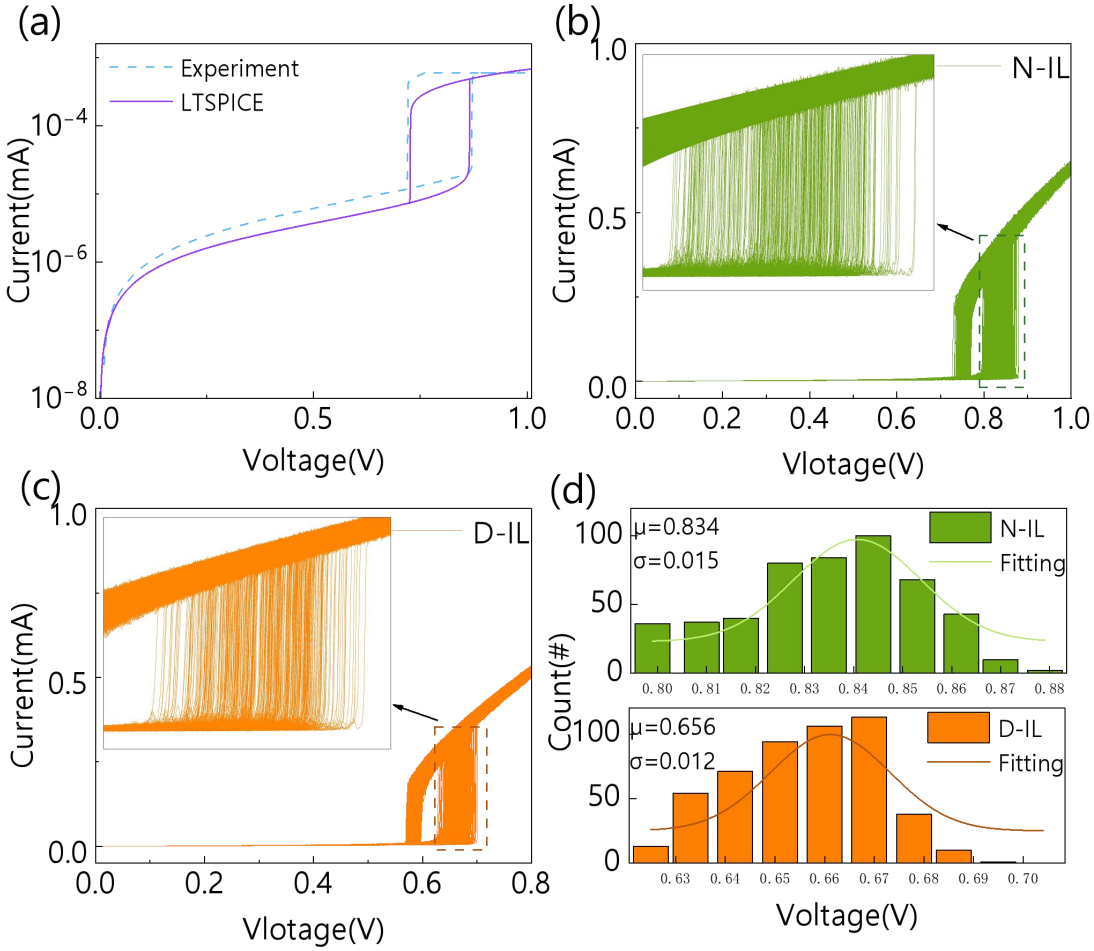

FIG.S4 (a) LTspice model of NbO_x-TSM is in good agreement with the experimental data. (b) and (c) When considering the thermal fluctuation equation of the device, the simulation was used to measure the distribution of V_{th} over 500 cycles, and this was statistically represented in (d).

The incorporation of the low-thermal-conductivity interlayer reduces the device leakage current from 4.2 μA to 2.9 μA, as shown in **Figure S5**. To evaluate its efficacy in mitigating thermal crosstalk within a dense array, we simulated the thermal distribution in a 3 × 3 × 3 array using COMSOL. Here, to match the characteristics of 2D devices, some modifications were made to the 3D device modeling: the thickness of NbO_x is set to 30 nm, and the radius is fixed at 30 nm. **Figure S6** shows the simulated thermal distribution immediately after V_{th} in two working conditions. The results, summarized in **Table S1**, when a triangular bias

voltage is applied, the temperature in the threshold switching region decreases by 981 K from the N-IL device to the D-IL device, while that in the adjacent devices drops by 171 K.[18]

To further verify the thermal management in a high-density integration scenario, we simulated a 10×10×5 array, as shown in **Figure S7**, with results summarized in **Table S2**. The temperatures across all regions within the array decreased by nearly half. For instance, the temperature in the threshold region of adjacent devices dropped by approximately 435K.

Pt top and bottom electrodes (TE/BE), while acting as efficient heat sinks due to their high thermal conductivity, also promote thermal crosstalk. This can elevate the temperature of adjacent devices and potentially triggering malfunctions.[23] The introduced interlayer mitigates this issue by confining Joule heat, thereby reducing the total heat generated during switching. Consequently, temperatures in the active region, electrodes, and adjacent devices are significantly suppressed. In small-scale arrays, generated heat can dissipate readily to the boundaries. However, in large-scale arrays, heat accumulation increases local temperature as the array volume expands. This analysis confirms that the low-thermal-conductivity interlayer $CdTe_2$ effectively minimizes thermal crosstalk, enhancing the operational reliability of densely integrated memristor arrays.

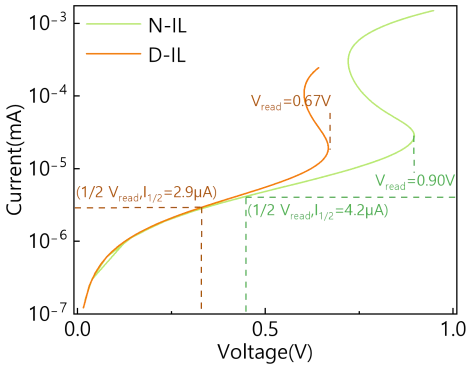

FIG.S5 The I-V curve diagrams of N-IL and D-IL devices. The leakage current of D-IL is lower than that of N-IL.

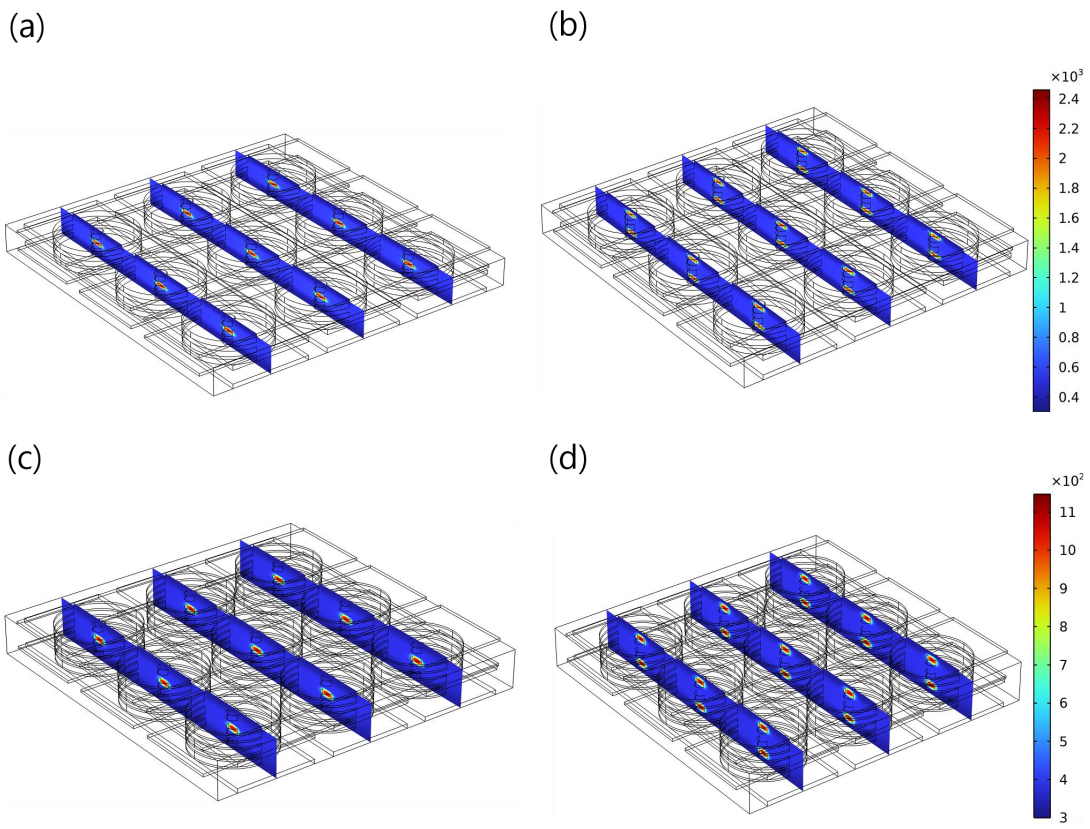

FIG.S6 In a $3 \times 3 \times 3$ array, using COMSOL to simulate and analyze the thermal distribution at the moment after V_{th} in two working conditions. (a) and (c) represent the temperature distribution during the operation of the N-IL and D-IL intermediate layer memristors, respectively. (b) and (d) represent the temperature distribution of the upper and lower layers of the N-IL and D-IL memristors during their operation.

Table S1. Temperature statistics corresponding to Figure S6.

	Threshold switching area	**Interlayer ($CdTe_2$)**	**TE/BE**	**Adjacent device threshold switching region**
S14(a)	2059K	/	566K	463K
S14(b)	2085K	/	549K	530K
S14(c)	1082K	617K	359K	330K
S14(d)	1104K	639K	366K	359K

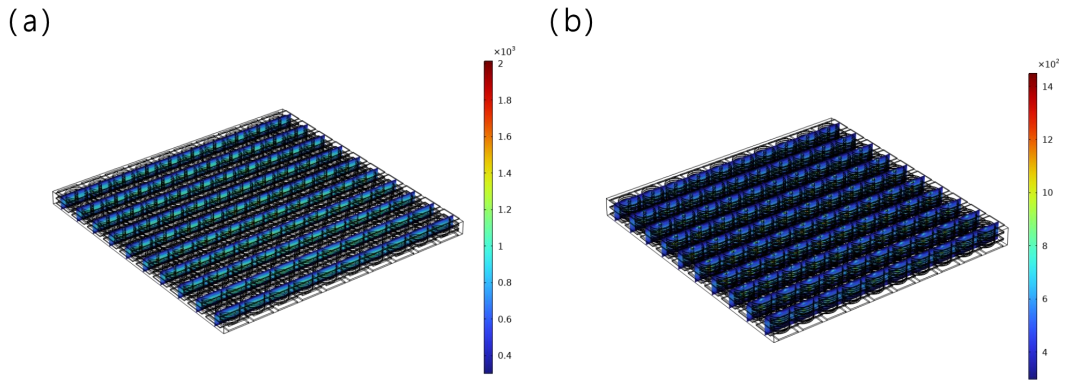

FIG.S7 Simulated temperature distribution in a 10 × 10 × 5 crossbar array immediately after threshold switching. The working layers are arranged in an alternating pattern, separated by non-working layers for thermal isolation. Distinct isotherm contours highlight the temperature reduction achieved by the design. (a) Array without an interlayer (N-IL). (b) Array with the $CdTe_2$ interlayer (D-IL).

Table S2. Temperature values extracted from the simulations in Figure S7.

	Threshold switching area	**Interlayer ($CdTe_2$)**	**TE/BE**	**Adjacent device threshold switching region**
N-IL (S7(a))	2331 K	/	932 K	996 K
D-IL (S7(b))	1258 K	968 K	578 K	561 K

As the thermal recovery time required for heat dissipation in a dense array may be a critical factor for system latency, we provide an in-depth discussion on residual heat dissipation rates.

First, we consider the thermal time constant of the device. As shown in **Figure 2**, the R_{th} of D-IL is estimated in the static limit, at which point the C_{th} value is calculated to be 1.31e-16 J/K through numerical simulation (COMSOL probe). The effective thermal time constant $\tau_{th}=R_{th}\cdot C_{th}$ is thus estimated to be 0.836 ns. Here, R_{th} relates to thermal conduction, while C_{th} represents the thermal inertia included of the device. This sub-nanosecond time constant aligns well with the requirements of

high-speed neuromorphic circuits.[24, 25]

Second, to evaluate performance in a high-density scenario, we simulated a 10×10×5 array under a periodic bias voltage (**Figure S8(a)**). **Figure S8(b)** shows the current of a single device alongside the temperature of its switching region and the surrounding air. At point B in each cycle, where the current is nearly zero, the switching region temperature and air temperature for the 10×10×5 array without the interlayer (N-IL) drop to approximately 334 K. The device temperature continues to decrease with the falling voltage, while the residual air temperature decays to 301 K within 311 ns. Although previous studies have indicated that small-sized arrays can achieve thermal equilibrium within the picosecond range,[23] in this study, the residual heat dissipation time of the large-sized array also falls within the picosecond range. For the array with the interlayer (D-IL), the switching region and air temperatures drop to approximately 332 K and 321 K, respectively, with the residual air temperature reaching 301 K within 400 ns. The heat dissipated per cycle is represented by the shaded block in **Figure S8(c)**, with a detailed view in **Figure S8(d)**. The heat dissipation rate ($\Delta T/\Delta t$) and time are summarized in **Table S3**. For the array with our interlayer, the device dissipation rate decreases from 1.1×10^9 K/s to 6.6×10^8 K/s in region 1, and from 7.4×10^7 K/s to 3.9×10^7 K/s in region 2. Correspondingly, the air dissipation rate decreases from 2.9×10^8 K/s to 1.4×10^8 K/s in region 1, and from 7.33×10^7 K/s to 3.2×10^7 K/s in region 2. Compared with the N-IL array, although the dissipation rate of the D-IL array has decreased, the residual heat dissipation is still extremely rapid, and the residual heat dissipation time changes little, having a very small impact on the subsequent operation cycle. This is because both the device and the air temperature can follow the change of the bias voltage, without significant deviation.

Furthermore, the I-V characteristics of individual devices under periodic bias (**Figure S9**) that the threshold voltage does not change significantly over a period of ten consecutive cycles. This confirms that the system's rapid heat dissipation rate ensure reliable operation.

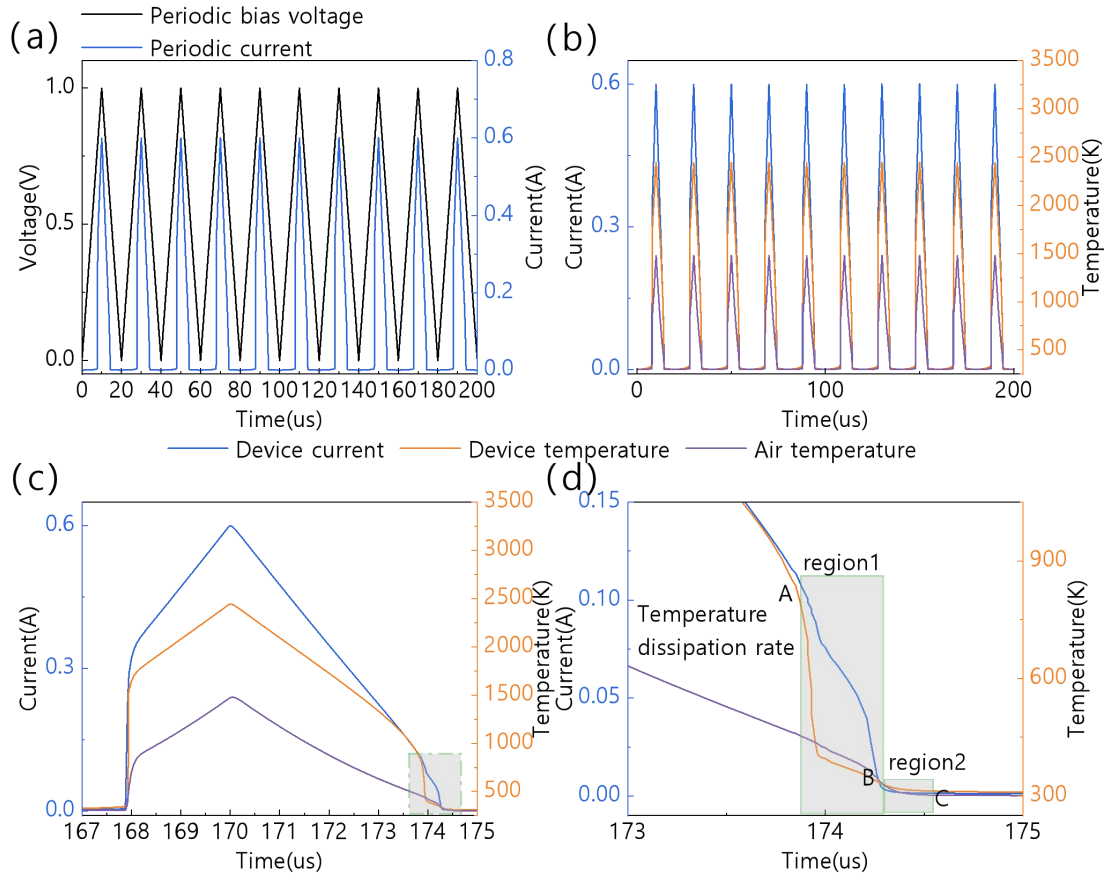

FIG.S8 Transient thermal and electrical response of a representative device in the array under periodic switching. (a) Applied triangular-wave bias voltage (period: 20 μs, amplitude: 1 V) and the corresponding current of a single device in the array. (b) Device current plotted together with the temperature of the device's switching region and the surrounding air temperature. (c) The heat-dissipation portion within a single cycle; the shaded block region is enlarged in Figure (d). Region 1 (A→B) corresponds to the device turn-off process (current reaches zero at point B). Region 2 (B→C) represents the dissipation of residual heat after switching.

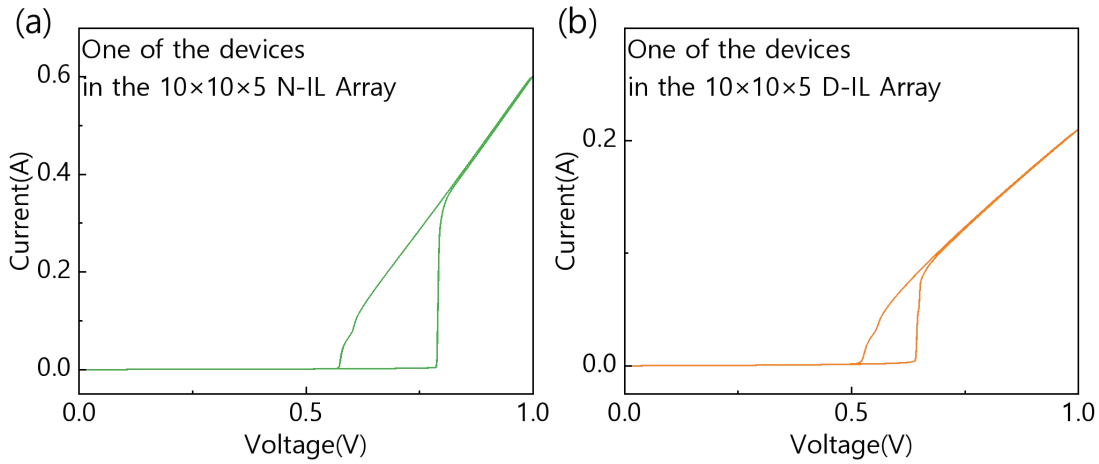

FIG.S9 Current- voltage (I- V) characteristics of a single device in the array during ten consecutive switching cycles. (a) Array without an interlayer (N- IL, 10×10×5). (b) Array with the $CdTe_2$ interlayer (D- IL, 10×10×5).

Table S3. Measured heat-dissipation rate and residual heat dissipation time.

	10×10×5 N-IL			**10×10×5 D-IL**		
	Region1 (ΔT/Δt)	**Region2 (ΔT/Δt)**	**Residual heat dissipation**	**Region1 (ΔT/Δt)**	**Region2 (ΔT/Δt)**	**Residual heat dissipation**
Device	1.1×10^{9} K/s	7.4×10^{7} K/s	/	6.6×10^{8} K/s	3.9×10^{7} K/s	/
Air	2.9×10^{8} K/s	7.3×10^{7} K/s	311 ns	1.4×10^{8} K/s	3.2×10^{7} K/s	400 ns

A key advantage of P-F conduction mechanism is its relatively low operational temperature range (380–400 K) for threshold switching, which offers superior power efficiency and enhanced device durability compared to the NbO_x-IMT mechanism, which requires temperatures near 1080 K.[26] **Table S4** provides a comprehensive comparison between this work and other NbO_x-based TSM designs. The comparison demonstrates that while previous studies often achieve improvements in a single performance metric, our design simultaneously delivers significant gains across multiple key parameters, including thermal switching voltage, threshold stability.

Table S4. Comparison of other NbO_x Mott memristor designs with this work

Literature	**ΔV_{th}**	**ΔV_h**	**Threshold stability**
Pt/Nb/ORL-NbO_x/W/Ti[27]	↑ 0.23V	/	/
AlN/NbO_x/Pt/Ti[28]	/	↑ 0.40V	↑
Pt/LTO/Nb/NbO_x/W/Ti[8]	/	/	↑
Ti/NbO_2/HfO_2/Pt[29]	↑ 0.1V	↑ 0.1V	/
Pt/NbO_2/HfO_2/Rough-Pt[30]	↑ 0.1V	↑ 0.2V	/
Pt/TiO_2/NbO_2/Pt[31]	↓ 1.0V	/	↓
TiN-size/NbO_2/W[32]	↓ 0.5V	/	/
This Work	**↓ 0.22V**	**↓ 0.12V**	**↑**

Note: ↑ indicates increase, ↓ indicates reduction, / indicates no relation.

The action potential in biological neurons evolves through four distinct four phases,[33] as illustrated in **Figure S10** and **S11**, which are mapped to the corresponding states in our memristive neuron**.** First, during the resting potential (**Figure S10(a)**), the Na^+ and K^+ concentrations across the cell membrane remain basically unchanged, resulting in zero net ionic current. This state corresponds to the latter part of segment of 1→2 in **Figure S11**, where both Na^+ and K^+ channels are closed (OFF state) and the device remains in a HRS. Second, when the membrane potential rises and the applied voltage exceeds the threshold, the Na^+ channels are activated (ON state), and the device switches to a LRS, representing the depolarization behavior (**Figure S10(b)** and segment 2→3 in **Figure S11**). Third, as the membrane potential peaks, the K^+ channels open, allowing K^+ efflux that drives repolarization (**Figure S10(c)** and segment 3→1 in **Figure S11**), during which the device returns to the HRS. Finally, in the subsequent refractory period (**Figure S10(d)** and the first half of segment 1→2 in **Figure S11**), K^+ continues to flow out until the membrane potential stabilizes, rendering the neuron unresponsive to further stimuli—a state maintained by the device's HRS.

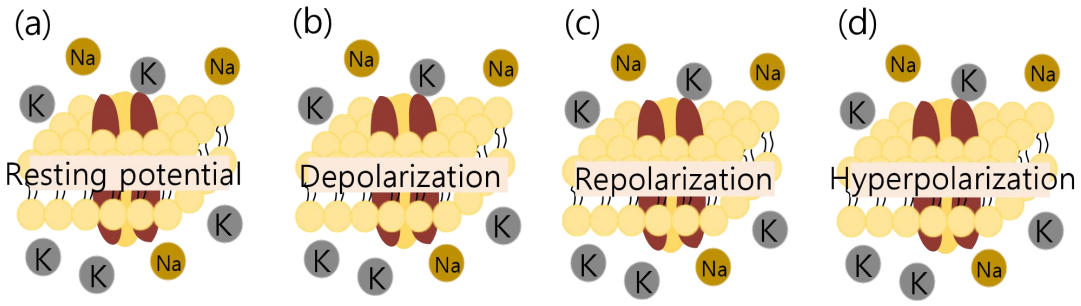

FIG.S10 Four dynamic states of neuronal activity during a single pulse cycle. (a) Resting potential: Both Na^+ and K^+ channels remain closed. (b) Depolarization: Activation of Na^+ channels triggers ion influx across the cellular membrane. (c) Repolarization: Activation of K^+ enables ion efflux. (d) Hyperpolarization: Neural recovery following stimulus-induced activation.

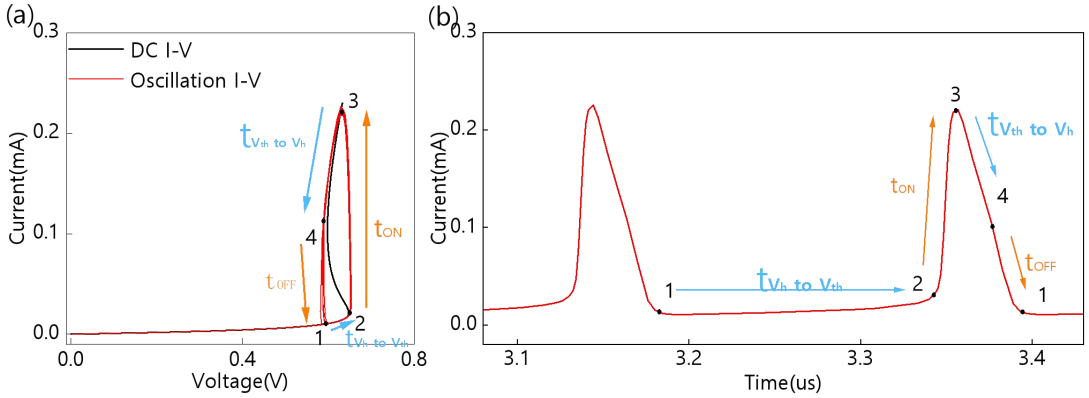

FIG.S11 Oscillation characteristics of D-IL (5 nm + 5 nm) device at 301 K. (a) *I-V* curve when a DC voltage is applied; (b) *I-t* dynamics during sustained oscillation.

Table S5. The specific times of each stage of the oscillation difference process.

Time (us)	5nm+5nm、RC(example)	5nm+5nm、RC(magnify)	10nm+10nm、RC(invariability)
$t_{V_h\ to\ V_{th}}$	0.159	0.477	0.065
t_{ON}	0.012	0.016	0.026
$t_{V_{th}\ to\ V_h}$	0.019	0.016	0.030
t_{OFF}	0.016	0.017	0.023

The NbO_x-based threshold-switching memristor (TSM) leaky integrate-and-fire (LIF) neuron effectively emulates fundamental functionalities of biological neurons. Specifically, it successfully replicates four characteristic features of biological nociceptors: threshold detection, relaxation, non-adaptation, and sensitization,[34] as comprehensively demonstrated in **Figure S12**. **Figure S12(a)** illustrates the threshold characteristic: when external stimuli exceed a specific voltage threshold, nociceptors

initiate pain signal transmission, resulting in neural conduction and pain perception. Sub-threshold stimuli elicit no response. **Figure S12(b)** demonstrates the relaxation property, showing that when two nociceptive stimuli are separated by sufficient time intervals (1.3 μs or 3.3 μs following a 1.3 V stimulus), no response current is generated. The non-adaptation characteristic is shown in **Figure S12(c)**, where continuous harmful stimulation (1.1 V following 1.3 V priming stimulus) produces sustained response currents without signal attenuation. **Figure S12(d)** demonstrates injury-induced sensitization through graded pulse stimulation, manifesting as allodynia (response to normally non-noxious stimuli) and hyperalgesia (enhanced response to noxious stimuli). Quantitative analysis in **Figure S12(e)** shows increased current peaks under sensitized conditions. These results collectively validate the biophysical plausibility of our NbO_x-TSM LIF model, demonstrating its capability to reproduce complex nociceptive processing for advanced neuromorphic computing applications.

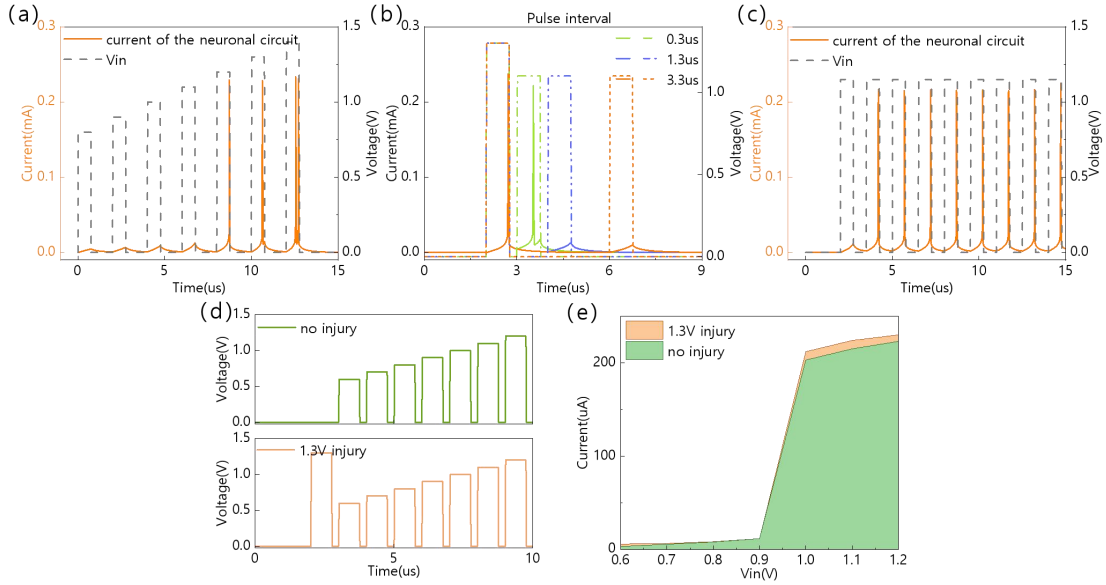

FIG.S12 Neural circuit response characteristics under varied stimulation paradigms. (a) Output current response to amplitude-modulated input pulses (0.8–1.4 V range, 0.1 V step size, 2 μs period). (b) Current output for fixed input voltages of 1.3 V and 1.1 V, showing corresponding time intervals of 0.3 μs, 1.3 μs, and 3.3 μs. (c) Sustained oscillation behavior under continuous pulse stimulation (1.15 V amplitude, 1.5 μs duration). (d) Injury simulation protocol: a priming stimulus of 1.3 V followed by test pulses ranging from 0.6 V to 1.2 V (0.1 V step size, 1 μs period). (e) Comparison of current peak amplitudes under normal versus injury-simulated conditions.

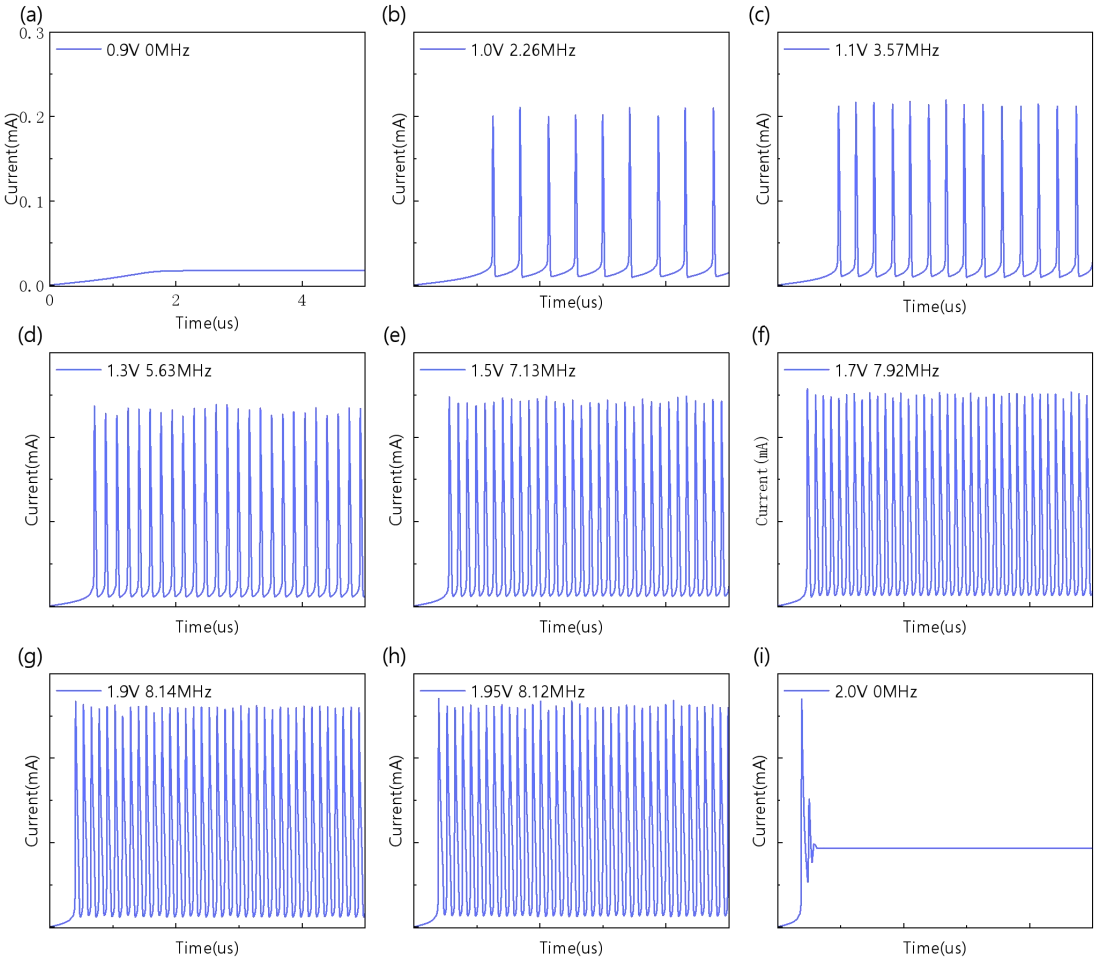

FIG.S13 Detailed description of the variation of spike oscillation with applied voltage for the D-IL (5 nm + 5 nm) device under an ambient temperature of 301 K.

As supported by existing research,[9] the oscillation frequency is predominantly governed by the V_{th} (**Figure 4(c)**), while the HRS and LRS exhibit a relatively weak influence, as shown in **Figure S14(a)**. Furthermore, **Figure 4(d)** reveals that the reduction in oscillation frequency with increasing interlayer thickness exhibits a saturation trend. This saturation correlates with the device's resistance states: **Figure S14(b)** shows that the change of HRS is minor, and the degree of increase in the oscillation frequency gradually weakens. During this process, LRS demonstrates a gradual increase.

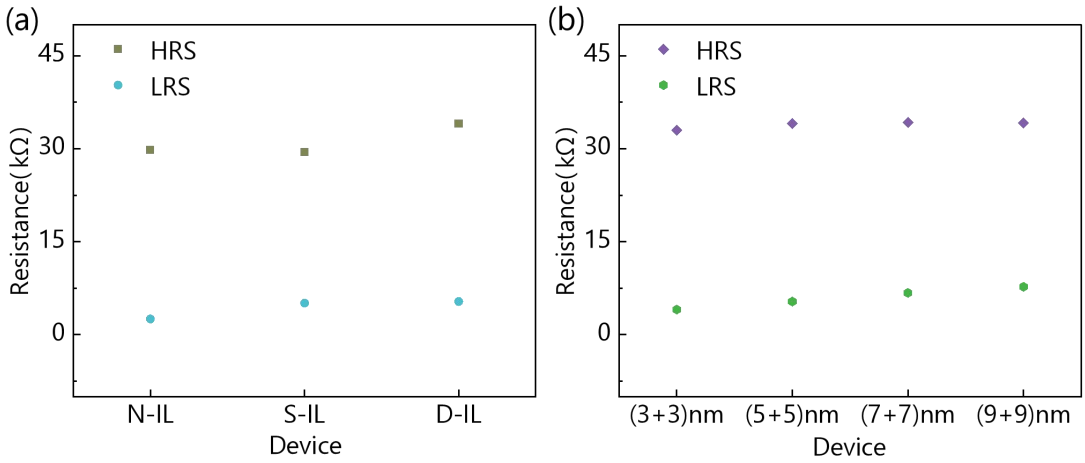

FIG.S14 (a) The HRS and LRS of the device vary with the change of the device's interlayer. (b) The HRS and LRS of the device change with the thickness of the device's interlayer.

In the LIF neural circuit, the oscillation frequency is governed by the memristor's switching dynamics and the circuit's RC time constant. As demonstrated in **Figure S15**, the frequency exhibits an inverse relationship with both resistance and capacitance. Specifically, **Figure S15(a)** shows that increasing the resistance from 15 kΩ to 25 kΩ demands a higher input voltage to maintain a given oscillation frequency. Similarly, **Figure S15(b)** indicates that a larger capacitance (58 pF to 580 pF) limits the maximum achievable frequency, even with increased voltage. Therefore, the oscillation frequency can be effectively tuned not only by the memristor itself but also synergistically through the strategic selection of resistance and capacitance values, enabling a broader range of neuromorphic dynamics.

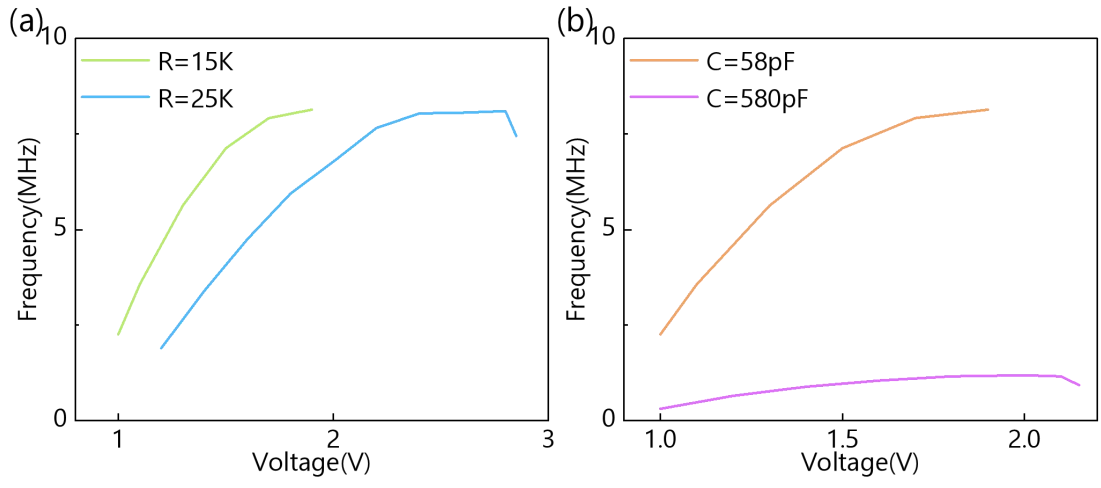

FIG.S15 (a) and (b) respectively represent the variation trends of resistance and

capacitance with respect to the input voltage.

Furthermore, considering the influence of other disturbances on the oscillation in practical applications,[14, 35] we introduced Gaussian noise into the circuit, as shown in **Figure S16**. With a 1.2 V input signal, oscillations remain stable when the noise amplitude is below 10% (**Figure S16(a)**) of the signal amplitude but are disrupted when the noise exceeds approximately 20% (**Figure S16(b)**) establishing a clear operational tolerance.

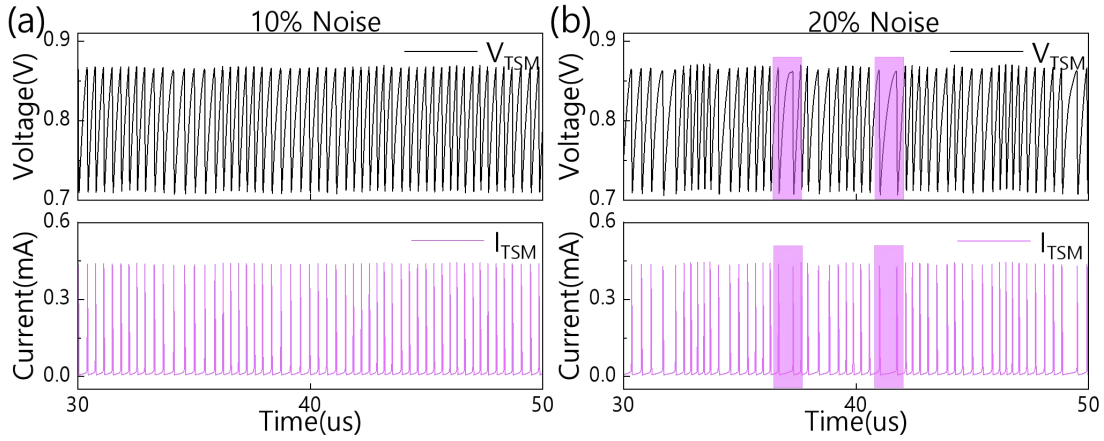

FIG.S16 (a) When the circuit interference is 10% Gaussian noise, the oscillation is not affected. (b) When the circuit interference is 20% Gaussian noise, the oscillation is significantly affected.

Neuromorphic systems with biomimetic characteristics represent a promising approach for reducing energy consumption in computing systems. The energy consumption of a neuromorphic cells is calculated by measuring the circuit current (total current through R_s) and the voltage across the cell, then integrating their product over time.[9] **Figure S17(a)** shows these parameters under DC input conditions ($V_{in} = 1.5V, R_s = 15k\Omega, C = 58pF$). The energy consumed per spike was computed accordingly. **Figure S17(b)** demonstrates that for a fixed interlayer thickness, the energy consumption per spike decreases from 14.41 pJ for N-IL device, to 5.73 pJ for the S-IL device, and to 4.96 pJ for D-IL devices.

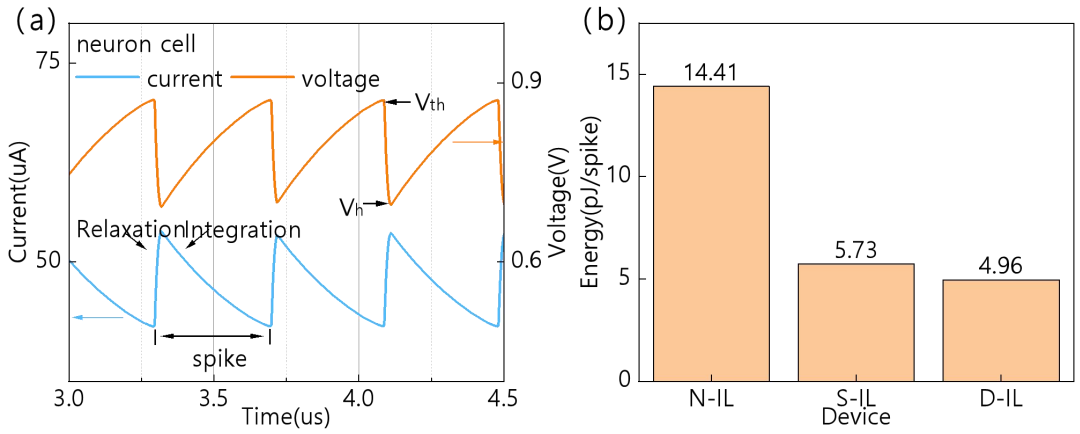

FIG.S17 (a) Calculation diagram of charging and discharging energy consumption during a single spike: the orange curve represents the current flowing into the node of the neuronal unit, and the blue curve represents the voltage across the neuronal soma. (b) Comparison of energy consumption per spike for the three devices configurations (N-IL, S-IL, and D-IL).

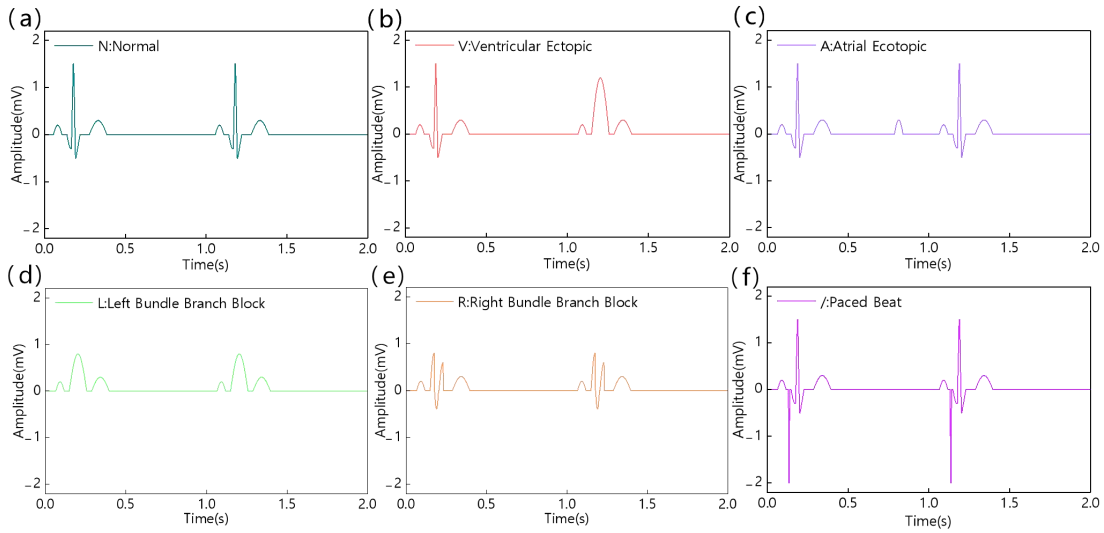

FIG.S18 (a)-(f) Six arrhythmia types: N, V, A, L, R, and / as determined by systematic monitoring.

Supplementary Note 2: Advantages of the Memristor Architecture over Conventional Digital Processors

The proposed memristor-based architecture offers distinct advantages over traditional digital processors or low-power microcontrollers for bio-signal processing, primarily in energy efficiency, temporal dynamics, hardware integration, and edge deployment.

First, regarding energy efficiency, conventional digital processors suffer from the von Neumann bottleneck, where frequent data shuttling between separate memory and processing units incurs significant power overhead during real-time ECG analysis.[36] For instance, microcontroller-based ECG edge computing systems consume ~66 mW for data acquisition and 99–137 mW for real-time inference.[37, 38] In contrast, memristors enable dynamic signal processing through NDR response, opening the door for complex edge computing and real-time data processing, thereby eliminating the cost of data transmission.[39] As a new type of storage device, offer a significant advantage in terms of low power consumption, which is superior to traditional digital implementations.[40] Our NbO_x device, with ~5 ns switching speed, can thus achieve per-inference energy consumption at the pJ level, offering a substantial advantage over MCU-based solutions.[17]

Second, and more critically, our memristor architecture possesses inherent temporal dynamics advantageous for processing physiological signals. Key ECG s features—such as the QRS complex duration (80–120 ms), PR interval (120–200 ms), and QT interval (200–400 ms)—are inherently temporal.[41] Conventional digital systems require additional clock circuits, sampling buffers, and memory to process such features, whereas our thermally engineered NbO_x memristor exhibits a tunable thermal relaxation time constants, with threshold switching governed by internal temperature dynamics.[42] This allows the device's memory decay characteristics to be matched to ECG time scales, enabling intrinsic temporal filtering without extra circuitry. Supporting this, Kumar et al. demonstrated that a single NbO_x neuron can emulate 18 biomimetic neuronal behaviors—including integrator, threshold variability, and frequency adaptation functions—via engineered thermal dynamics.[43] Similarly,

Yuan et al. constructed a sparse pulse asynchronous encoder for electrocardiogram using oxide-based memristors, and the classification accuracy for arrhythmia reached 95.83%.[44]

Third, from a hardware perspective, conventional wearable ECG systems typically integrate multiple discrete components (analog-to-digital converters, microcontrollers, static random-access memory, digital filter circuits, and wireless transmission modules), increasing system complexity, area, and power.[45] Memristors, with their two-terminal metal-insulator-metal structure, offer stable switching at sub-10-nm feature sizes and can be densely integrated into 3D crossbar arrays.[40, 46] More importantly, a single memristor device can simultaneously implement memory, computation, and temporal processing, dramatically simplifying the system architecture. This multifunctionality is particularly valuable for area- and power-constrained wearable devices.

Finally, for practical deployment, conventional wearable ECGs often rely on cloud processing, requiring wireless transmission (Bluetooth: 10–25 mW; WiFi: 150–250 mW) that introduces latency, privacy risks, and bandwidth limitations.[47] Research has shown that artificial spiking neurons possess the computing capabilities within their sensors, which can be used to regulate peripheral information and achieve local data processing.[27, 48] This edge-computing approach can retain 85–95% of raw data of raw data on-device, transmitting only compressed results, thereby slashing transmission power and extending battery life—a crucial feature for continuous arrhythmia monitoring.[47]

In summary, these advantages—rooted in the physical operating mechanism of memristors—are difficult to replicate with traditional digital or microcontroller-based systems.

Table S6 Material parameters used in the COMSOL simulation.

SYMBOL	VALUE[UNITS]	DESCRIPTION
$\boldsymbol{\sigma_0}_{NbO2}$	8.4×10^{4}[S/m]	The prefactor of the electrical conductivity of NbO_2[15]
$\rho_{m,NbO2}$	5800[kg/m^3]	Density of mass of NbO_2[15]
$C_{p,NbO2}$	459[J/(kg•K)]	Specific heat of NbO_2[15]
$\boldsymbol{\varepsilon}_i$	22	The relative dielectric constant of NbO_2[15]
κ_{ph}	0.12[W/(m•K)]	Heat conductivity of NbO_2[15]
$\boldsymbol{\sigma}_{Nb2O5}$	1×10^{-10}[S/m]	Room temperature conductivity of Nb_2O_5[15]
$\rho_{m,Nb2O5}$	4550[kg/m^3]	Density of mass of Nb_2O_5[15]
$C_{p,Nb2O5}$	459[J/(kg•K)]	Heat capacity at constant pressure of Nb_2O_5[15]
κ_{Pt}	71.4[W/(m•K)]	Heat conductivity of Platinum[15]
$\boldsymbol{\sigma}_{Pt}$	1×10^{7}[S/m]	Electrical conductivity of Platinum[15]
$\rho_{m,Pt}$	21450[kg/m^3]	Density of mass of Platinum[15]
$C_{p,Pt}$	133[J/(kg•K)]	Heat capacity at constant pressure of Platinum[15]
κ_{CdTe2}	0.33[W/(m•K)]	Heat conductivity of $CdTe_2$[7]
$\boldsymbol{\sigma}_{0,CdTe2}$	5×10^{3}[S/m]	Electrical conductivity of $CdTe_2$[7]
q	1.602×10^{-19}[C]	Unit charge quantity
k	1.38×10^{-23}[J/K]	boltzmann constant[15]
L	2.44×10^{-8}[W•Ω•K^{-2}]	Lorenz number for the Wiedemann-Franz law[15]

Reference

[1] A. Ali and Y.-H. Shin 2022 *Phys. Chem. Chem. Phys.* **24** 29772-29780 https://doi.org/10.1039/D2CP04123E.

[2] J. Zhang, X. Xia, Y. Gao, and Z. Huang 2023 *ACS Applied Energy Materials* **6** 11385-11395 https://doi.org/10.1021/acsaem.3c02379.

[3] T. Kang, Z. Lu, L. Liu, M. Huang, Y. Hu, H. Liu, R. Wu, Z. Liu, J. You, Y. Chen, K. Zhang, X. Duan, N. Wang, Y. Liu, and Z. Luo 2023 *Nano Lett.* **23** 11034-11042.

[4] R. Dagan, Y. Vaknin, A. Henning, J. Y. Shang, L. J. Lauhon, and Y. Rosenwaks 2019 *Appl. Phys. Lett.* **114** 101602.

[5] S. Huang 2023 *Modern Physics* **13** 8-16 https://doi.org/10.12677/MP.2023.131002.

[6] X. Wan, E. Chen, J. Yao, M. Gao, X. Miao, S. Wang, Y. Gu, S. Xiao, R. Zhan, K. Chen, Z. Chen, X. Zeng, X. Gu, and J. Xu 2021 *ACS Nano* **15** 20319-20331.

[7] B. Wan, Z. Gao, X. Huang, Y. Yang, L. Chen, Q. Wang, C. Fang, W. Shen, Y. Zhang, H. Ma, H. Gou, X. Jia, and Z. Zhang 2022 *ACS Applied Energy Materials* **5** 9549-9558 https://doi.org/10.1021/acsaem.2c01176.

[8] Y. Wang, G. Zhang, C. Gong, S. Zhao, Y. Yuan, S. Fan, J. Hu, X. Li, W. Liu, L. Geng, and C. Yu Han 2025 *IEEE Trans. Electron Devices* **72** 3605-3610 https://doi.org/10.1109/TED.2025.3574134.

[9] Y. Ding, Y. Zhang, X. Zhang, P. Chen, Z. Zhang, Y. Yang, L. Cheng, C. Mu, M. Wang, D. Xiang, G. Wu, K. Zhou, Z. Yuan, and Q. Liu 2022 *Front. Neurosci.* **15** 786694.

[10] Y. Wang, W. Wang, H. Xu, S. Liu, R. Cao, Y. Sun, P. Tong, B. Song, and Q. Li 2024 *ACS Applied Nano Materials* **9** 10679-10689.
[11] P. O. Jean Rousset, Brian McCandless,Daniel Lincot 2008 *Chem. Mater.* **20** https://doi.org/10.1021/cm801887v.
[12] Z. Cai, B. Liu, X. Zou, and H.-M. Cheng 2018 *Chem. Rev.* **118** 6091-6133.
[13] N. T. Adilet, M. N. Sidorova, A. S. Slavich, M. K. Tatmyshevskiy, I. A. Zavidovskiy, G. A. Ermolaev, V. S. Volkov, D. A. Ghazaryan, and A. V. Arsenin 2024 *Bulletin of the Russian Academy of Sciences: Physics* **87** S453-S457.
[14] H. Rhee, G. Kim, H. Song, W. Park, D. H. Kim, J. H. In, Y. Lee, and K. M. Kim 2023 *Nat. Commun.* **14** 7199.
[15] W. Park, G. Kim, J. H. In, H. Rhee, H. Song, J. Park, A. Martinez, and K. M. Kim 2023 *Nano Lett.* **23** 5399-5407.
[16] S. Kumar, Z. Wang, N. Davila, N. Kumari, K. J. Norris, X. Huang, J. P. Strachan, D. Vine, A. L. D. Kilcoyne, Y. Nishi, and R. S. Williams 2017 *Nat. Commun.* **8** 658.
[17] M. D. Pickett and R. Stanley Williams 2012 *Nanotechnology* **23** 215202.
[18] Z. Zhang, A. Chen, G. Ma, Y. He, C.-Y. Lin, C.-C. Lin, H. Wang, and T.-C. Chang 2020 *IEEE Trans. Electron Devices* **67** 2771-2777.
[19] S. Kumar, J. P. Strachan, and R. S. Williams 2017 *Nature* **548** 318-321.
[20] G. Kim, J. H. In, Y. S. Kim, H. Rhee, W. Park, H. Song, J. Park, and K. M. Kim 2021 *Nat. Commun.* **12** 2906
[21] Y. Pei, B. Yang, X. Zhang, H. He, Y. Sun, J. Zhao, P. Chen, Z. Wang, N. Sun, S. Liang, G. Gu, Q. Liu, S. Li, and X. Yan 2025 *Nat. Commun.* **16** https://doi.org/10.1038/s41467-024-55293-9.
[22] Y. Kang, X. Zhai, Q. Yang, J. Hu, Z. Zhang, J. Miao, H. Chen, D. Pu, H. Hu, W. Chen, Y. Zhao, and B. Yu 2025 *ACS Materials Letters* **7** 2574-2579 https://doi.org/10.1021/acsmaterialslett.5c00380.
[23] P. Sun, N. Lu, L. Li, Y. Li, H. Wang, H. Lv, Q. Liu, S. Long, S. Liu, and M. Liu 2015 *Scientific Reports* **5** 13504.
[24] P.-Y. Chen and S. Yu 2015 *IEEE Trans. Electron Devices* **62** 4022-4028.
[25] J. B. Roldán, G. González-Cordero, R. Picos, E. Miranda, F. Palumbo, F. Jiménez-Molinos, E. Moreno, D. Maldonado, S. B. Baldomá, M. Moner Al Chawa, C. de Benito, S. G. Stavrinides, J. Suñé, and L. O. Chua 2021 *Nanomaterials* **11** 1261.
[26] G. A. Gibson, S. Musunuru, J. Zhang, K. Vandenberghe, J. Lee, C.-C. Hsieh, W. Jackson, Y. Jeon, D. Henze, Z. Li, and R. Stanley Williams 2016 *Appl. Phys. Lett.* **108** 023505.
[27] Y. Yuan, R. Gao, Q. Wu, S. Fang, X. Bu, Y. Cui, C. Han, L. Hu, X. Li, X. Wang, L. Geng, and W. Liu Jul 28 2023 *ACS Sens* **8** 2646-2655.
[28] G. Liu, F. Li, Y. Chen, H. Ren, D. Li, Y. Wang, Y. Tang, Z. Zhang, R. Wang, H. Wang, and B. Zhu 2024 *IEEE Electron Device Lett.* **45** 708-711 https://ieeexplore.ieee.org/abstract/document/10423063.
[29] Y. Jin, Z. Zhang, S. Ke, Y. Zhao, C. Liu, G. Liu, and C. Ye 2025 *Appl. Phys. Lett.* **127** 113502 https://doi.org/10.1063/5.0265442.

[30] X. Liu, S. K. Nandi, D. K. Venkatachalam, K. Belay, S. Song, and R. G. Elliman 2014 *IEEE Electron Device Lett.* **35** 1055-1057 https://ieeexplore.ieee.org/document/6878476.
[31] M. Kang and J. Son 2016 *Appl. Phys. Lett.* **109** 202101
[32] E. Cha, J. Park, J. Woo, D. Lee, A. Prakash, and H. Hwang 2016 *Appl. Phys. Lett.* **108** 153502.
[33] H. Chen, H. Li, T. Ma, S. Han, and Q. Zhao 2023 *Science and Technology of Advanced Materials* **24** 2183712.
[34] Y. Qin, M. Wu, N. Yu, Z. Chen, J. Yuan, and J. Wang 2024 *ACS Applied Electronic Materials* **6** 4939-4947 https://doi.org/10.1021/acsaelm.4c00482.
[35] K. Boahen, Y. Wang, J. Wijekoon, T. Serrano-Gotarredona, S. Saighi, F. Folowosele, K. Hynna, J. Arthur, G. Cauwenberghs, J. Schemmel, S. Renaud, P. Häfliger, P. Dudek, S.-C. Liu, T. Delbruck, R. Etienne-Cummings, A. v. Schaik, T. J. Hamilton, B. Linares-Barranco, and G. Indiveri 2011 *Front. Neurosci.* **5** 73.
[36] D. Ielmini and H. S. P. Wong 2018 *Nat. Electron.* **1** 333-343.
[37] P. Srivastava, N. Shah, and K. Jaiswal 2024 *Engineering Proceedings.* **78** 3 https://doi.org/10.3390/engproc2024078003.
[38] Z. Huang, L. F. Herbozo Contreras, W. H. Leung, L. Yu, N. D. Truong, A. Nikpour, and O. Kavehei 2024 *J Cardiovasc. Transl. Res.* **17** 879-892.
[39] H. Lu, S. Xie, W. Zhang, Y. Chen, J. Tao, C. M. Mhaskar, A. Roy Chaudhuri, Y. Lin, J. Li, S. Mathur, and Z. Huang 2025 *Nanoscale* **17** 20606-20642 https://doi.org/10.1039/D5NR02491A.
[40] Z. Xia, X. Sun, Z. Wang, J. Meng, B. Jin, and T. Wang 2025 *Nano-Micro Letters* **17** 217 https://doi.org/10.1007/s40820-025-01705-4.
[41] *Surawicz, B., & Knilans, T. K. (2008). Chou's Electrocardiography in Clinical Practice: Adult and Pediatric (6th ed.). Saunders Elsevier.*
[42] S. Slesazeck, H. Mähne, H. Wylezich, A. Wachowiak, J. Radhakrishnan, A. Ascoli, R. Tetzlaff, and T. Mikolajick 2015 *RSC Advances* **5** 102318-102322.
[43] G. Kim, J. H. In, Y. Lee, H. Rhee, W. Park, H. Song, J. Park, J. B. Jeon, T. D. Brown, A. A. Talin, S. Kumar, and K. M. Kim 2024 *Nat. Mater.* **23** 1237-1244.
[44] R. Yuan, P. J. Tiw, L. Cai, Z. Yang, C. Liu, T. Zhang, C. Ge, R. Huang, and Y. Yang 2023 *Nat. Commun.* **14** 3695.
[45] E. Covi, E. Donati, X. Liang, D. Kappel, H. Heidari, M. Payvand, and W. Wang 2021 *Front. Neurosci.* **15** 611300.
[46] H. Li, S. Wang, X. Zhang, W. Wang, R. Yang, Z. Sun, W. Feng, P. Lin, Z. Wang, L. Sun, and Y. Yao 2021 *Advanced Intelligent Systems* **3** 2100017.
[47] S. Patel, Park, H., Bonato, P., Chan, L., & Rodgers, M. 2012 *Journal of NeuroEngineering and Rehabilitation* **9** 21.
[48] S.-O. Park, H. Jeong, J. Park, J. Bae, and S. Choi 2022 *Nat. Commun.* **13** 2888.