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Supporting Information

Side gate vertical OECTs for integrated complementary circuits

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This PDF includes:
Figures S1-S24
Table S1-S2

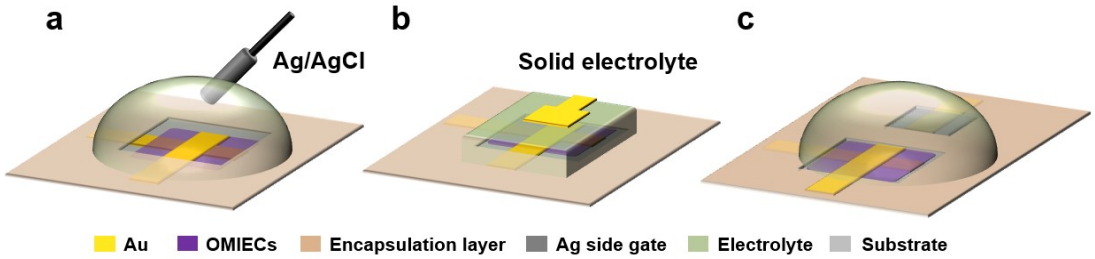

Figure S1. Schematic illustrations of OECT gate configurations: (a) Floating gate, (b) Top gate, and (c) Side gate.

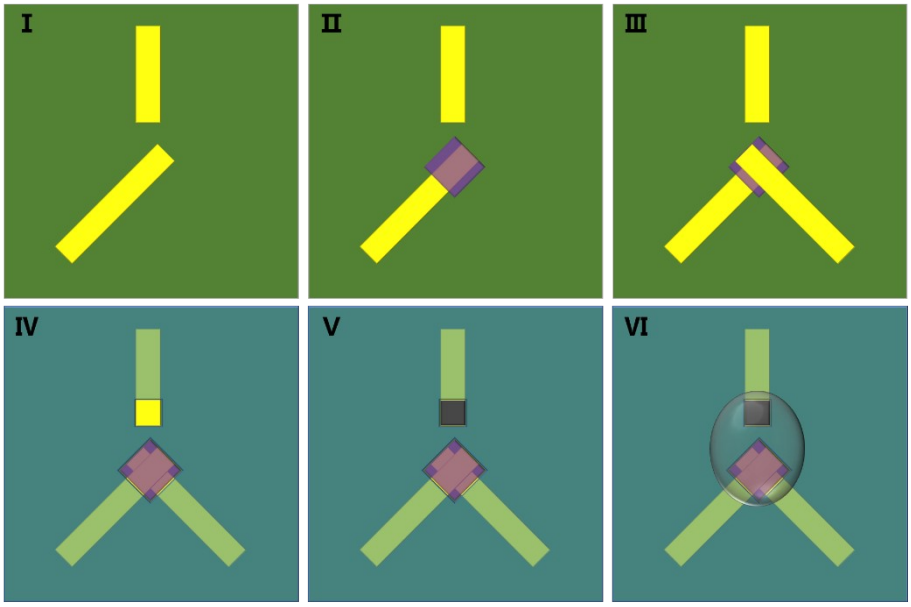

Figure S2. Fabrication process of Ag side gate vOECTs. (I) Bottom electrode and gate lead deposition, (II) N-type Homo-gDPP semiconductor deposition and patterning, (III) Top electrode deposition, (IV) Photoresist (SU8-2002) deposition and development, (V) Ag side gate electrode fabrication, (VI) Electrolyte application.

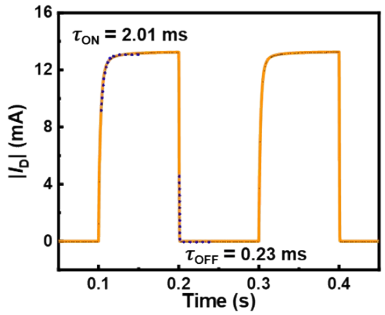

Figure S3. Transient response characteristics of the Homo-gDPP vOECT with an Ag/AgCl floating gate (V_D=0.1 V, V_G=0-0.8 V).

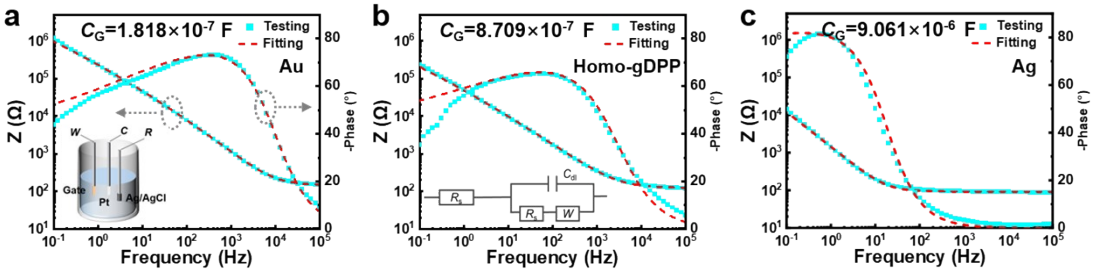

Figure S4. EIS characterization of different gate materials. (a) Au gate, (b) Homo-gDPP gate, (c) Ag gate.

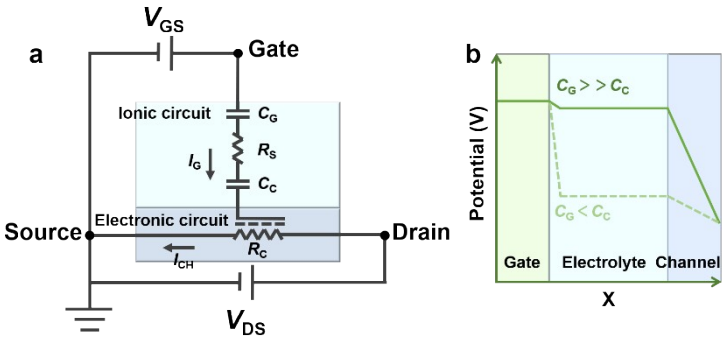

Figure S5. OECT equivalent circuit model. (a) Equivalent circuit model showing ionic and electronic pathways in OECTs. (b) Potential distribution in the ionic circuit: solid line represents effective gating with most voltage drop occurring at the electrolyte/channel interface; dashed line indicates poor gating where most voltage drops are located at the gate/electrolyte interface. C_G, gate/electrolyte interface capacitance; C_C, channel/electrolyte interface capacitance; R_S, electrolyte resistance; I_G, gate current; I_{CH}, channel current; x, distance.[1]

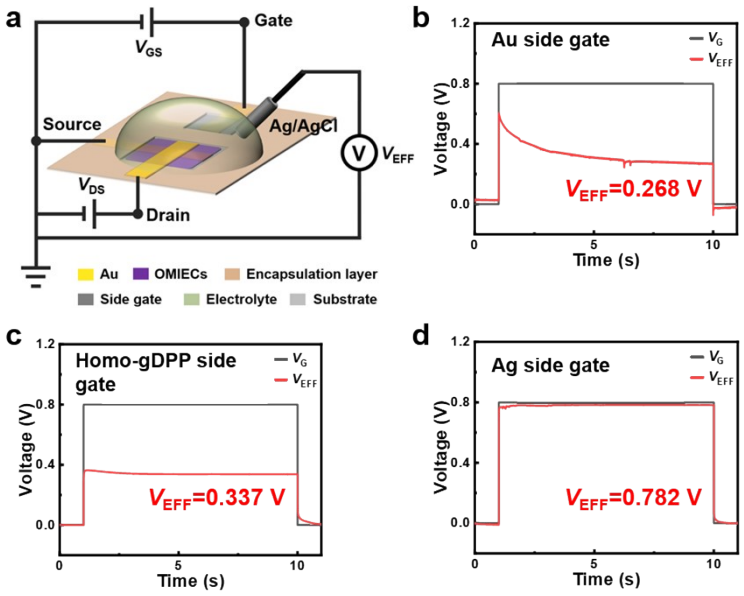

Figure S6. Effective gate voltage (V_{EFF}) measurement setup and results. (a) Schematic circuit diagram of the measurement setup. V_{EFF} measured with different gate materials

at applied V_G of 0.8 V: (b) Au, (c) Homo-gDPP, and (d) Ag.

Table S1. Comparative performances of vOECTs with Ag and Ag/AgCl gate electrodes.

Gate	I_{ON} (mA)	I_{ON}/I_{OFF}	g_{m_peak} (mS)	V_{ON} (V)
Ag/AgCl floating gate	12.62±0.35	(1.95±0.21)×10^8	74.52±3.23	0.23±0.01
Ag side gate	11.37±0.42	(2.19±0.50)×10^8	72.91±5.03	0.21±0.01

Variance data represent seven devices (V_D = 0.1 V, V_G = 0-0.8 V).

Table S2. Performance comparison of Ag side-gate OECTs in this work with reported side-gate OECTs.

Material	**Type**	**Structure**	**Channel size (w×d) (μm)**	**I_{ON} (mA)**	**g_{m_peak} (mS)**	**I_{ON}: I_{OFF}**	**τ_{ON}, τ_{OFF} (ms)**	**Ref.**
PEDOT:PSS	P	Planar	2500×10	34 (-0.6 V)	50		0.0008, /	2
BBL	N	Planar	100×10	0.03 (0.7 V)	0.125	3.0×10^3	0.62, 0.29	3
P($g_3$2T-TT)	P			0.2 (-0.7 V)	0.50	1.0×10^5	0.21, 0.36	
PEDOT:PSS	P	Planar	60×12	0.24 (-0.1)	2.0	2.2×10^3	/, /	4
gDPP-g2T	P	Vertical	30×30	2.5 (-0.1 V)	15.1	2.3×10^4	6.91, 1.09	5
BBL	N		120×30	2.2 (0.1 V)	7.6	7.1×10^3	12.17, 2.52	
3D hydrogel semiconductor	P	Planar	10000×5000	13.5 (-0.1 V)	53.1	8.5×10^3	/, /	6
PEDOT:PSS/PEI	P	Vertical	5×8	2 (-0.1 V)	4	1.0×10^4	0.009, /	7
FBDPPV-OEG	N	Planar	100×3	0.1 (0.7 V)	-	1.0×10^6	1.5, /	8
P(g32T-TT)	P		25×3	-0.1 (-0.7 V)	-	1.0×10^6	/, /	
BBL	N		100×3	0.1 (0.7 V)	-	1.0×10^5	3.2, /	
pgBTTT	P	Planar	97×47	3.1 (-0.5 V)	8	1.0×10^6	6.37, 1.08	9
Homo-gDPP	**N**	**Vertical**	**30×30**	**13.83 (0.1 V)**	**87.56**	**5.21×10^8**	**1.56, 0.14**	**This work**

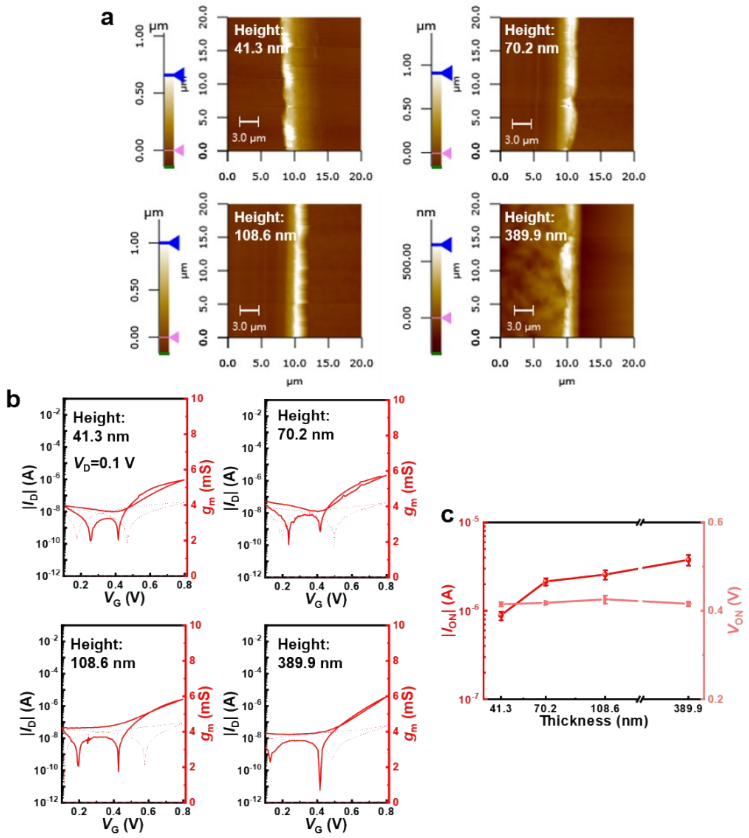

Figure S7. (a) Atomic force microscopy (AFM) thickness characterization of the Homo-gDPP gate layer, (b) Transfer characteristics of devices with different Homo-gDPP gate layer thicknesses, (c) I_{ON} and turn-on voltage (V_{ON}) extracted from the transfer characteristics.

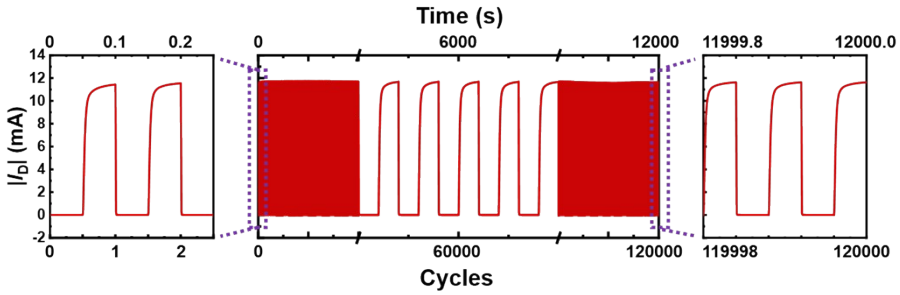

Figure S8. Cycling stability of an Ag side-gate OECT tested under a V_G sweeping between 0 and 0.8 V at a frequency of 10 Hz (0.01 M PBS).

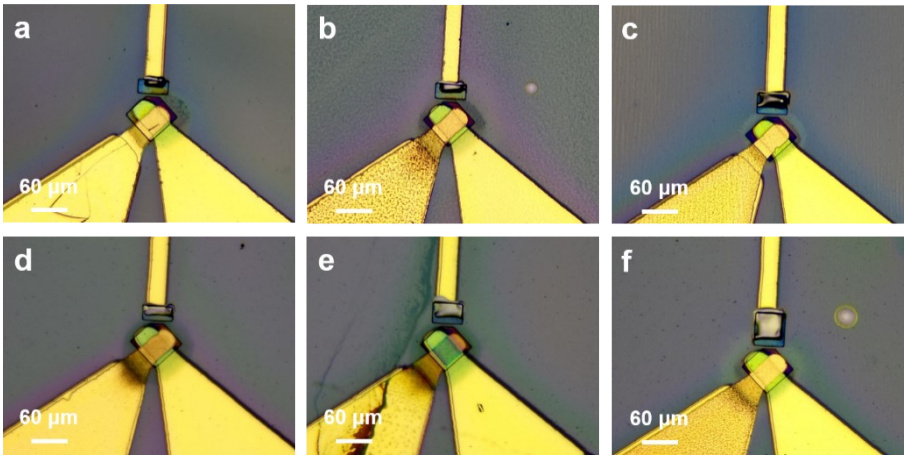

Figure S9. Optical microscopy images of printed Ag side-gate vOECTs with varying S_G: (a) 200 μm², (b) 240 μm², (c) 320 μm², (d) 400 μm², (e) 800 μm², (f) 1600 μm².

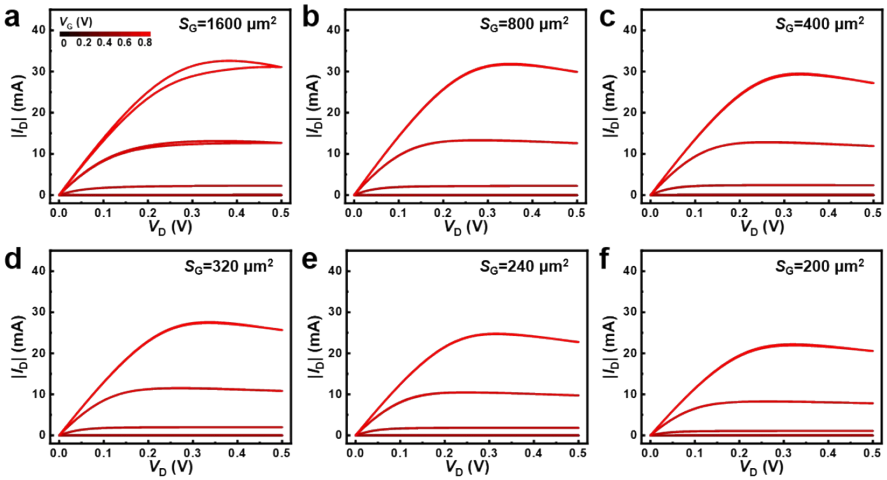

Figure S10. Output characteristics of the Homo-gDPP OECTs with different S_G: (a) 1600 μm², (b) 800 μm², (c) 400 μm², (d) 320 μm², (e) 240 μm², and (f) 200 μm².

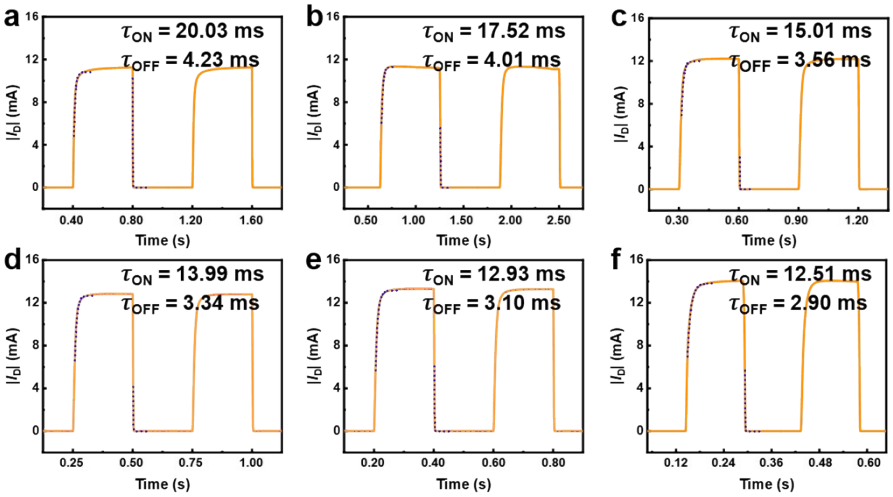

Figure S11. Transient response curves of printed Ag side-gate vOECTs with varying S_G: (a) 200 μm², (b) 240 μm², (c) 320 μm², (d) 400 μm², (e) 800 μm², (f) 1600 μm²

(V_D=0.1 V, V_G=0-0.8 V).

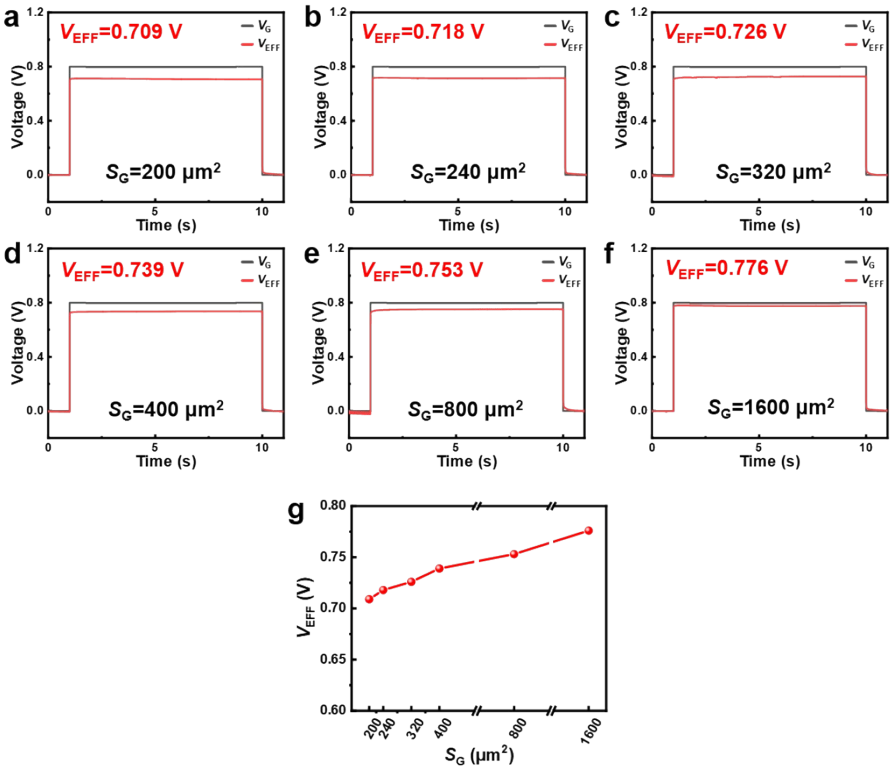

Figure S12. V_{EFF} measurements of printed Ag side gate vOECTs with varying S_G: (a) 200 μm², (b) 240 μm², (c) 320 μm², (d) 400 μm², (e) 800 μm², (f) 1600 μm², (g) The summary of V_{EFF} under varying S_G (ranging from 200 to 1600 μm²).

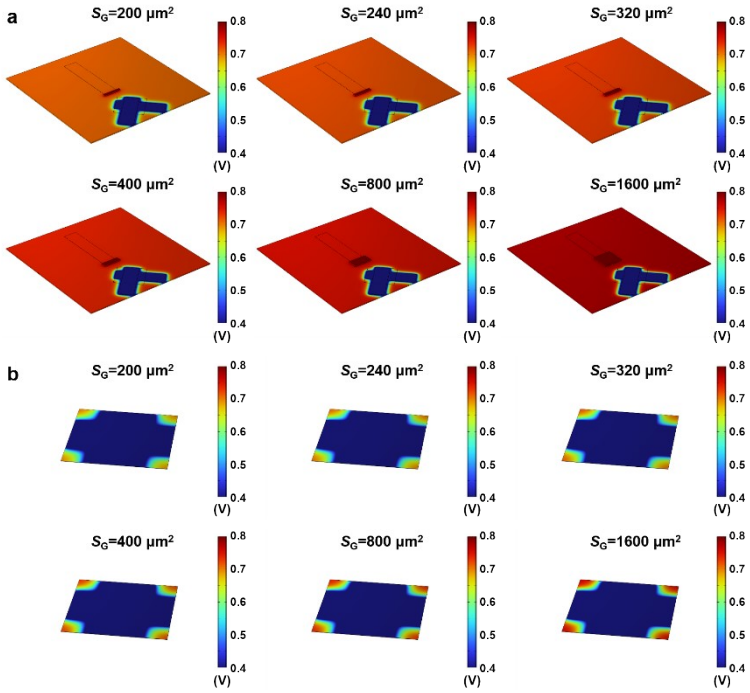

Figure S13. Electric field distribution simulation of Ag side gate vOECTs with varied S_G (200, 240, 320, 400, 800, 1600 μm²): (a) Device-scale potential distribution, (b)

Potential distribution across the channel region.

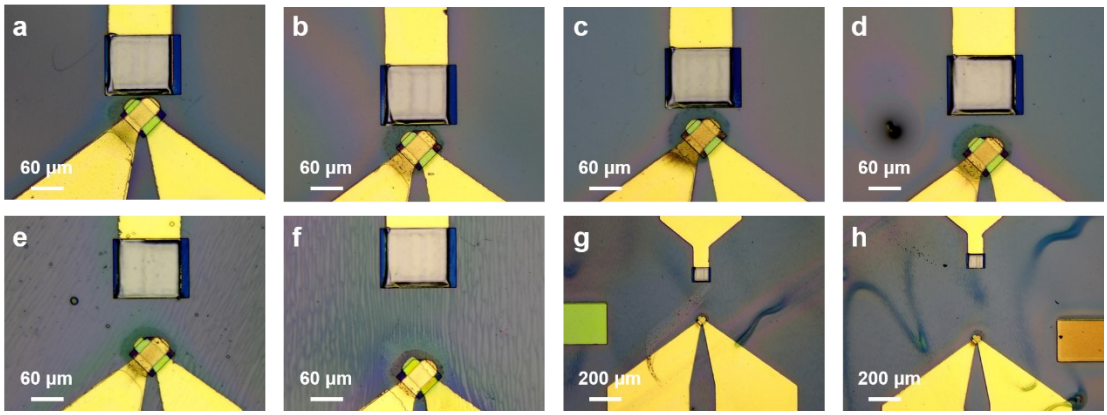

Figure S14. Optical microscopy images of printed vOECTs with varying D_{GC}: (a) 15 μm, (b) 20 μm, (c) 30 μm, (d) 50 μm, (e) 80 μm, (f) 120 μm, (g) 260 μm, (h) 500 μm.

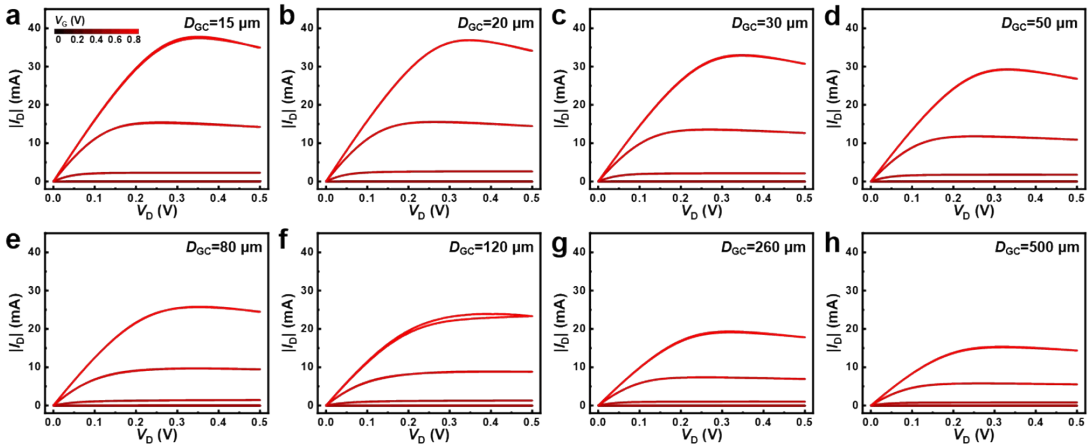

Figure S15. Output characteristics of the Homo-gDPP OECTs with different D_{GC}: (a) 15 μm, (b) 20 μm, (c) 30 μm, (d) 50 μm, (e) 80 μm, (f) 120 μm, (g) 260 μm, and (h) 500 μm.

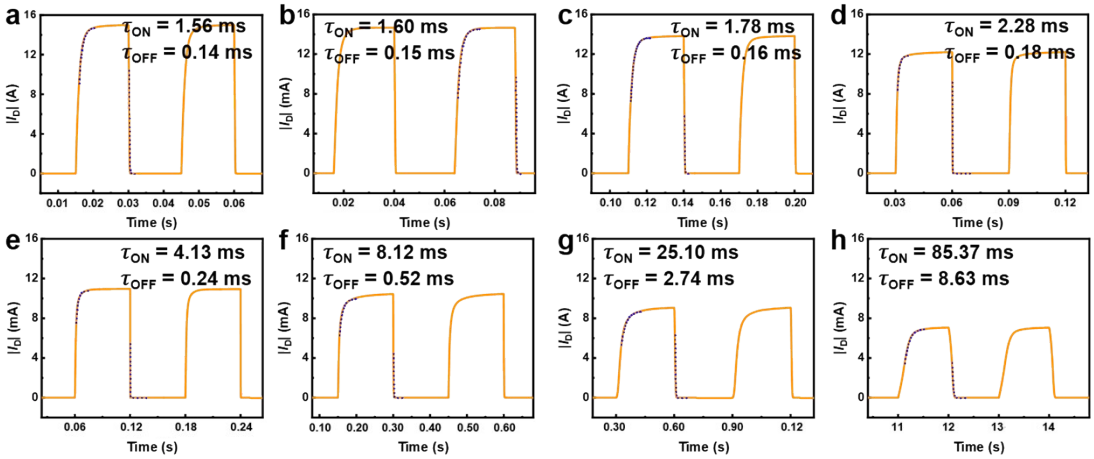

Figure S16. Transient response curves of printed Ag side-gate vOECTs with varying

D_{GC}: (a) 15 μm, (b) 20 μm, (c) 30 μm, (d) 50 μm, (e) 80 μm, (f) 120 μm, (g) 260 μm, (h) 500 μm (V_D=0.1 V, V_G=0-0.8 V).

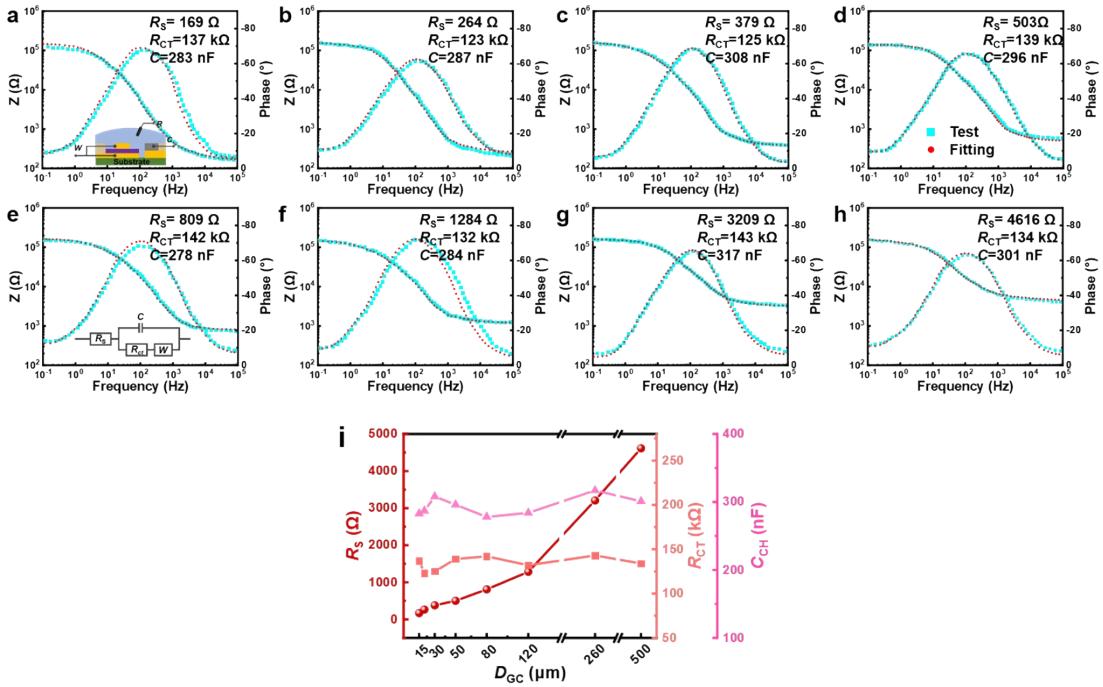

Figure S17. EIS measurements of printed Ag side-gate vOECTs with varying D_{GC}: (a) 15 μm, (b) 20 μm, (c) 30 μm, (d) 50 μm, (e) 80 μm, (f) 120 μm, (g) 260 μm, (h) 500 μm, (i) Extracted R_S, R_{CT}, and C_{CH} from the EIS characterization of printed Ag side-gate vOECTs with varying D_{GC}.

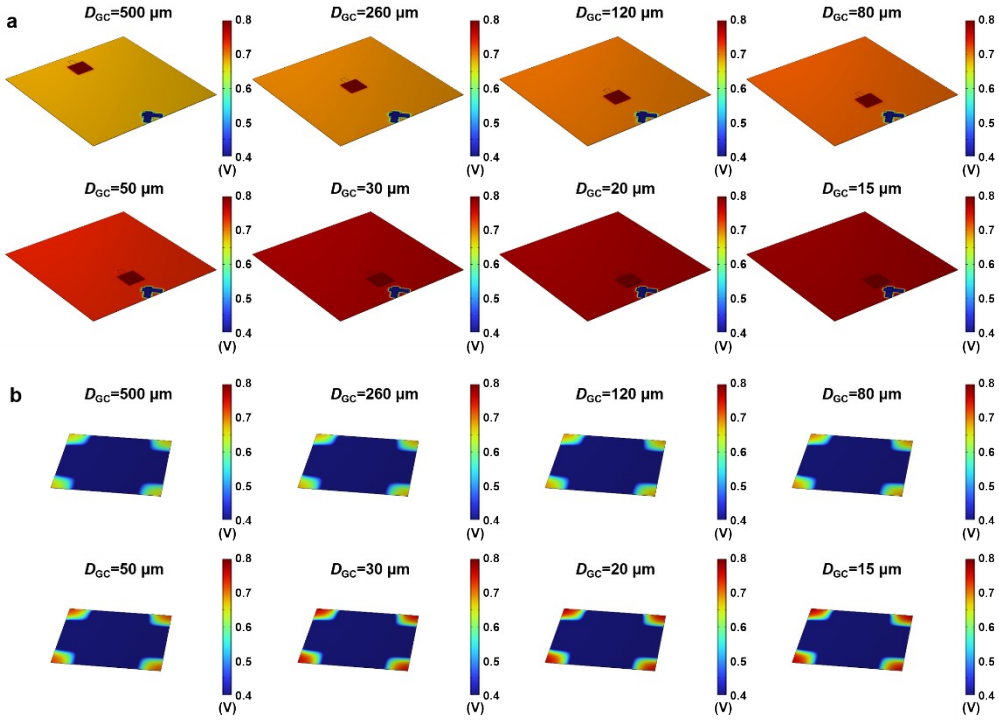

Figure S18. Electric field distribution simulation of Ag side gate vOECTs with varied

D_{GC} (500, 260, 120, 80, 50, 30, 20, 15 μm): (a) Device-scale potential distribution, (b) Potential distribution across the channel region.

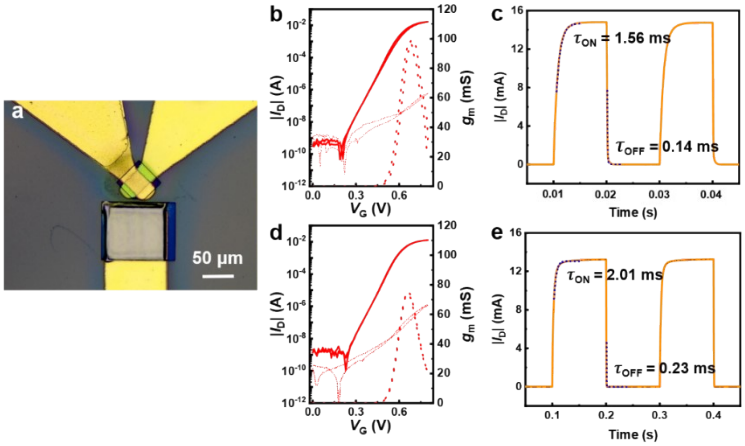

Figure S19. (a) Optical microscopy image of vOECT with an Ag side gate of 10,000 μm^2, (b,c) Transfer characteristics and transient response curves of the vOECT with a 10,000 μm^2 Ag side gate, (d,e) Corresponding transfer characteristics and transient response of the vOECT employing an Ag/AgCl floating gate (V_D=0.1 V, V_G=0-0.8 V).

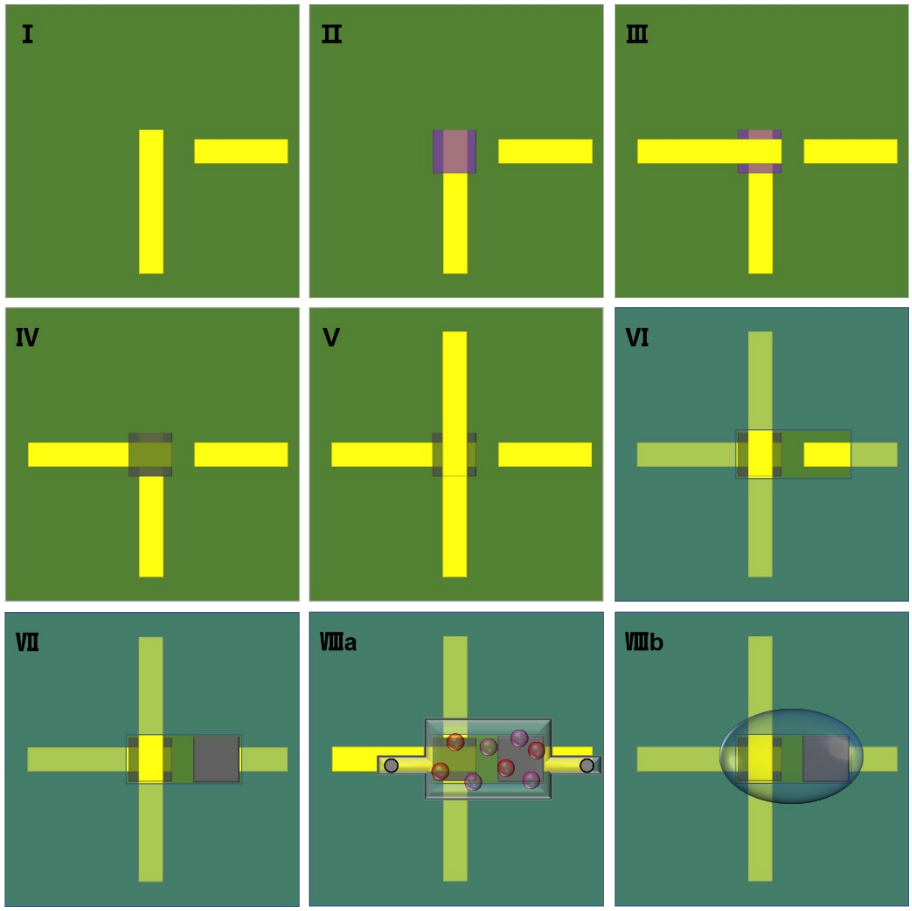

Figure S20. Fabrication process of the inverter with PDMS well or LiCl-PEG electrolytes. (I) Bottom electrode deposition, (II) N-type semiconductor deposition and patterning, (III) Middle electrode deposition, (IV) P-type semiconductor deposition and

patterning, (V) Top electrode deposition, (VI) Photoresist (SU8-2002) deposition and development, (VII) Ag gate electrode fabrication, (VIIIa) PDMS well and electrolyte (1 M LiCl) application, or (VIIIb) Electrolyte (LiCl-PEG) application.

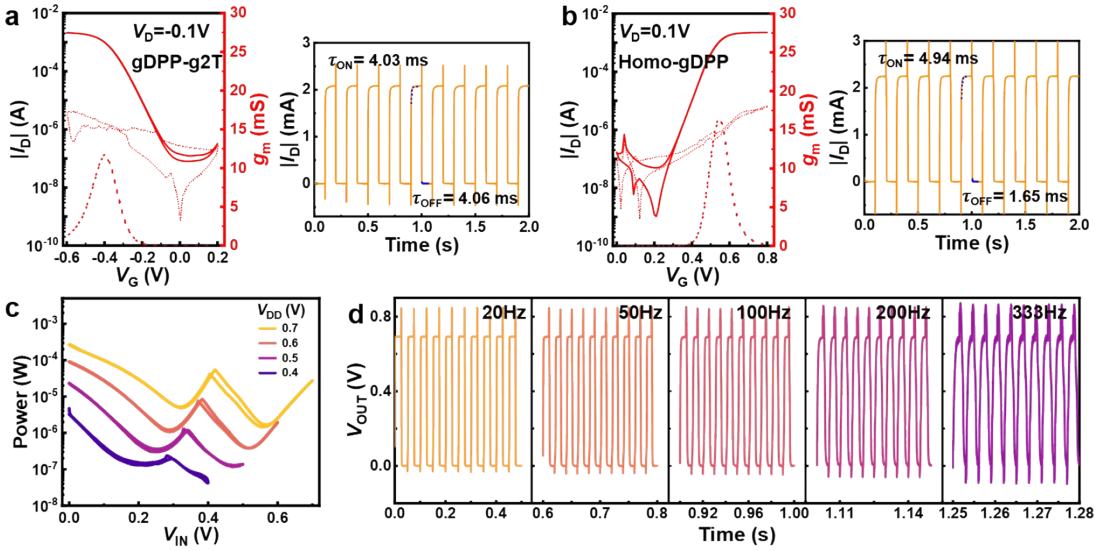

Figure S21. Performance characterization of the inverter with a PDMS well. (a,b) Electrical performance of p/n-type vOECTs in the inverter. (c) Power dissipation of the inverter. (d) Frequency response of the inverter where V_{IN} is 0-0.7 V square-wave input pulses.

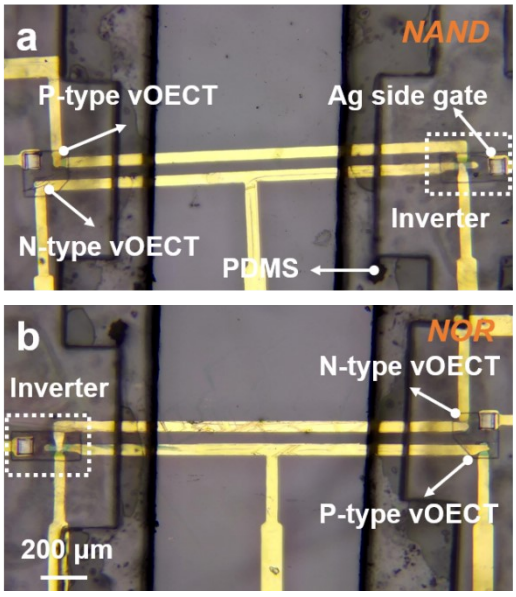

Figure S22. (a,b) Optical microscope images of the fabricated NAND and NOR gates with PDMS wells.

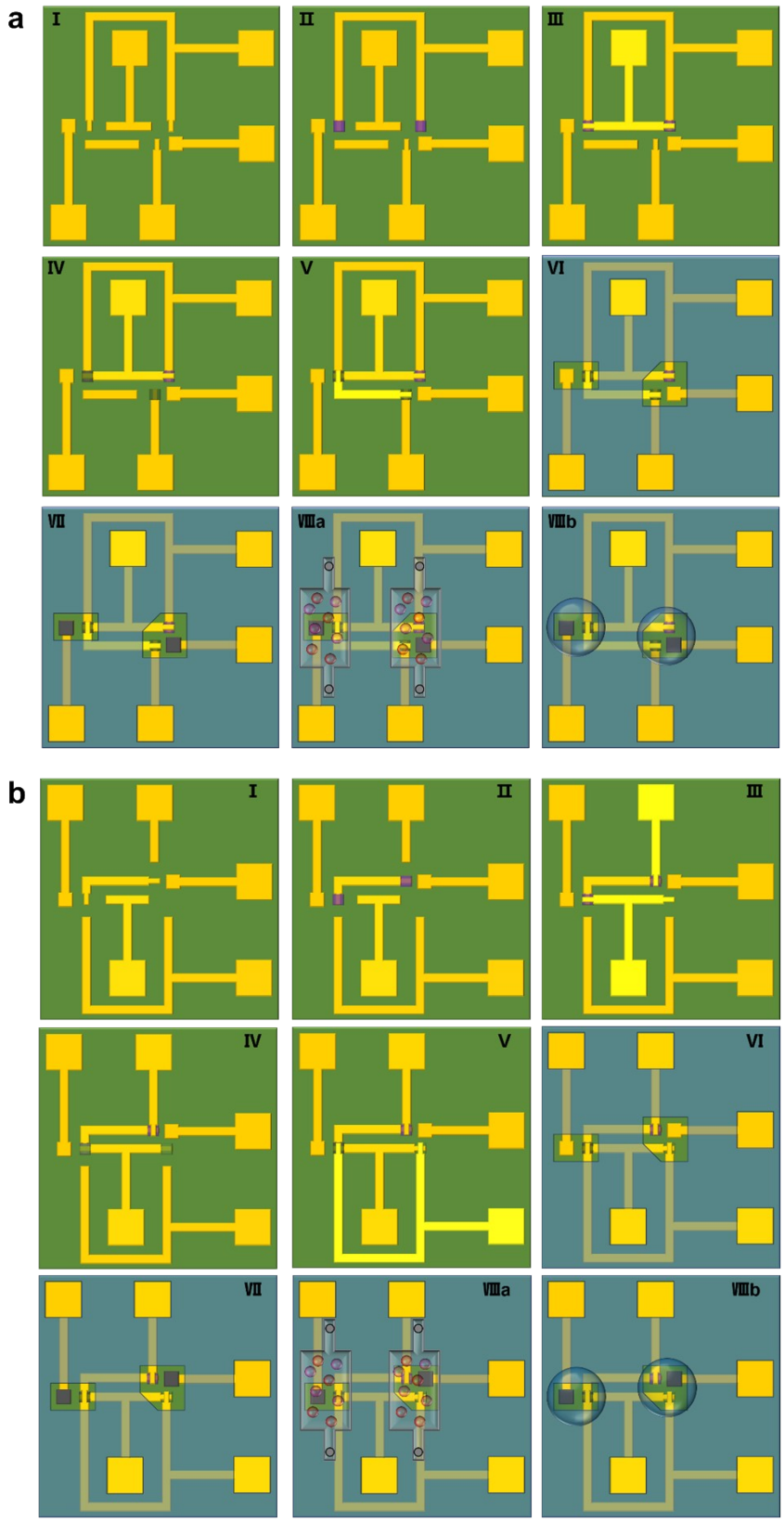

Figure S23. (a,b) Fabrication process of NAND and NOR gates with PDMS well or LiCl-PEG electrolyte. (I) Bottom electrode deposition, (II) N-type semiconductor deposition and patterning, (III) Middle electrode deposition, (IV) P-type semiconductor deposition and patterning, (V) Top electrode deposition, (VI) Photoresist (SU8-2002)

deposition and development, (VII) Ag gate electrode fabrication, (VIIIa) PDMS well and electrolyte (1 M LiCl) application, or (VIIIb) Electrolyte (LiCl-PEG) application.

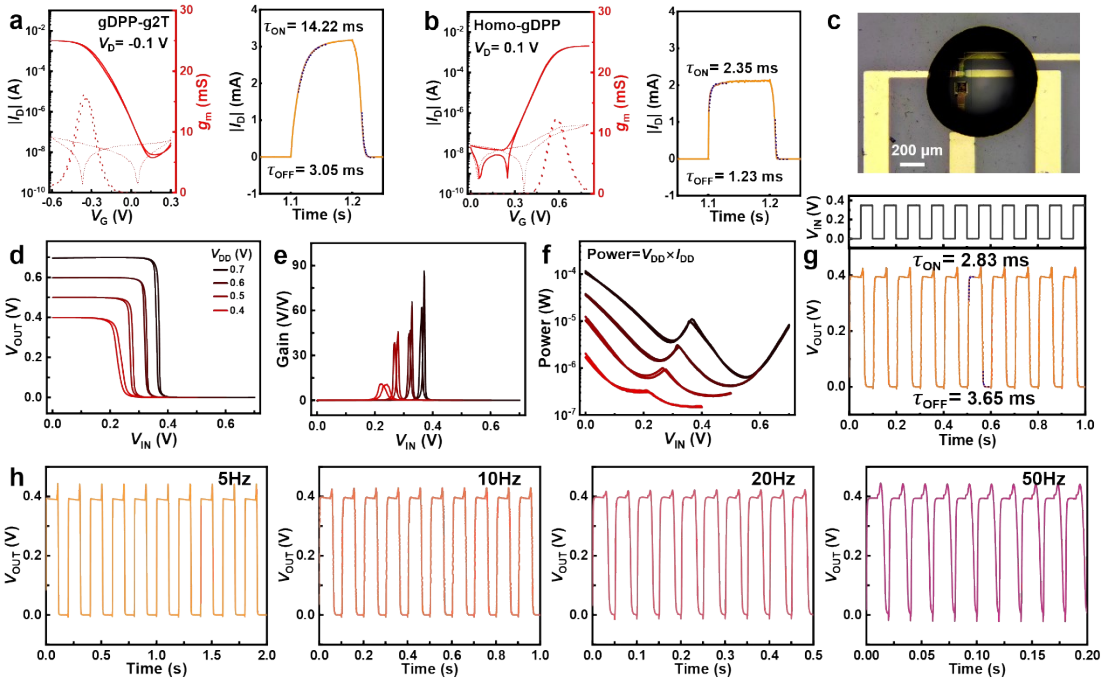

Figure S24. Performance characterization of the LiCl-PEG-based inverter. (a,b) Electrical performance of p/n-type vOECTs. (c-f) Optical microscopy images and electrical performance of the fabricated LiCl-PEG-based inverter. (g,h) Switching time and frequency response of the inverter where V_{IN} is a square-wave input pulse of 0-0.4 V.

P/n-type OECT maintained I_{ON} of 1.80±0.12/2.07±0.16 mA, along with balanced g_m of 10.07±0.09/15.64±1.03 mS, respectively (Figure S22a,b). Furthermore, both types of OECTs showed switching speed within 14 ms, along with symmetrical V_{ON} of -0.13 and 0.15 V obtained in p/n-type OECTs, respectively. Next, high-integrity complementary circuits are characterized.

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