Electronic Supplementary Information

Uncovering a Third Function of the Transistor Beyond Switching and Amplification: Coupled Photo-Responsive Oscillators for In-Sensor Computing

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Supplementary figures

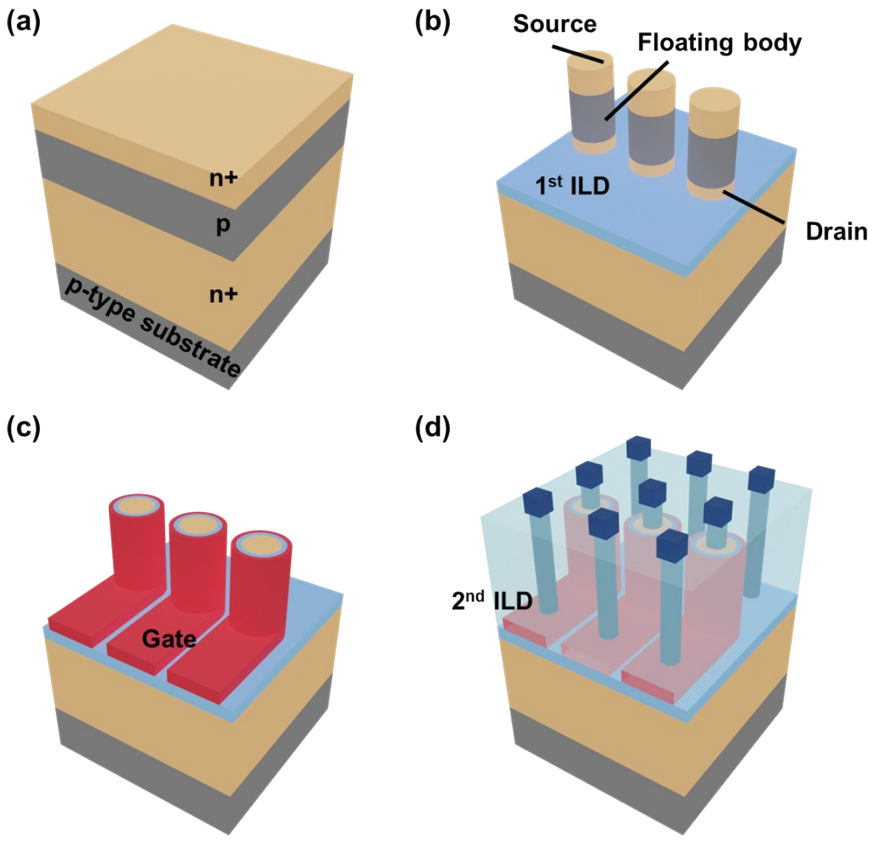

Figure S1. Fabrication of photo-responsive oscillators (PROs). (a) A three-step iterative ion implantation process was conducted on a (100) bulk Si wafer. The top of the silicon pillar serves as the source (S), the middle portion is designated as the floating body (FB), and the bottom of the pillar functions as the drain (D). The drain region with a deep depth was heavily doped through high energy implantation with a high dose of phosphorus (500 keV and 3×10^{14} cm^{-2}). The body region with an intermediate depth was moderately doped through medium energy implantation with a moderate dose of boron (100 keV and 4×10^{13} cm^{-2}). The source region with a shallow depth was heavily doped through low energy implantation with a high dose of arsenic

(80 keV and 3×10^{15} cm^{-2}). The dopants were activated through rapid thermal annealing (RTA). (b) Vertical Si pillars were patterned by photolithography and plasma etching. The channel length, defined by the pillar height (H_p) between the n^+ S and the n^+ D, was fixed at 700 nm across the wafer. the channel width (W) is controlled by the pillar diameter (D_p), which ranges from 400 nm to 5000 nm; accordingly, the channel perimeter, given by πD_p, corresponds to W. The first interlayer dielectric (1st ILD), which is analogous to the shallow trench isolation (STI) in conventional planar-typed CMOS technology, was then deposited with a thickness of 100 nm to isolate adjacent PROs. (c) Gate dielectric layers with an equivalent oxide thickness (EOT) of approximately 13 nm and a conformal poly-Si gate with a thickness of 260 nm were sequentially deposited to wrap around the vertical pillars. (d) A second ILD layer (2nd ILD) with a thickness of 800 nm was deposited to isolate the PROs and the overlying interconnection metal lines. Metal contact holes were defined by photolithography and plasma etching, followed by sequential deposition of titanium (Ti), titanium nitride (TiN), and tungsten (W). Finally, all the metal layers were patterned for interconnections using another photolithography and plasma etching.

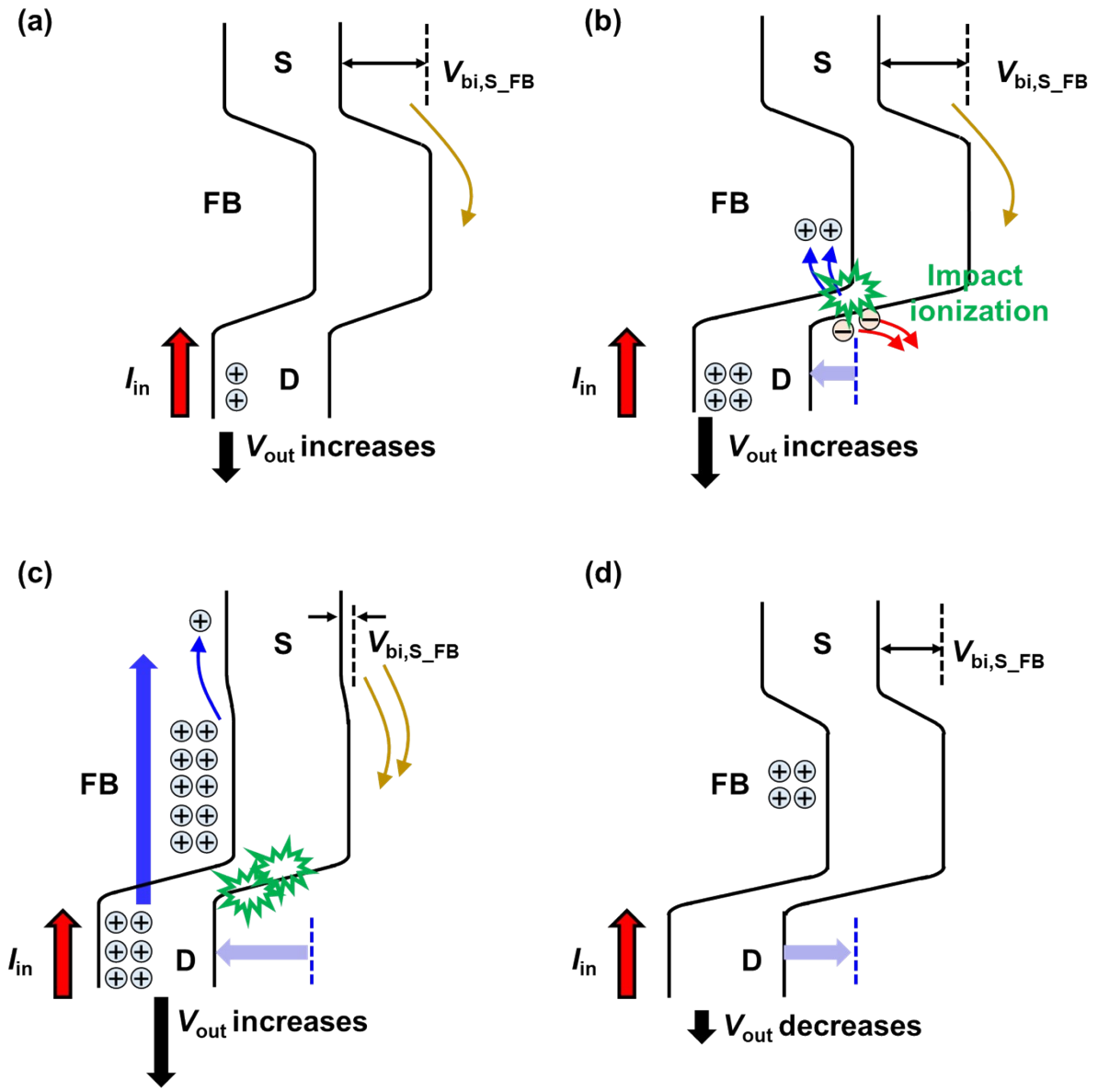

Figure S2. Oscillation mechanism with energy band diagrams. (a) When a constant input current (I_{in}) is applied to the drain (D) of the PRO in high-resistance state (HRS), positive charges accumulate at a parasitic capacitance (C_{par}), which includes contributions from the drain capacitance, probing pad capacitance, and measurement equipment capacitance with cable capacitance. (b) As the output voltage (V_{out}) at the D increases, electrons that overcome the built-in potential barrier (V_{bi,S_FB}) formed at the n^+ source (S) and the p-type floating body (FB) are injected from the S. Those electrons trigger impact ionization (*I.I*) near the D junction, generating electron-hole pairs. While the electrons move toward the D, the generated holes are temporarily stored in the FB. These holes lower the V_{bi,S_FB}, causing more electrons to be injected from the S to the FB. This process corresponds to the charging process. (c) When V_{out} reaches the latch-up voltage (V_{LU}), C_{par} is rapidly discharged due to a sudden transition from the HRS to the low-resistance state (LRS). This transition is known as the single transistor latch

(STL) process, during which the holes temporarily stored in the FB are concurrently released. This process corresponds to the discharging process. (d) The PRO automatically returns to the HRS after the abrupt discharging, completing one oscillation cycle. The next charging and discharging cycle begin and continue to repeat. To this end, oscillating output (V_{out}) is generated as long as the constant I_{in} is applied to the D.

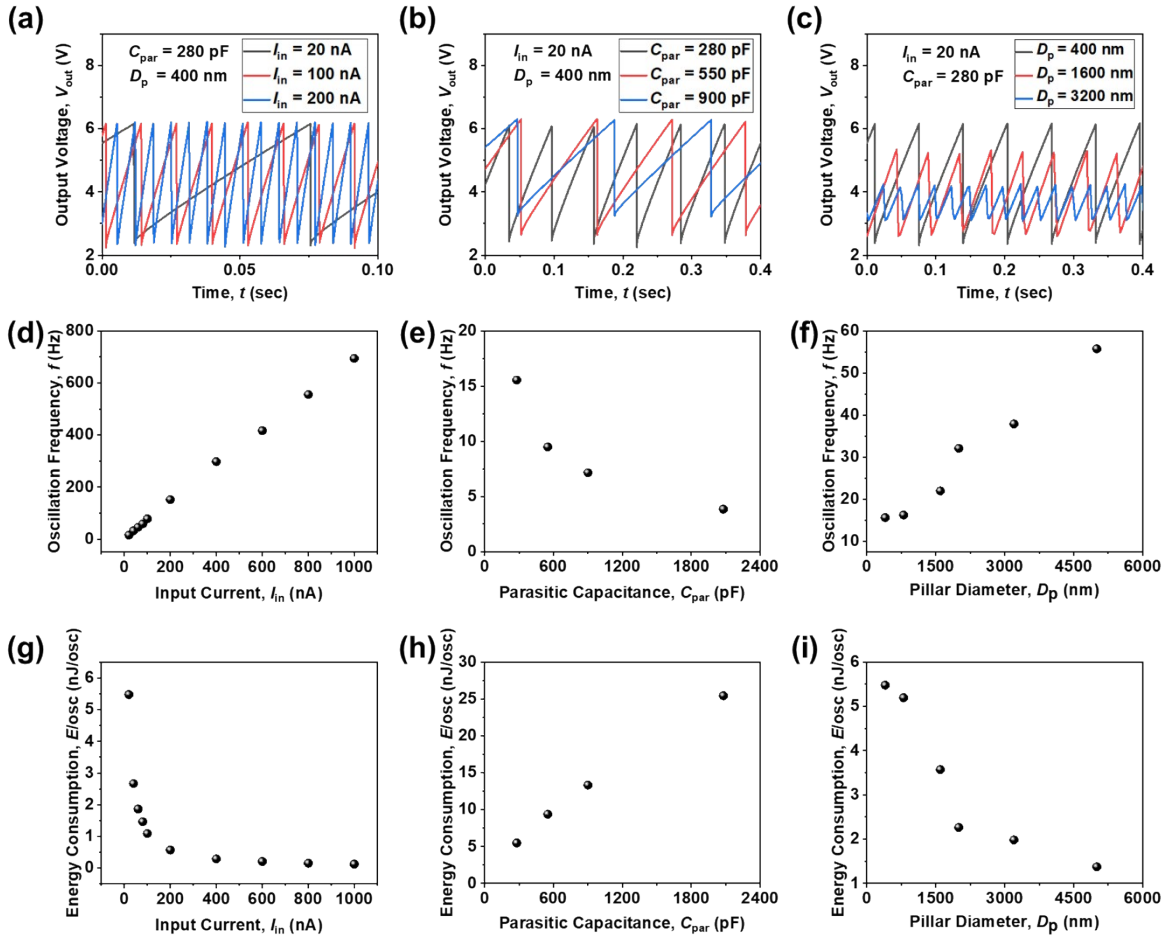

Figure S3. Measured oscillation characteristics from the PRO for various I_{in}, C_{par}, and D_p. (a) Measured oscillating V_{out} for different I_{in}. (b) Measured oscillating V_{out} for different C_{par}. (c) Measured oscillating V_{out} for different D_p. (d) Extracted oscillation frequency (f) according to I_{in}. (e) Extracted f according to C_{par}. (f) Extracted f according to D_p. (g) Estimated energy consumption per oscillation (E/osc) according to I_{in}. (h) Estimated E/osc according to C_{par}. (i) Estimated E/osc according to D_p.

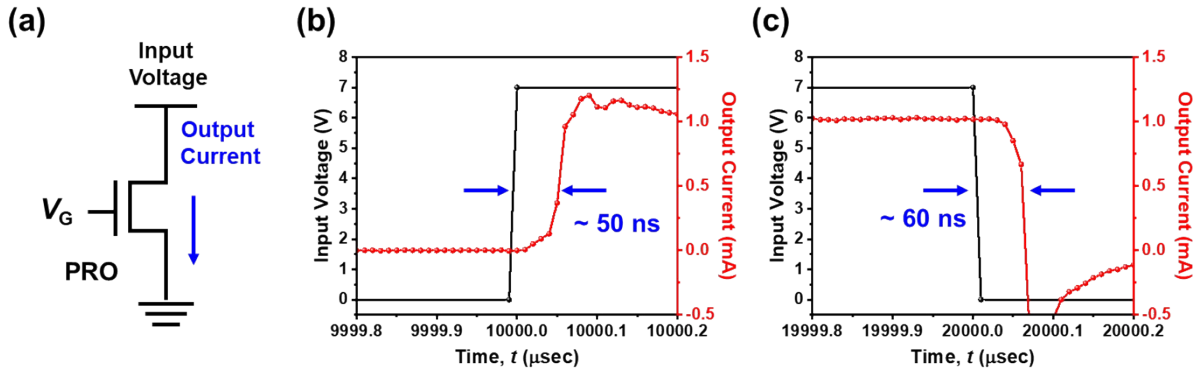

Figure S4. **Measured switching speed of the PRO.** (a) Circuit diagram used to measure the switching speed of PRO. Input voltage with a trapezoidal pulse was applied to a PRO, and output current was measured. (b) Switching delay when the PRO transitions from HRS to LRS, corresponding to the rising-up period. (c) Switching delay when the PRO transitions from LRS to HRS, corresponding to the falling-down period.

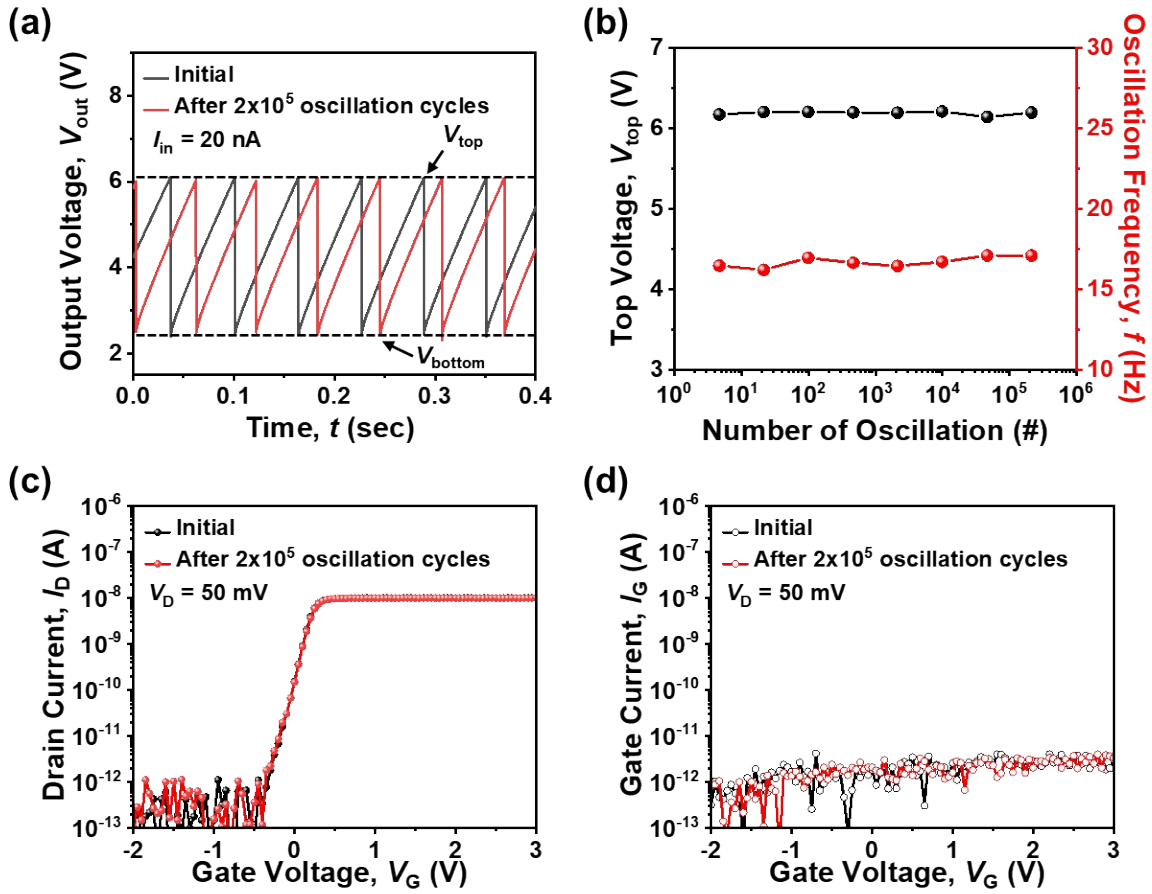

Figure S5. Endurance evaluation based on a comparison of measured I_D, V_T, and I_G before and after 2 × 10⁵ oscillation cycles in the PRO. (a) Comparison of the measured oscillation characteristics. (b) Extracted V_{top} and f from (a) according to the number of oscillations. (c) Comparison of the measured I_D according to V_G. (d) Comparison of the measured I_G according to V_G.

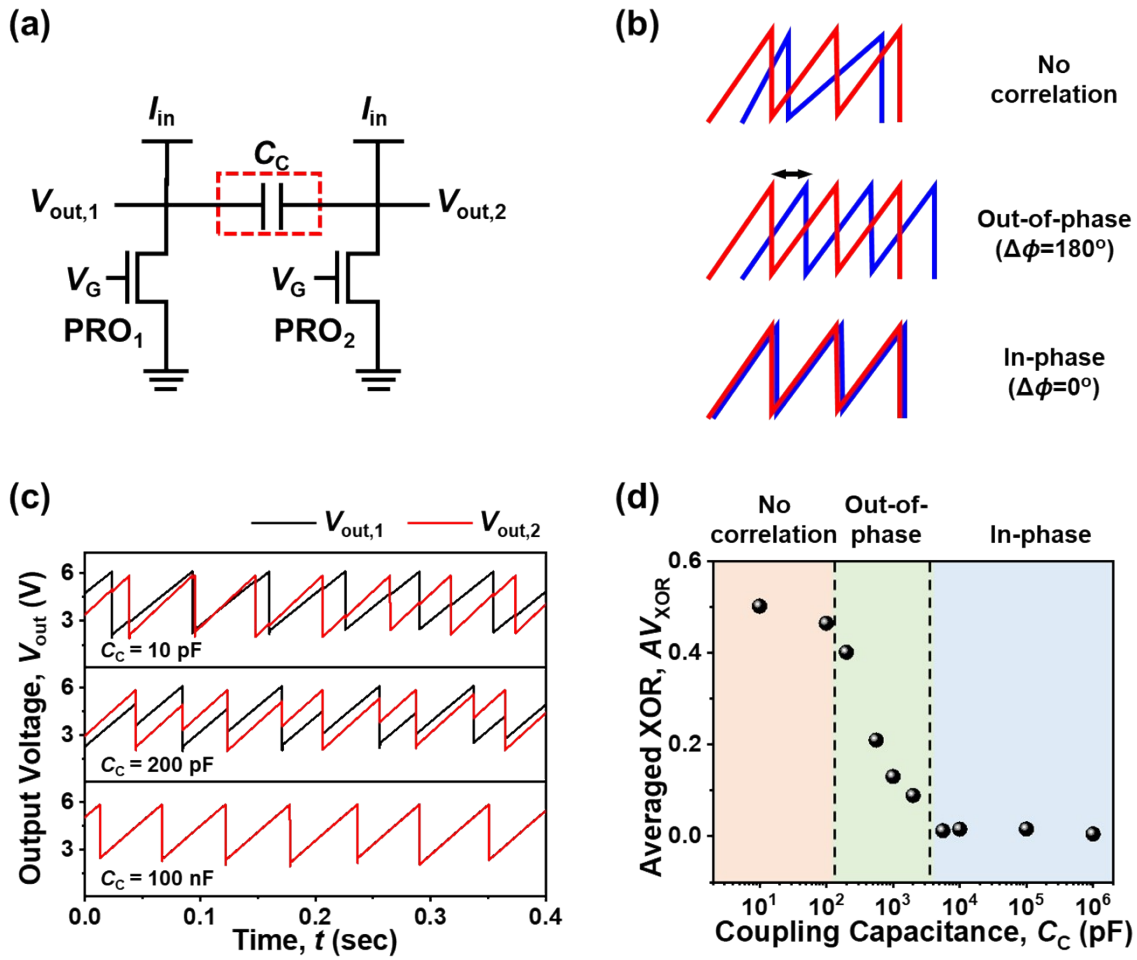

Figure S6. Synchronization behaviors of the coupled twin PROs (CT-PROs) without light illumination. (a) Circuit diagram of the CT-PROs through a coupling capacitor C_C. (b) Schematic illustration of three types of synchronization behavior in CT PROs: no correlation, out-of-phase synchronization, and in-phase synchronization. (c) Oscillating output voltages ($V_{out,1}$ and $V_{out,2}$) for various C_C. (d) Averaged XOR (AV_{XOR}) values for various C_C.

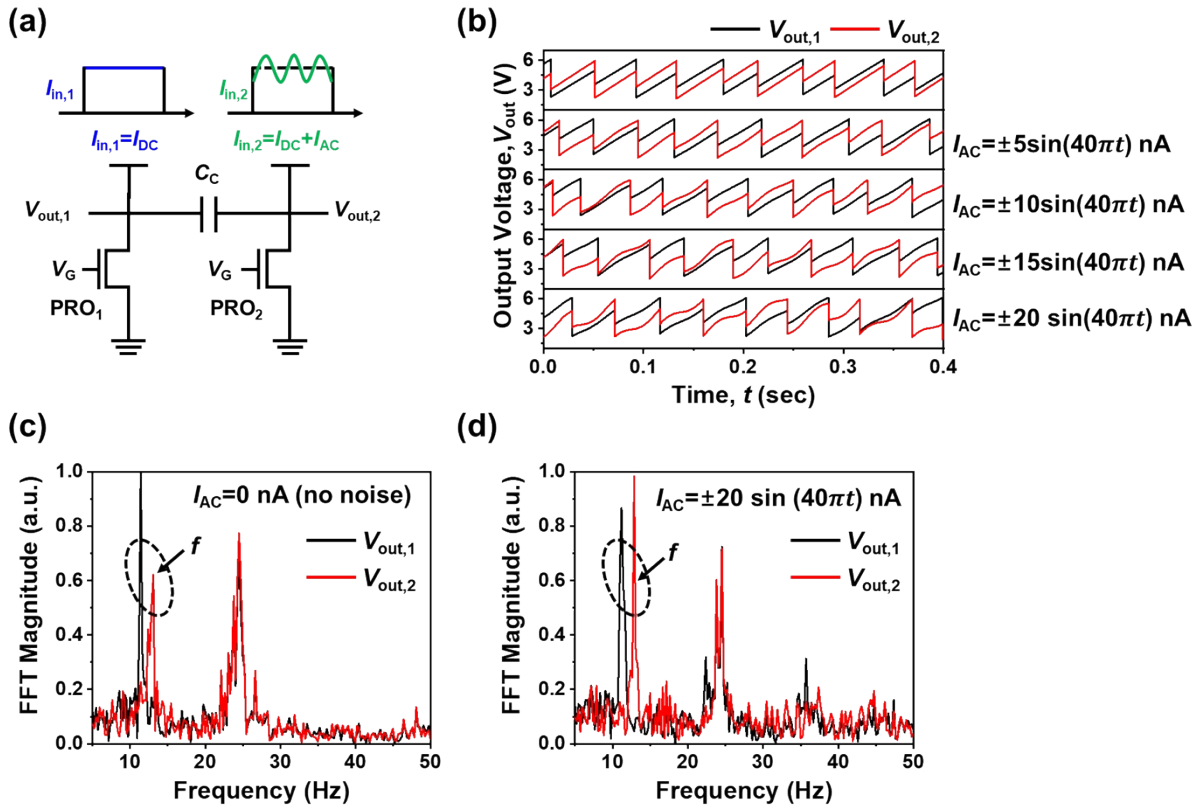

Figure S7. Noise-resilient CT-PROs against sine-wave noise and their measured synchronization characteristics. (a) Circuit diagram of the CT-PROs, where I_{DC} is applied to PRO_1 and I_{AC} with a sine-wave superimposed on the same I_{DC} is applied to PRO_2. (b) Measured $V_{out,1}$ and $V_{out,2}$ from the CT-PROs for different amplitudes of I_{AC} under the fixed frequency of 20 Hz. (c) Fast Fourier transform (FFT) spectra of $V_{out,1}$ and $V_{out,2}$ in the absence of I_{AC} (*i.e.*, without noise). (d) FFT spectra of $V_{out,1}$ and $V_{out,2}$ in the presence of I_{AC} (*i.e.*, with noise). Out-of-phase synchronization is robustly maintained regardless of the noise amplitude, demonstrating the high noise immunity of the CT-PROs.

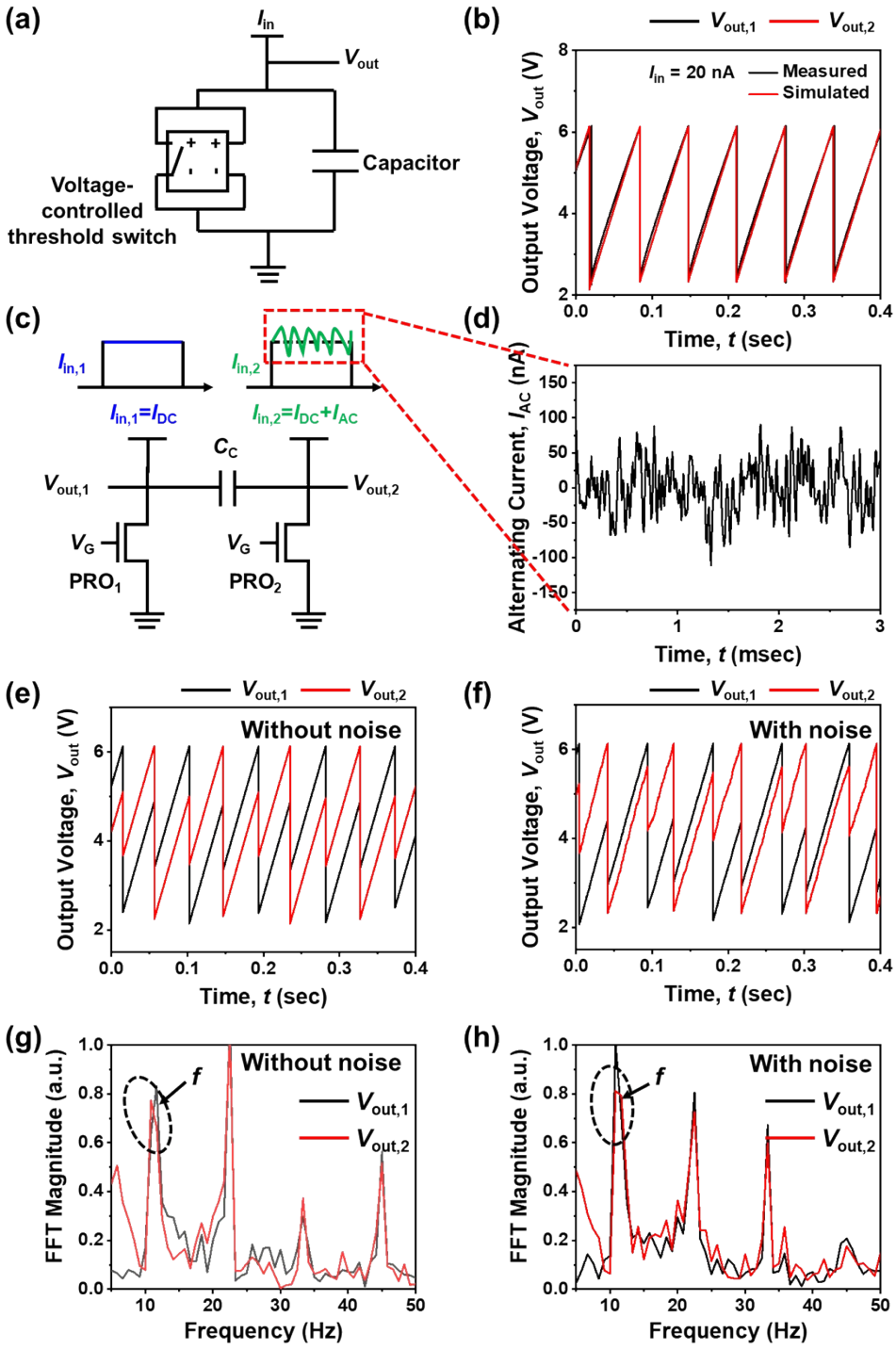

Figure S8. Noise-resilient CT-PROs against randomly fluctuating noise and their simulated synchronization characteristics. (a) Equivalent circuit model of the PRO used for SPICE circuit simulation. (b) Comparison of measured and simulated oscillation characteristic of the PRO for cross-calibration. (c) Circuit diagram of the CT-PROs, where I_{DC} is applied to PRO_1 and I_{AC} with randomly fluctuating noise superimposed on the same I_{DC} is applied to PRO_2. (d) Waveform of randomly fluctuating noise generated from the SPICE simulator. (e) Simulated $V_{out,1}$ and $V_{out,2}$ of the CT-PROs without the random noise. (f) Simulated $V_{out,1}$ and $V_{out,2}$ of the CT-PROs with the random noise. (g) FFT spectra of (e). (h) FFT spectra of (f).

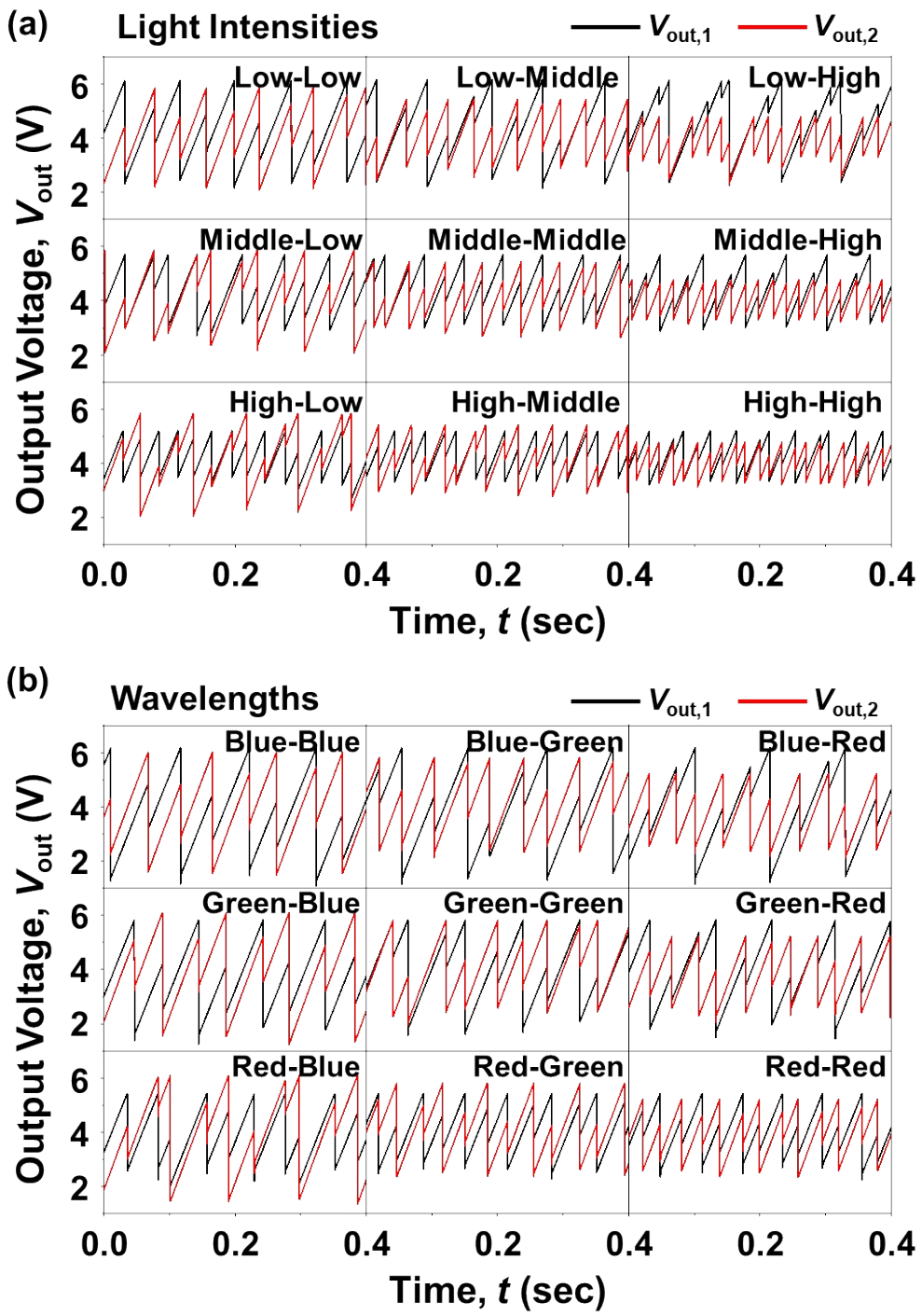

Figure S9. **Analyses of synchronization in the CT-PROs under independent sets of 9 I_L and 9 λ conditions.** (a) Measured $V_{out,1}$ and $V_{out,2}$ characteristics for various I_L (low, middle, high). **(b)** Measured $V_{out,1}$ and $V_{out,2}$ characteristics for various λ (red, green, blue).

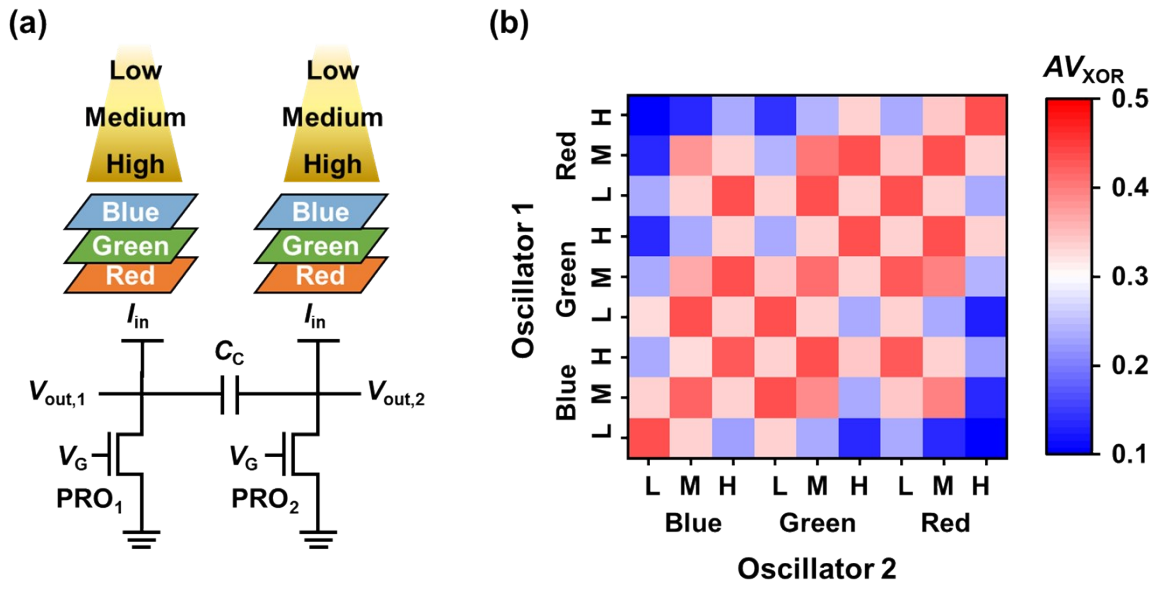

Figure S10. Analyses of synchronization in the CT-PROs under 81 cross-combinations of I_L and λ. (a) Circuit diagram of the CT-PROs for various I_L and λ. (b) Heatmap of the AV_{XOR} value for 9×9 combinations.

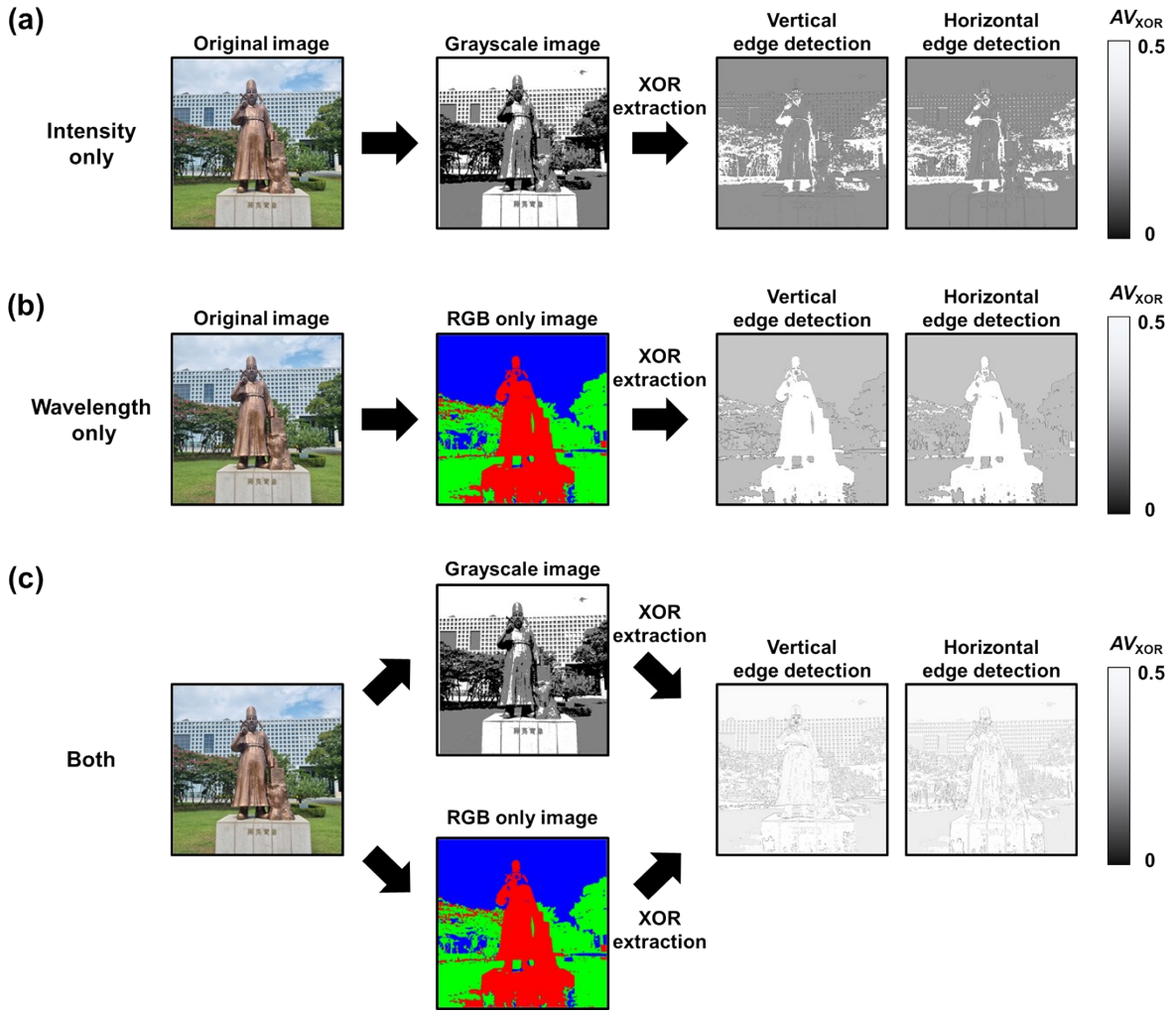

Figure S11. Image processing with edge detection for three scenarios: I_L variations, λ variations, and combined variations. (a) Edge detection images for I_L variations. (b) Edge detection images for λ variations. (c) Edge detection images for I_L and λ variations.

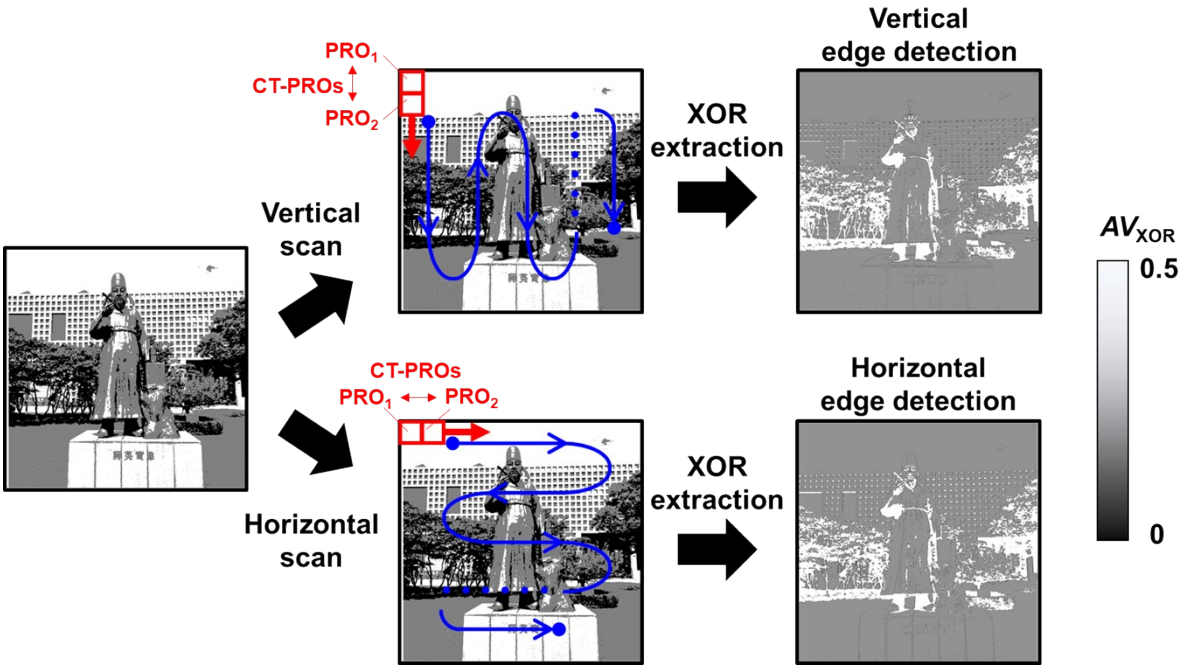

Figure S12. Comparison of minimum scanning unit (CT-PRO) in horizontal and vertical directions.

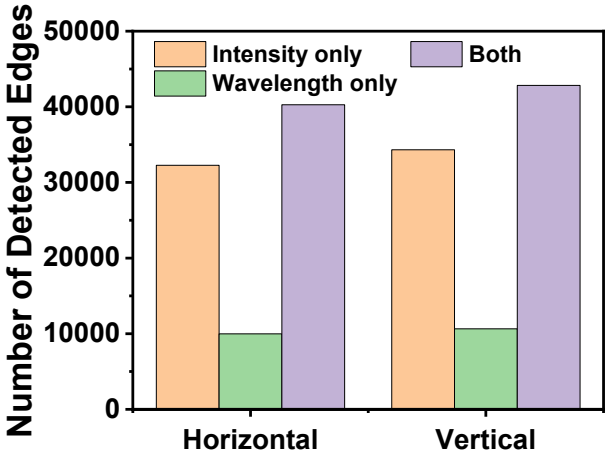

Figure S13. Comparison of the number of the detected edges along with the horizontal and vertical scanning for three scenarios: I_L variations, λ variations, and combined variations. When considering both I_L and λ, the CT-PRO detected the highest number of edges.

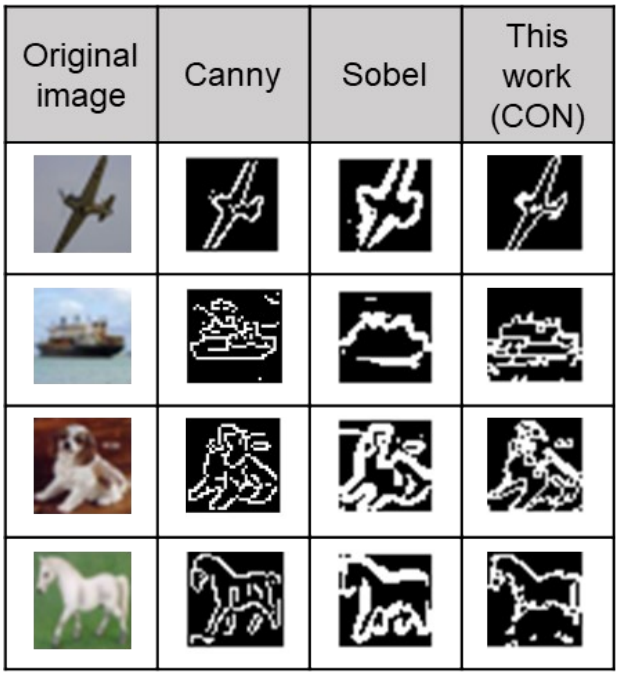

Figure S14. Edge maps generated using the Canny algorithm, Sobel algorithm, and CON composed of the CT-PROs.

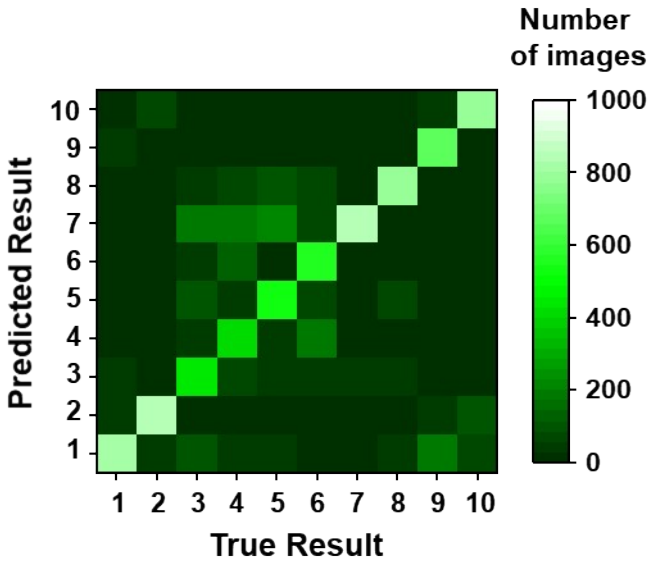

Figure S15. Confusion matrix for the classification of the CIFAR-10 dataset using the one-stream CNN.

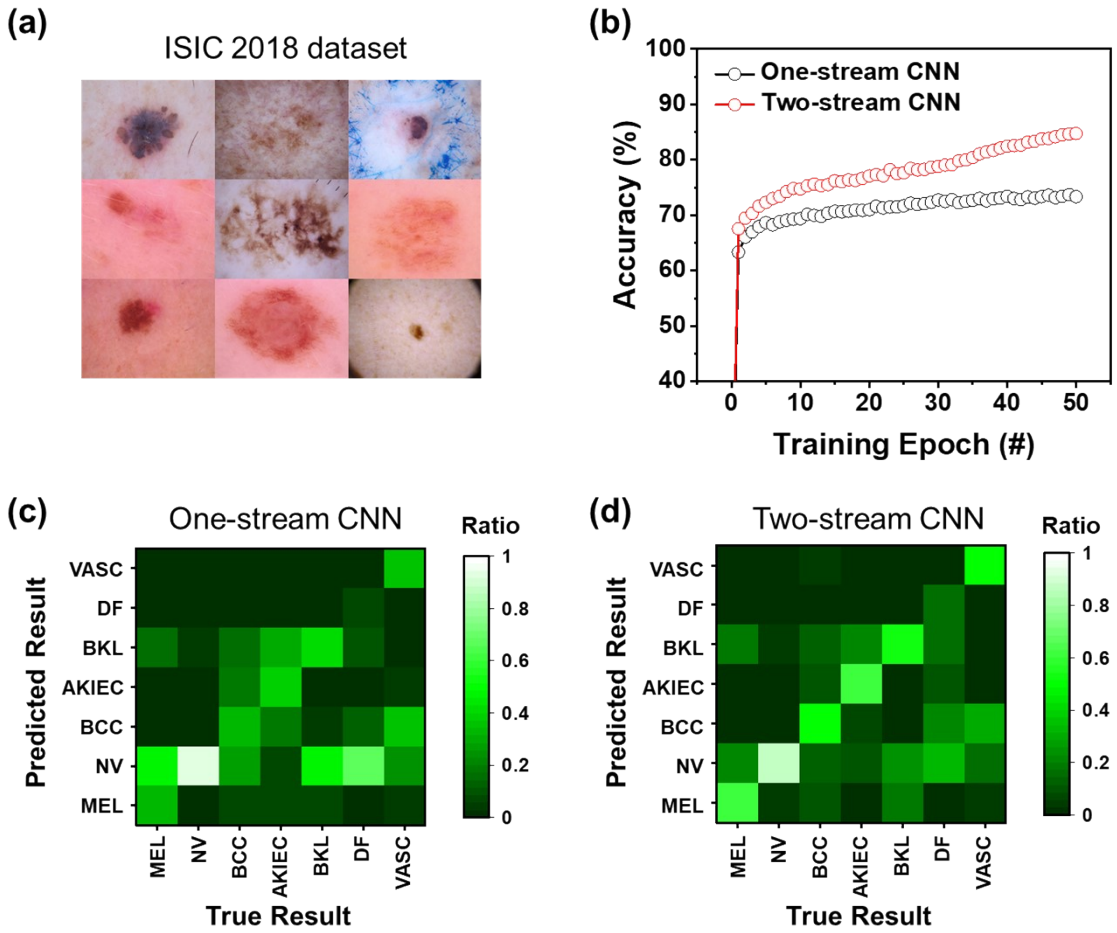

Figure S16. Classification of dermoscopic images in the ISIC 2018 dataset. (a) Example images of the ISCI 2018 dataset. (b) Classification accuracy over the number of epochs. Samples of the dermoscopic images from the ISIC 2018 dataset are shown in the inset. (c) Confusion matrix of classification results using the one-stream CNN. Since the number of images per class is imbalanced, the confusion matrix is normalized by the number of samples in each true class to allow an intuitive comparison of accuracy. (d) Confusion matrix of classification results using the two-stream CNN.

Supplementary Table

Class number	Class name
1	Airplane
2	Automobile
3	Bird
4	Cat
5	Deer
6	Dog
7	Frog
8	Horse
9	Ship
10	Truck

Table S1. Summarized table of classes in CIFAR-10 dataset.

Stream for original images		
Layer type	**Output size**	**Kernel**
Input	64×64×3	-
Convolution	64×64×32	(3×3, 32)
Max pooling	32×32×32	(2×2)
Convolution	32×32×64	(3×3, 64)
Max pooling	16×16×64	(2×2)
Convolution	16×16×128	(3×3, 128)
Global average pooling	1×1×128	-
Fully-connected (128→256)	1×1×256	-
Stream for edge maps		
Layer type	**Output size**	**Kernel**
Input	64×64×3	-
Convolution	64×64×32	(3×3, 32)
Max pooling	32×32×32	(2×2)
Convolution	32×32×64	(3×3, 64)
Max pooling	16×16×64	(2×2)
Convolution	16×16×128	(3×3, 128)
Global average pooling	1×1×128	-
Fully-connected (128→128)	1×1×128	-
Sigmoid (weight)	1×1×128	-
Fusion and output		
Layer type	**Output size**	**Kernel**
Concatenation	1×1×512	-
Dropout	1×1×512	-
Fully-connected (512→10)	1×1×10	-
Softmax	1×1×10	-
Classification	-	-

Table S2. Detailed information of the whole two-stream CNN.

Ref.	S1	S2	S3	S4	**This work**
Oscillator type	Circuit + FPGA	4 Transistors + 2 Capacitors	NbO2 IMT + Resistor	VO2 IMT + Resistor	**1 Transistor**
Footprint area	-	5027 μm^2	100 μm^2	-	**0.125 μm^2**
CMOS compatibility	High	High	Low	Low	**Very high**
Scalability	Low	High	High	High	**Very high**
Power consumption	~ mW	-	-	13 µW	**85.1 nW**
Frequency	2.73 MHz	0.35 MHz	0.3 MHz	31 MHz	**9.09 MHz**
In-sensor computing capability	No	No	No	No	**Yes**
Sensing information	Intensity	Intensity	Intensity	Intensity	**Intensity and wavelength**

Table S3. **Comparison with previously reported oscillators for visual recognition.** This work demonstrates, for the first time, a single-device oscillator with in-sensor computing capability.

References

S1 M. Abernot, T. Gil, A. Todri-Sanial, *Proc. Neuro-Inspired Comput. Elements Conf.* 2022, 13–21.

S2 E. Yu, A. Agrawal, D. Zheng, M. Si, M. Koo, P. D. Ye, S. K. Gupta, K. Roy, *IEEE Electron Device Lett.* 2021, **42**, 1670–1673.

S3 H. W. Kim, S. Jeon, H. Kang, E. Hong, N. Kim, J. Woo, *IEEE Trans. Electron Devices* 2023, **70**, 3031–3036.

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