

Supplementary Information

Optically Controlled Synaptic device based on PdSe₂ / α -In₂Se₃ vdW Heterostructure FET

Anurag Ghosh, Inbar Dahan, Bisweswar Santra, Gautham Vijayan, Michael Uzhansky and Elad Koren*

Nanoscale Electronic Materials and Devices Laboratory, Faculty of Materials Science and Engineering, Technion - Israel Institute of Technology, Haifa 3200003, Israel.

*eladk@technion.ac.il

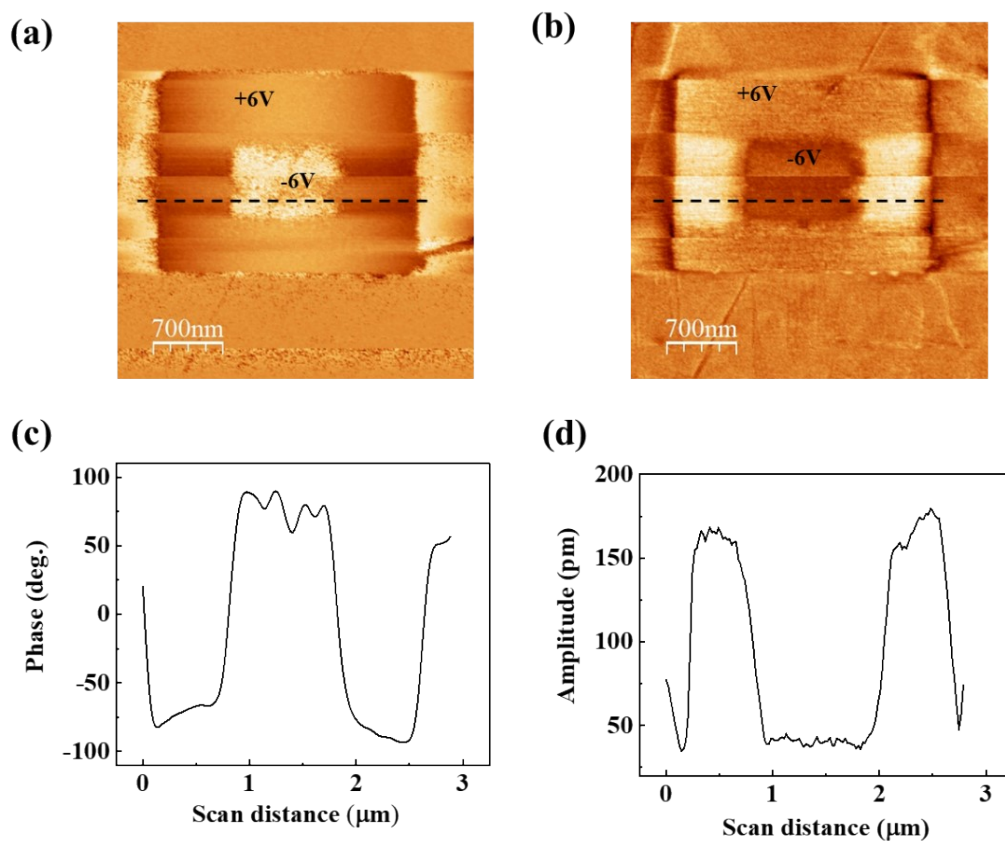


Figure S1: (a) PFM phase and (b) amplitude images after poling two squared areas with +/- 6V. (c) The corresponding line profile of phase and (d) amplitude across the black dotted line. For PFM analysis, a 30 nm thick In₂Se₃ was directly exfoliated over a 50/5 nm Au/Cr film deposited over 300 nm SiO₂-Si wafer.

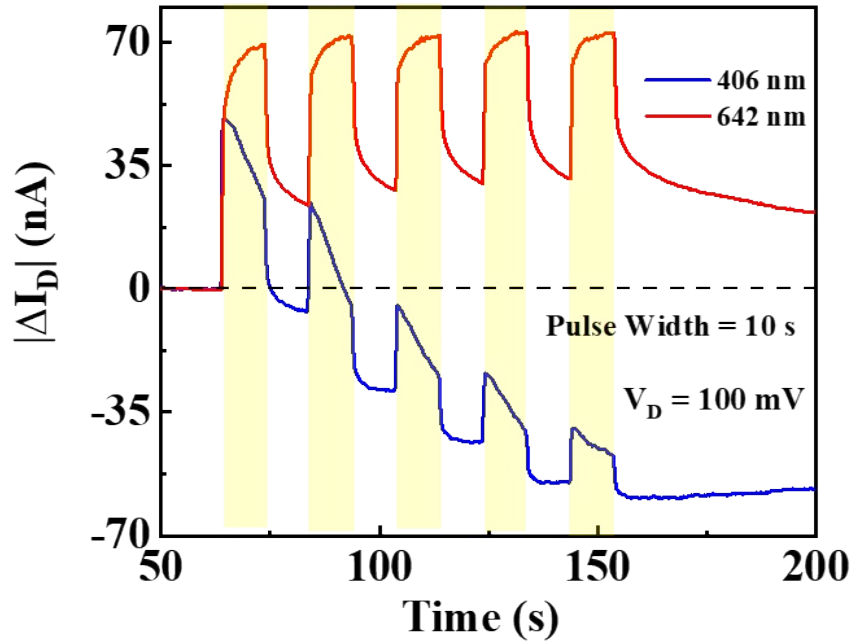


Figure S2: I_D - t measurements with 642 nm and 406 nm with 10 s of pulse duration. 642 nm excitation shows potentiation trend, whereas 406 nm excitation shows depression trend with an instant PPC effect followed by a gradual decrease in current showing NPC.

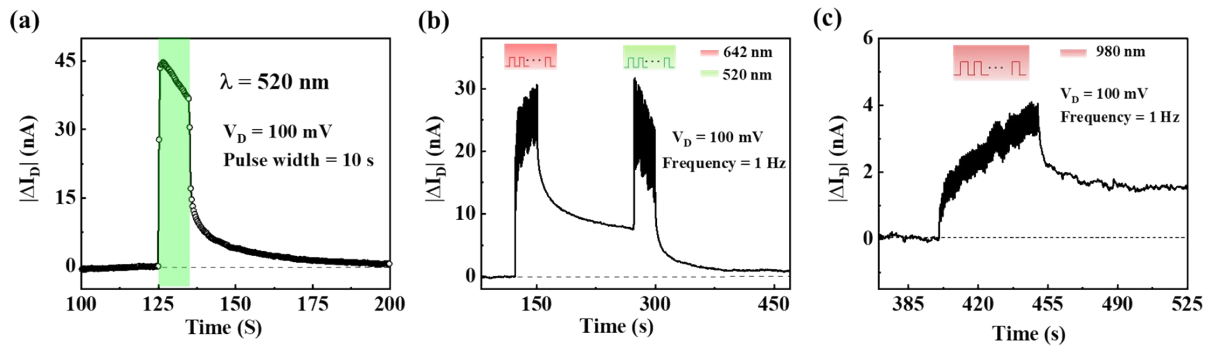


Figure S3: (a) Similar depression trend under 520 nm light pulse (Pulse width = 10 s). (b) Excitatory synaptic response under 642 nm followed by inhibitory response under 520 nm (Frequency = 1 Hz). (c) Excitatory synaptic response under 980 nm light Pulse (Frequency = 1 Hz).

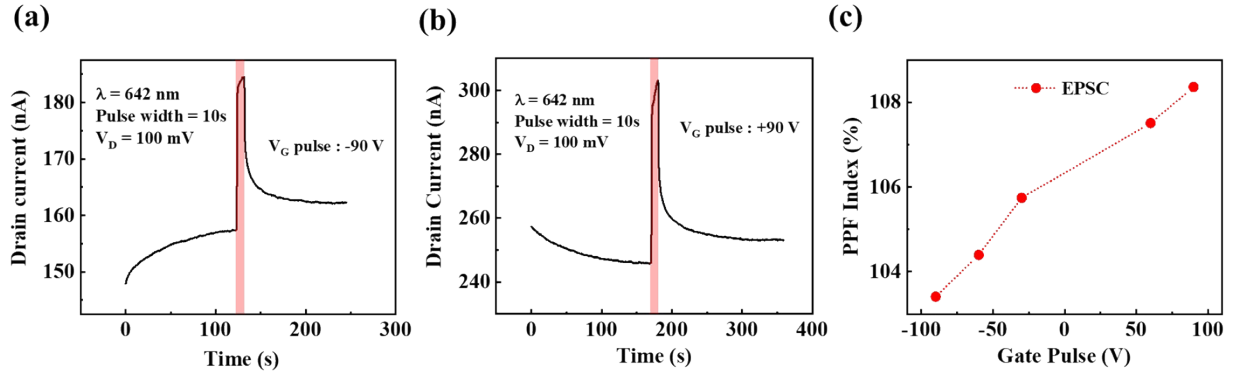


Figure S4: $I_D - t$ measurement following (a) -90 V and (b) +90 V gate actuation (executed at time = 0) showing the stabilized initial current level after waiting for ~ 2 -3 min (red box indicates the light pulse). (c) PPF index of EPSC versus gate actuation. ($\Delta t = 10$ s, Pulse duration = 1 s).

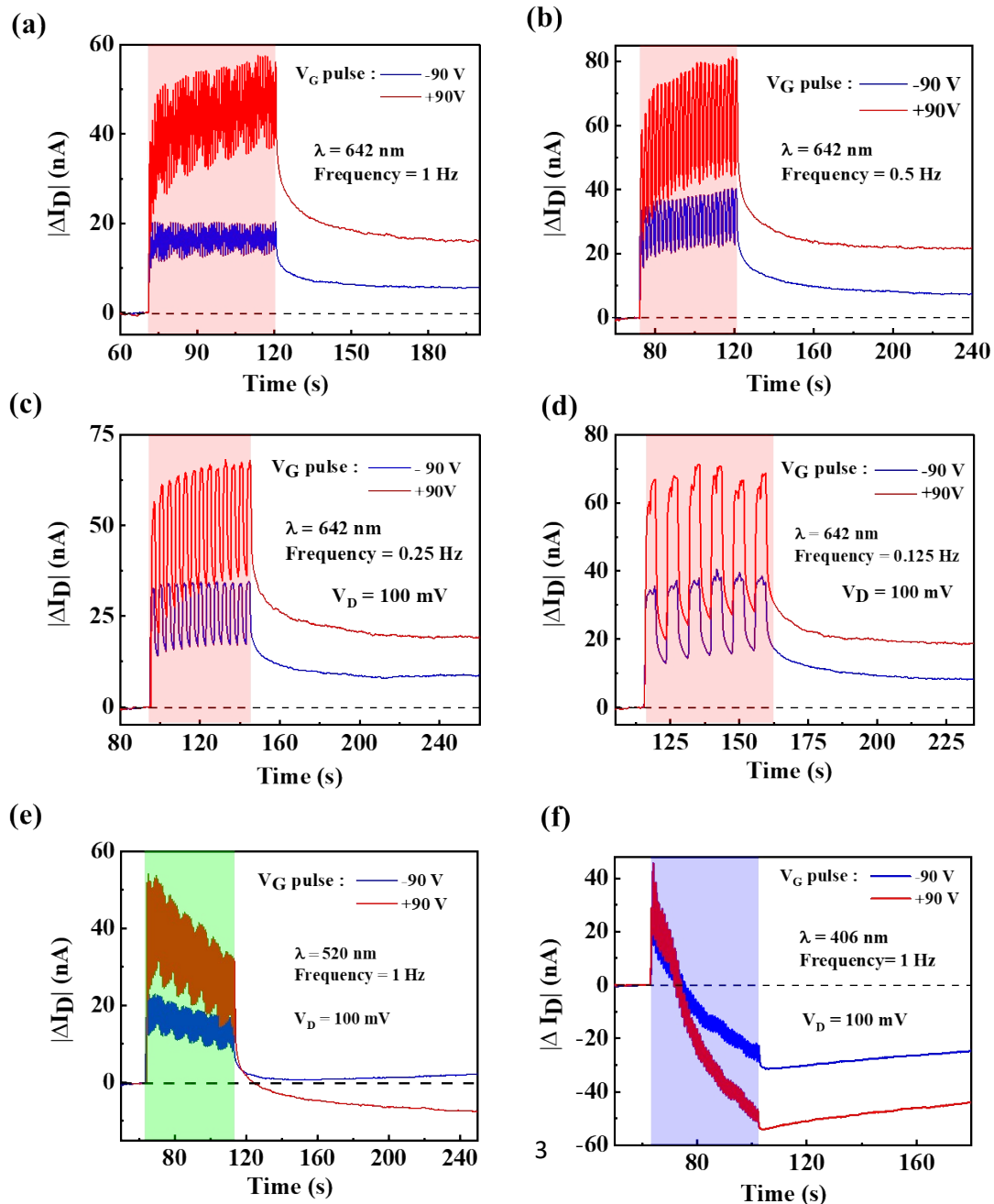


Figure S5: EPSC following two opposite gate actuations of ± 90 V triggered by 642 nm excitation of frequencies (a) 1 Hz (b) 0.5 Hz (c) 0.25 Hz, (d) 0.125 Hz. IPSC following two opposite gate actuations of ± 90 V triggered by (e) 520 nm light and (f) 406 nm light (Frequency = 1 Hz).

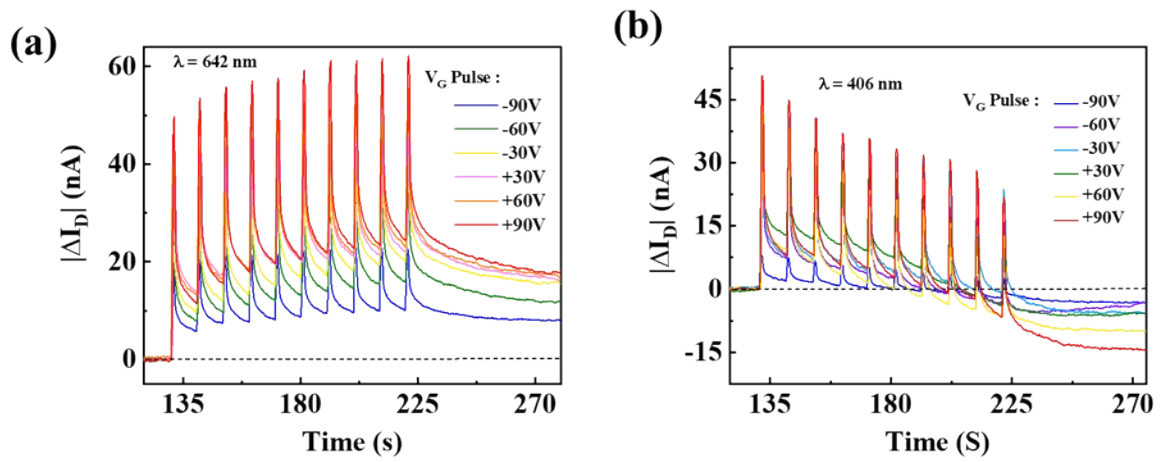


Figure S6: (a) EPSC and (b) IPSC following different gate poling conditions with uniform gate bias voltage intervals.

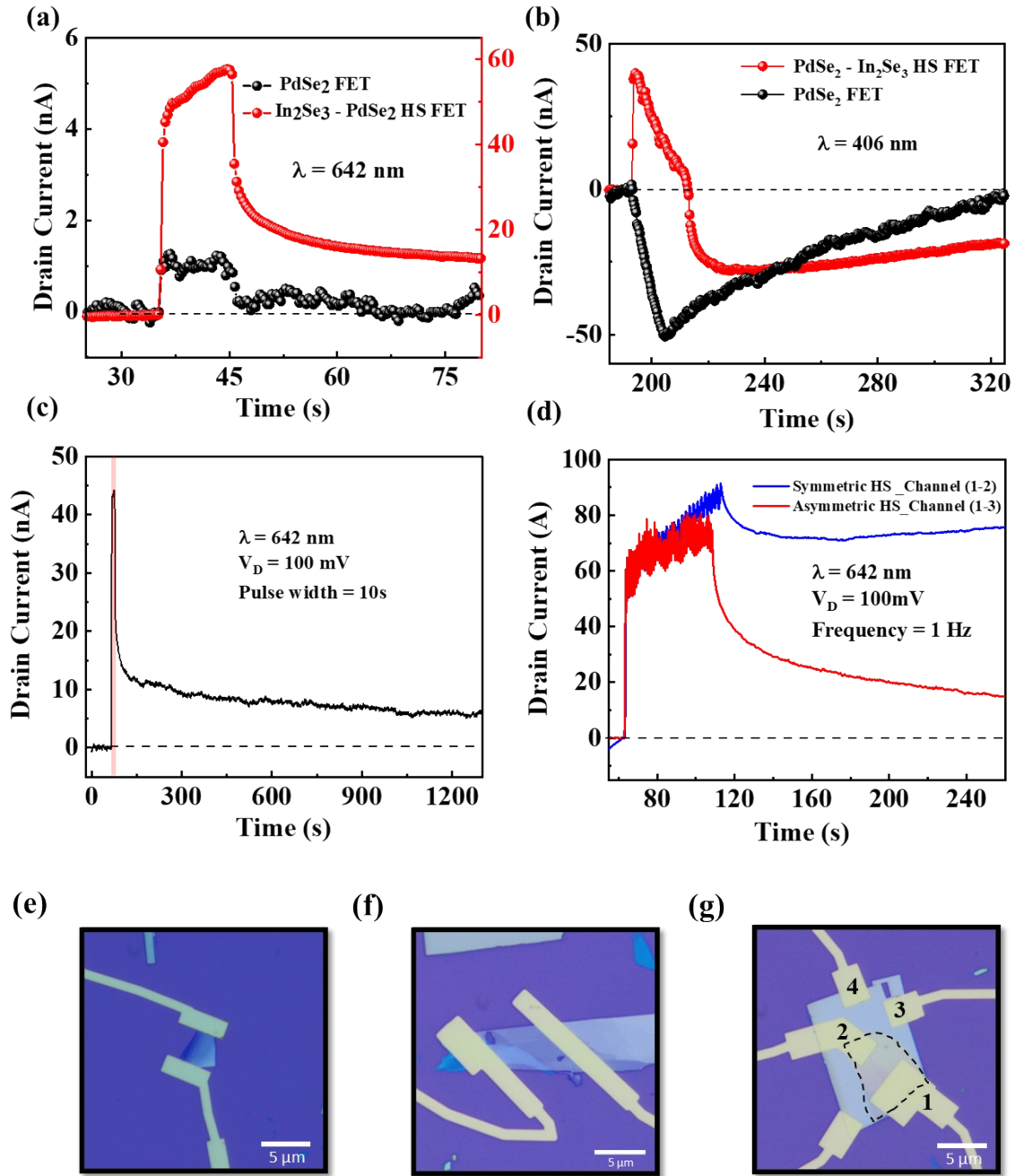


Figure S7: (a) Id-t measurement of a pristine PdSe₂ FET (black) and HS FET (red) under 10 s pulse of 642 nm light. The HS FET exhibits higher photoresponse compared to PdSe₂ FET. Moreover, after the withdrawal of light, the PSC level sustains for a longer period compared to PdSe₂ FET. (b) Id-t under 406 nm excitation of a pristine PdSe₂ FET (black) and HS FET (red) showing similar result where the PSC level sustains longer duration compared to PdSe₂ FET. (c) Retention time of the device showing stable PSC for more than 1200s after exposure to a 10 s pulse of 642 nm light. (d) Id-t measurements of asymmetric HS FET (red) and symmetric HS FET (blue) under 642 nm light at frequency of 1 Hz. It is clearly visible that after withdrawal of light, the decay time of PSC is much lower in case of symmetric HS. The drain current is also not falling rapidly after withdrawal of light compared to asymmetric HS showing very high trapping strength through OOP dipoles of In₂Se₃, as the channel (1-2) is entirely supported by ferroelectric dipoles. The difference in fall time in these two device geometry further confirms that interfacial trapping sites can be influenced by ferroelectric dipoles resulting in slower

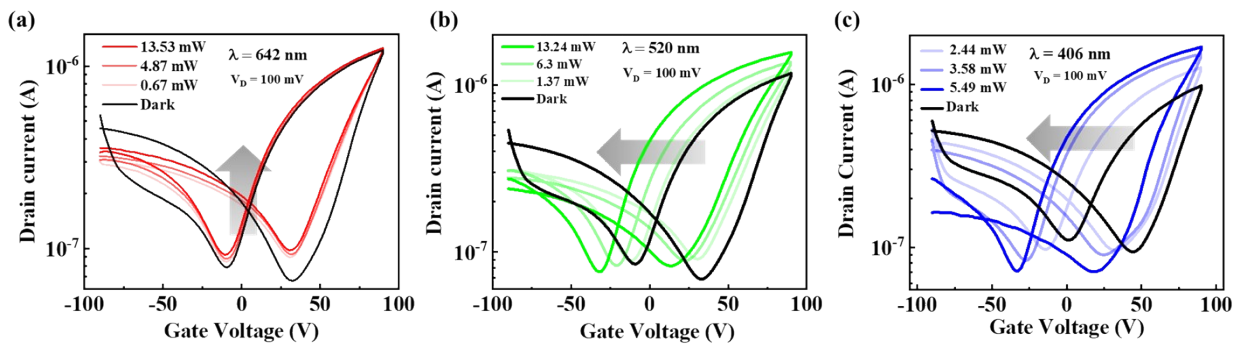
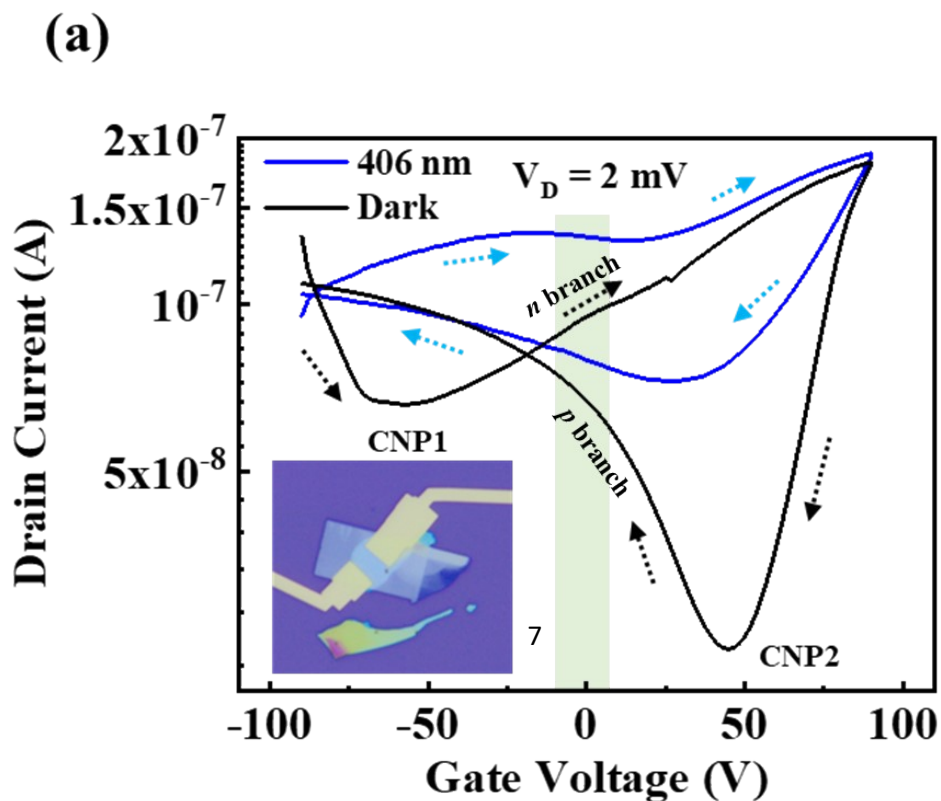


Figure S9: I_D - V_G characteristics in dark and different intensities of light illumination for (a) 642 nm, (b) 520 nm, (c) 406 nm wavelengths. As intensity of 520 nm and 406 nm increases, we see a gradual shift of I_D - V_G curve towards left side indicating more n -type doping. In case of 642 nm illumination, we see a gradual change in upward direction.



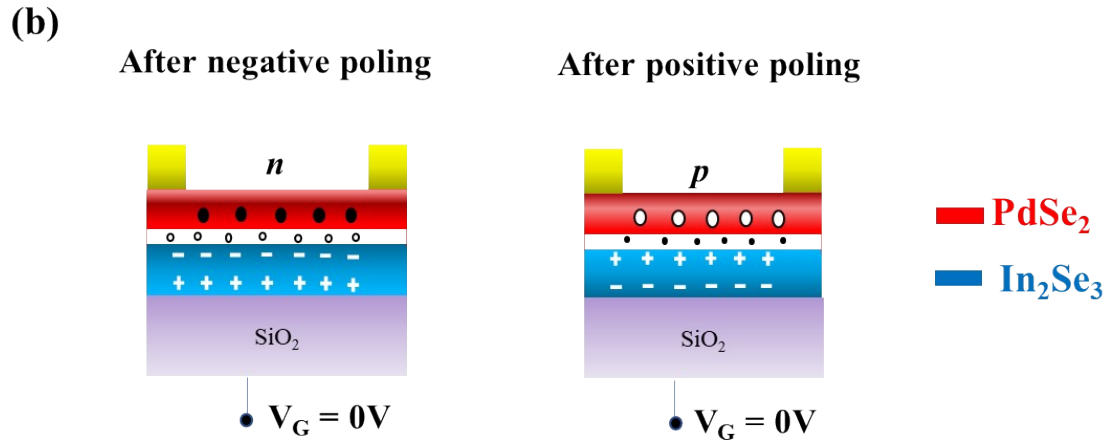


Figure S10: (a) I_D - V_G characteristics of a symmetric HS FET (inset shows the optical micrograph of the device) in dark and under 406 nm light illumination showing mild leftward shift due to dominant photogeneration from In₂Se₃. (b) Device configuration of the symmetric HS FET following two opposite poling conditions (@ $V_G=0V$).

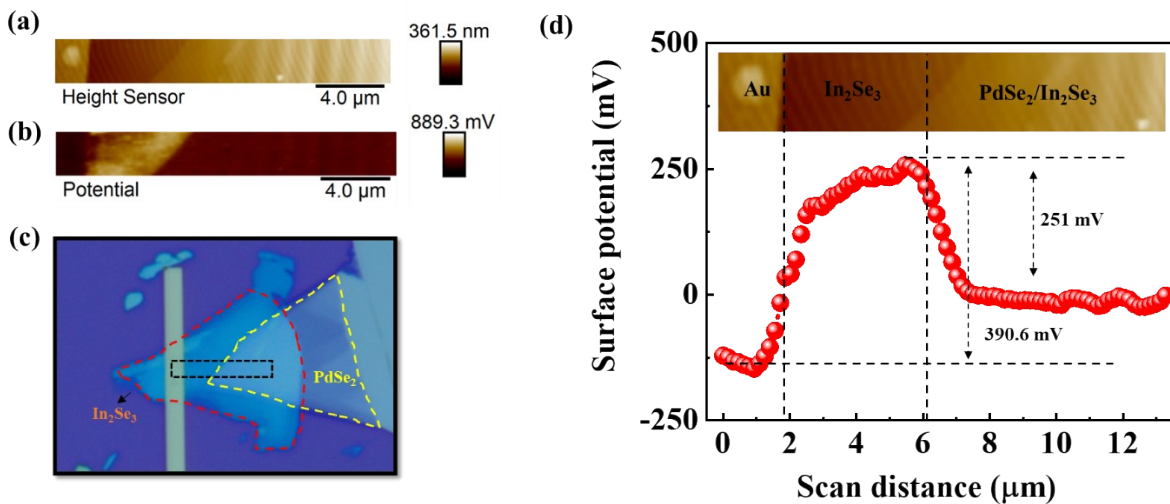
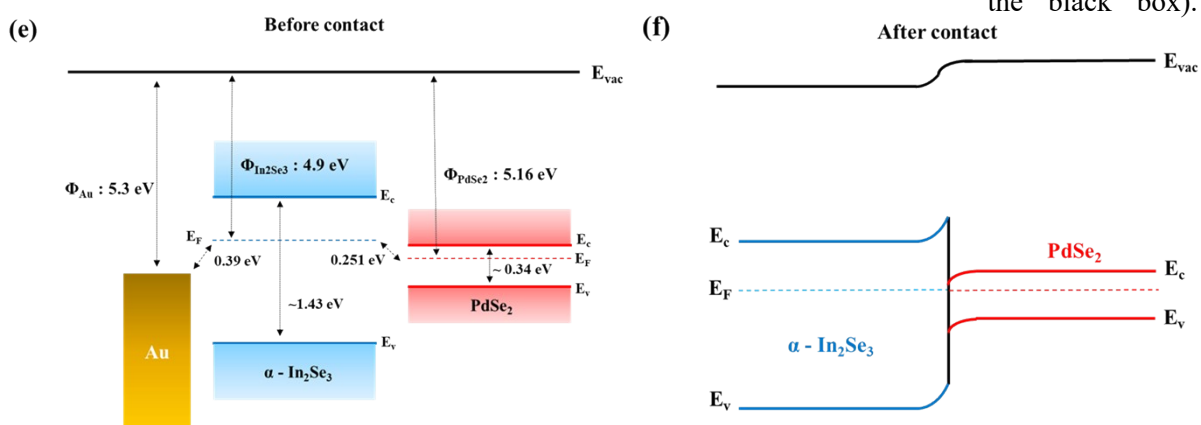


Figure S11: (a) Measured topography and (b) surface potential across the HS. (c) The corresponding optical image (the scanned area for acquiring the topographic and potential maps in a, b is marked by the black box).



(d) Surface potential profile across the Au, In₂Se₃ (non-overlapped region) and PdSe₂/In₂Se₃ (overlapped region, top surface is PdSe₂). Energy band diagram before (e) and after (f) contact in pristine state based on the KPFM measurements.

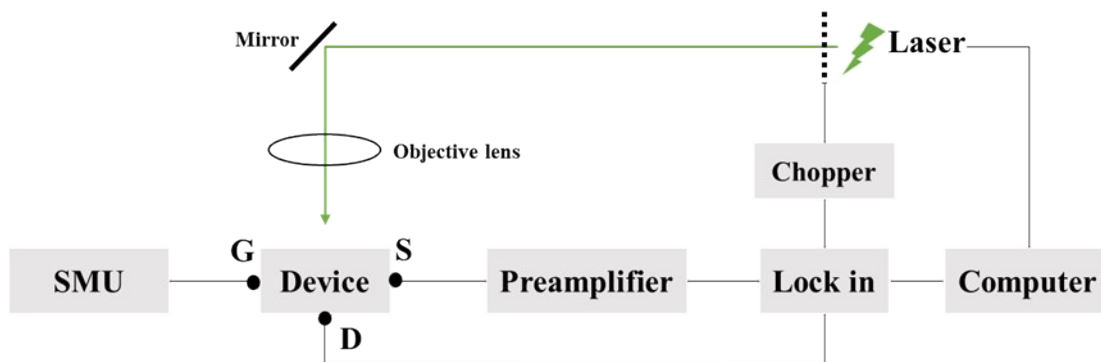


Figure S12: Scanning Photocurrent Microscopy (SPCM) measurement setup.

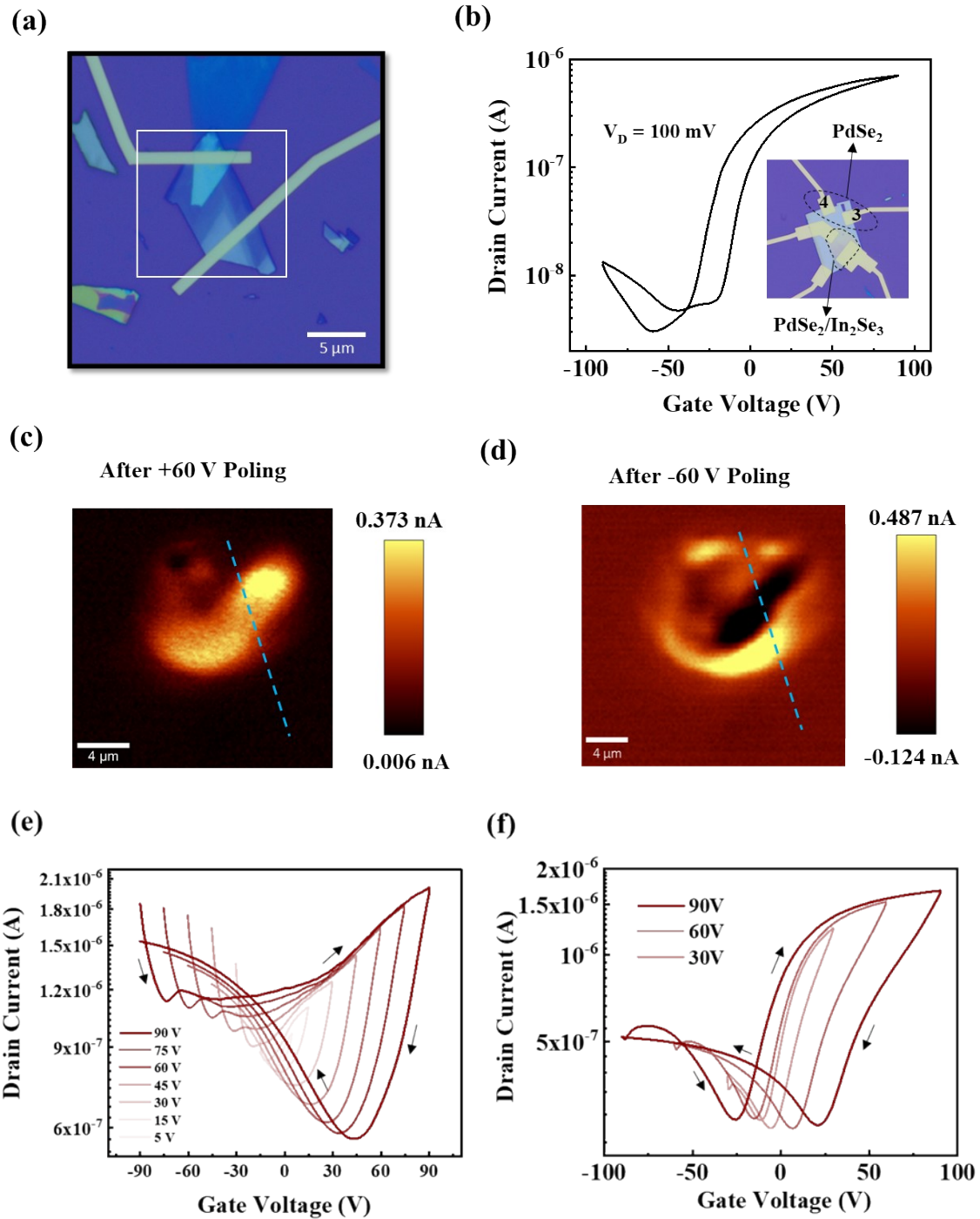


Figure S13: (a) Optical image of the device used for SPCM measurements. The white outline represents the scan area for SPCM measurements. (b) Transfer Characteristics of a pristine PdSe₂ FET on SiO₂ (channel_3-4) showing slight *n*-type behavior with negligible hysteresis.^{3,4} Inset shows the optical image of the device. Photocurrent map of the device following (c) +60 V and (d) -60 V gate poling. (e) Transfer curve of a symmetric HS FET (Optical image of the device shown in Figure S6) and (f) asymmetric HS FET for various gate sweep ranges ($V_D = 100$ mV). The hysteresis window reduces in the case of an asymmetric HS FET as the channel is partially supported by ferroelectric In₂Se₃.

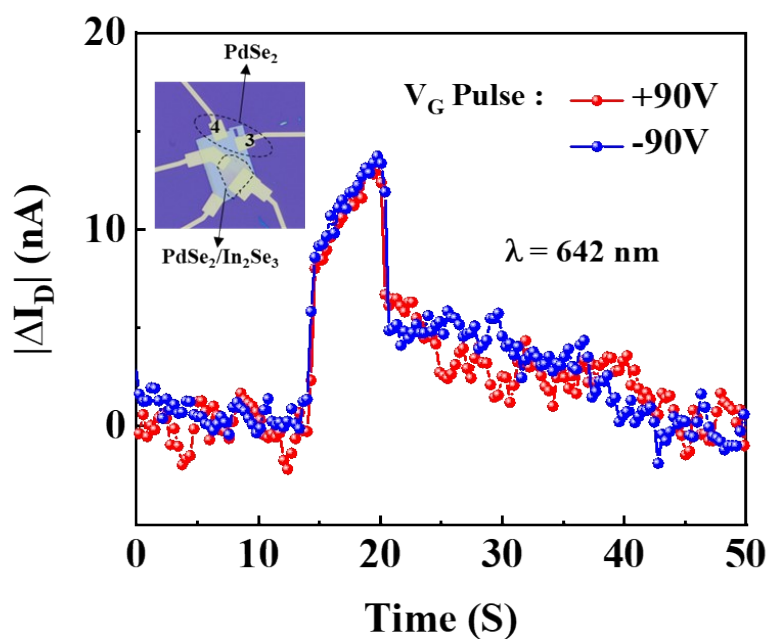


Figure S14: I_D - t ($@V_D=100$ mV) characteristics of PdSe₂ FET (channel_3-4) measured after opposite gate actuations (± 90 V) under 642 nm illumination showing no significant current variations.

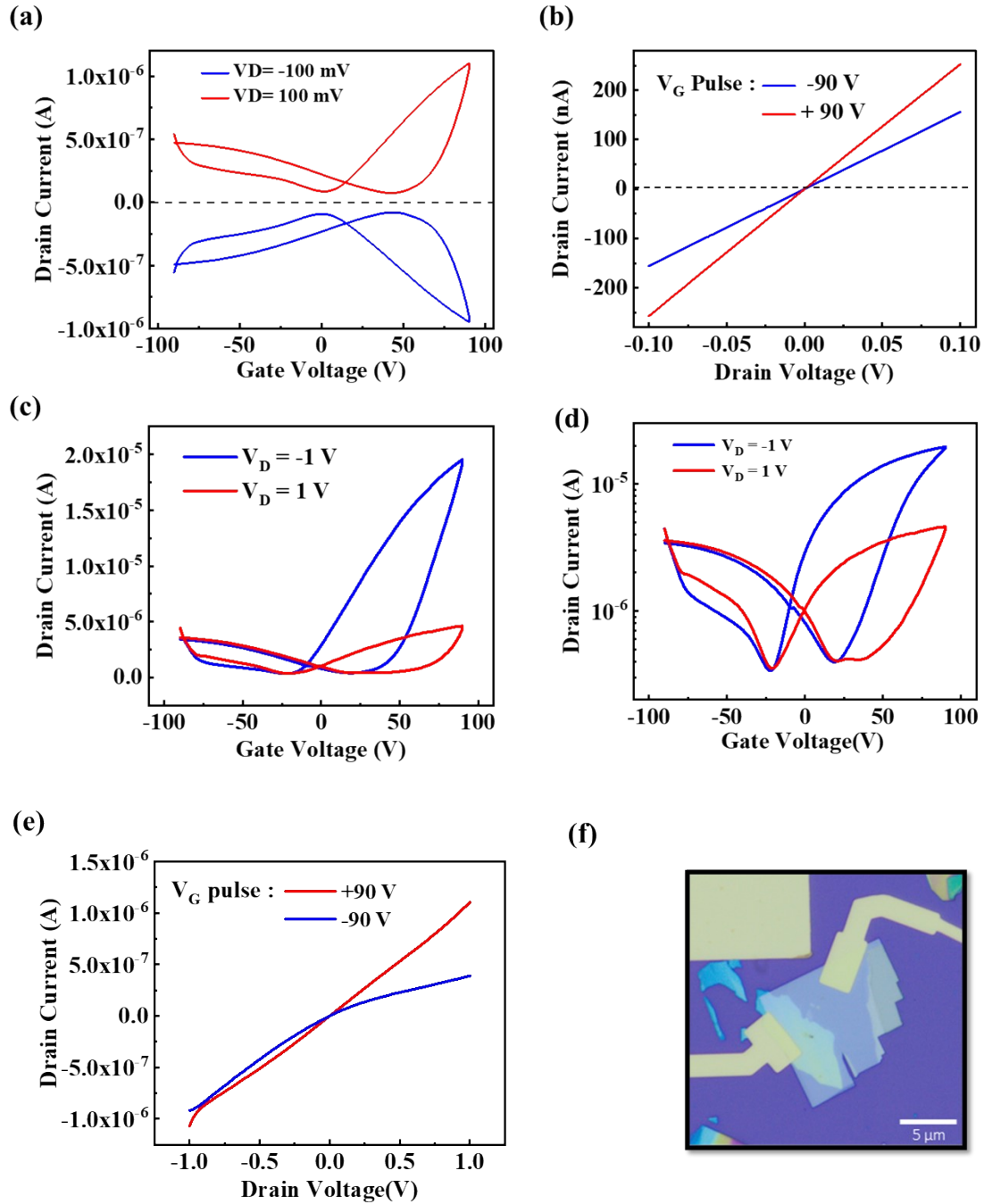


Figure S15: (a) I_D - V_G with two opposite applied drain bias voltages of ± 100 mV. (b) I_D - V_D following two opposite gate actuations of an asymmetric HS FET showing no sign for junction characteristics. I_D - V_G characteristics in linear (c) and logarithmic (d) scale at higher drain bias of ± 1 V. (e) Output characteristics of the device up to ± 1 V showing non-linear junction characteristics. (f) Optical image of the device.

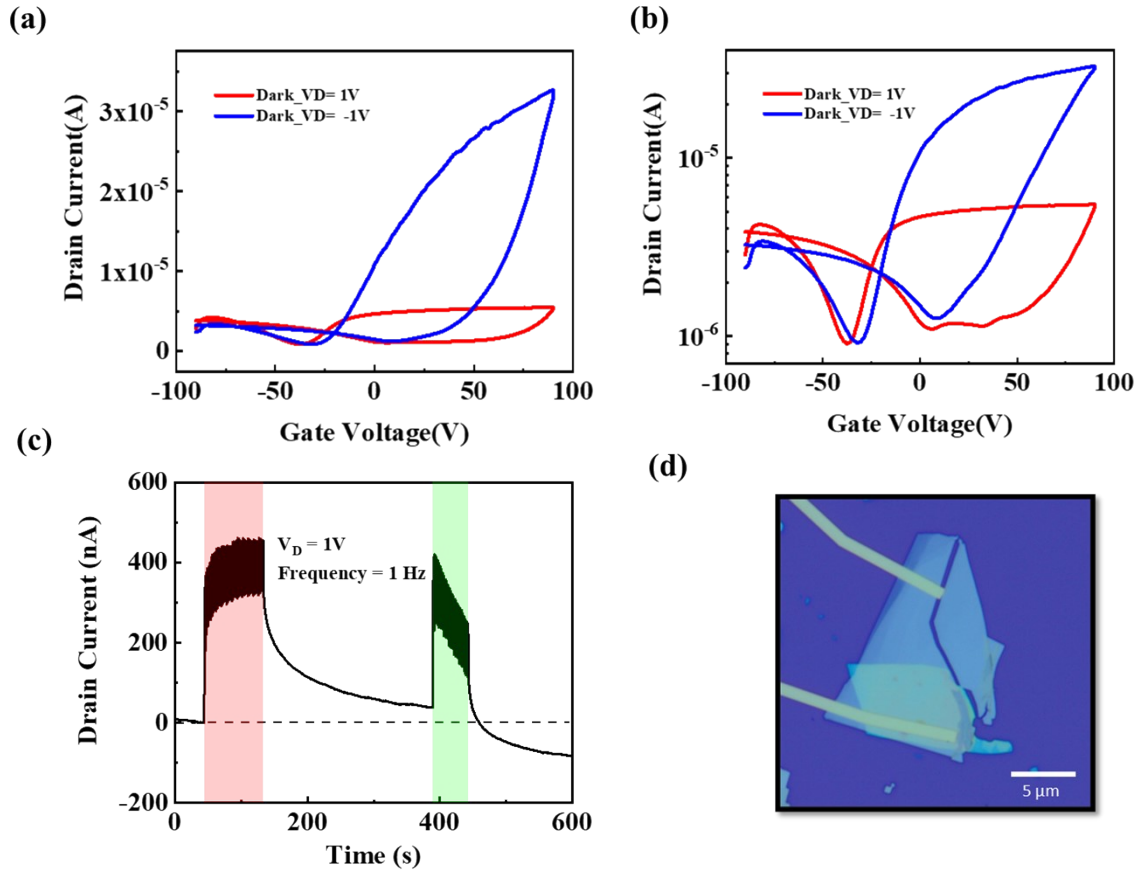


Figure S16: Reproducibility with another device showing similar transfer characteristics in linear (a) and logarithmic (b) scale; and (c) optical characteristics of bidirectional synaptic response. (d) Optical image of the corresponding device.

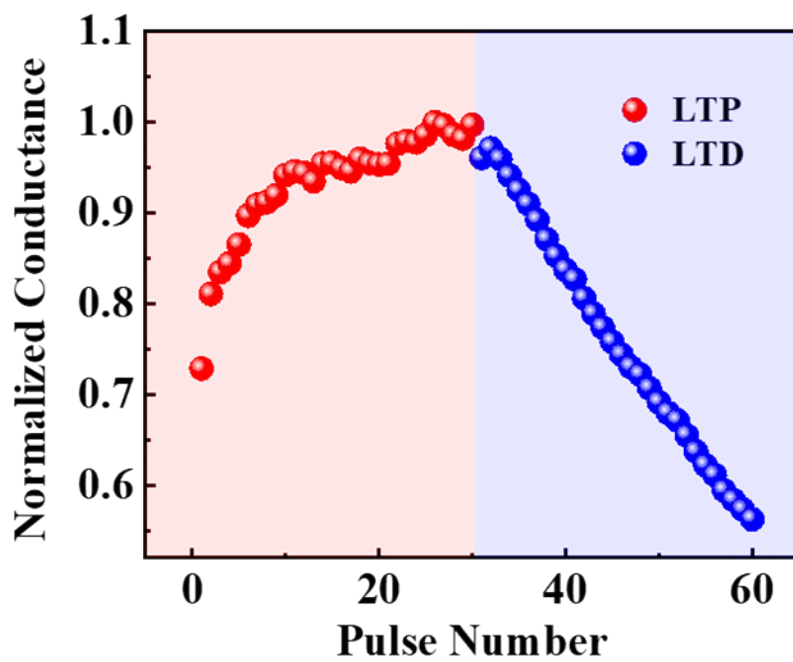


Figure S17: Normalized distinct conducting states with pulse number for LTP and LTD under illumination of 642 nm and 406 nm for 30 consecutive pulses of each wavelength.

ANN simulations

ANN was trained through two main steps: (i) computing the weight change using the backpropagation algorithm, and (ii) fine-tuning the weight by applying an optimal number of writing pulses to achieve the desired value, taking nonlinearity into account. Moreover, the synaptic weights in the artificial neural network can take both positive and negative values ($-1 \leq W_a \leq 1$), while in practical devices, the conductance (G) is inherently positive ($G_{\min} \leq G \leq G_{\max}$). Therefore, a normalization and mapping procedure was employed to correlate the experimentally obtained conductance values (Figure S13) with the simulated synaptic weights. First, the trained weights were normalized to the conductance range using:

$$W_H = \frac{W - W_{\min}}{W_{\max} - W_{\min}}$$

where W_H represents the normalized conductance weight. The corresponding quantized conductance levels were then obtained by discretizing into N distinct levels as:

$$G_{\text{mapped}} = \text{round}(W_H \times (N - 1))$$

To maintain consistency between experimental and simulated domains, the mapped conductance values were finally transformed back into normalized synaptic weights using:

$$W_A = 2 \times \frac{G - G_{\min}}{G_{\max} - G_{\min}} - 1$$

This mapping ensures a one-to-one correspondence between the physical conductance states of the device and the synaptic weights in the network, allowing a realistic hardware-compatible neuromorphic simulation.

Table S1: List of parameters required for training and testing for getting maximum accuracies. Training and Test accuracies obtained after simulation using ANN for MNIST handwritten digit recognition for different device conditions.

<i>Device Condition</i>	<i>Training Epoch</i>	<i>Test Epoch</i>	<i>Training Accuracy (%)</i>	<i>Test Accuracy (%)</i>
<i>Red (642 nm)</i>	<i>~70</i>	<i>~60</i>	<i>~99</i>	<i>~96</i>
<i>Blue (406 nm)</i>	<i>~20</i>	<i>~15</i>	<i>~99</i>	<i>~97</i>

References

1. Xia, Y. *et al.* 2D Reconfigurable Memory Device Enabled by Defect Engineering for Multifunctional Neuromorphic Computing. *Advanced Materials* **36**, 2403785 (2024).
2. Gao, J. *et al.* Multifunctional MoTe₂ Fe-FET Enabled by Ferroelectric Polarization-Assisted Charge Trapping. *Advanced Functional Materials* **32**, 2110415 (2022).
3. Mu, Y. *et al.* Homo-type α -In₂Se₃/PdSe₂ Ferroelectric van der Waals Heterojunction Photodetectors with High-performance and Broadband. *Advanced Functional Materials* **34**, 2315543 (2024).
4. Li, M. *et al.* Defect Engineering in Ambipolar Layered Materials for Mode-Regulable Nociceptor. *Advanced Functional Materials* **31**, 2007587 (2021).