Supplemental Information

Raised or Recessed? Finding the Optimal Gate Architecture for Improving the Static Performance of Graphene Transistors

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1. 3D and 2D white-light interferometry

White-light interferometry was used to observe the surface of the fabricated raised and recessed Al/hBN/graphene devices as shown in Figure S1(a) and (b), respectively. Devices with length = 10 μm and width = 20 μm, were inspected. The measured samples were coated with a thin layer of gold to provide enough contrast for the measurements. By comparison with the devices used for electrical testing purposes, the inspected device had an ungated region of ~10 μm per side to better observe the gate topology over the channel. Figure S1(a) and Figure S2(a) show that in the raised topology a step of 120-130 nm exists from the channel to the gate region. On the other hand, a much smoother transition is observed in the recessed topology where a step of only a few nanometers is observed in Figure S1(b) and Figure S2(b). These observations agree with the SEM analysis presented in the main text, Figure 4.

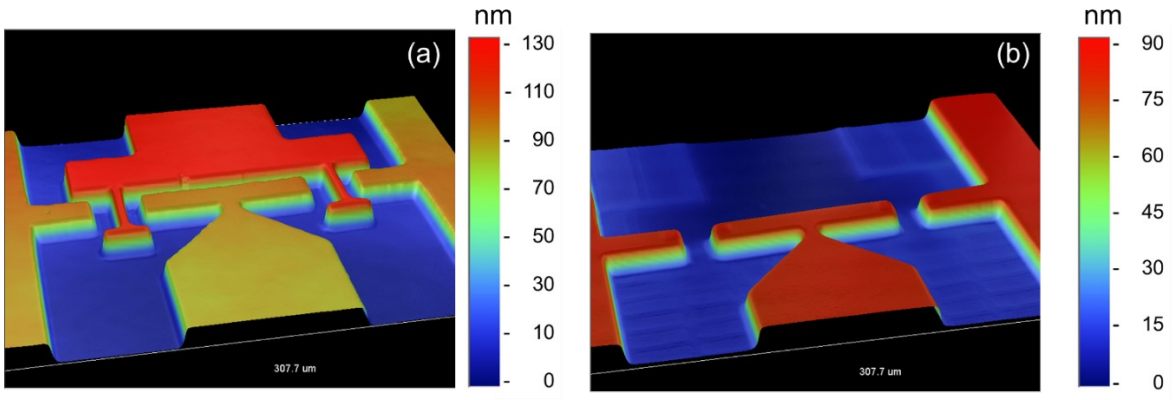

Figure S1. 3-dimensional white light interferometry scans of fabricated (a) raised and (b) recessed Al/hBN/graphene field effect transistors.

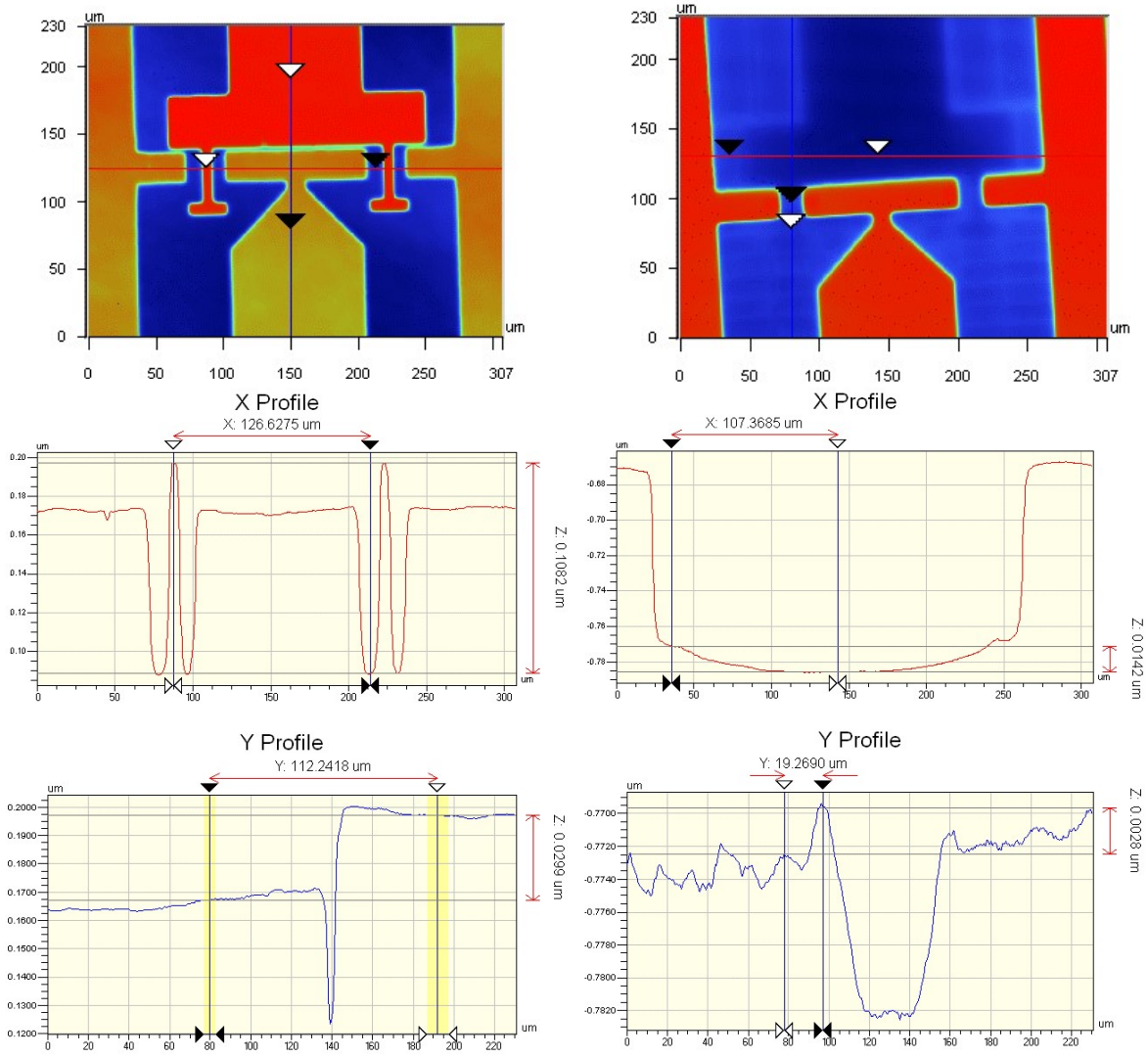

Figure S2. Surface contours plots and horizontal and vertical profiles of fabricated (a) raised and (b) recessed Al/hBN/graphene field effect transistors. The scale for the countor plots is the same as that of Figure S1.

2. ID-VG plots of all devices

The transfer curves of all 256 tested devices per group are shown in Figure S3(a) and (b) for raised and recessed architectures respectively. As seen in Figure S3(a) and (b) some devices had no current flow or no gate control and were considered as being not working devices due to missing graphene or missing continuity to the gate electrode. Figure S3(c) and (d) show the transfer curves after removing these non-working devices. Finally, in Figure S3(e) and (f), the transfer curves of devices with a maximum drain current within 5% of the maximum and minimum measured current levels have been removed to avoid non-typical devices or flyers, leaving 137 and 175 of raised and recessed architectures, respectively.

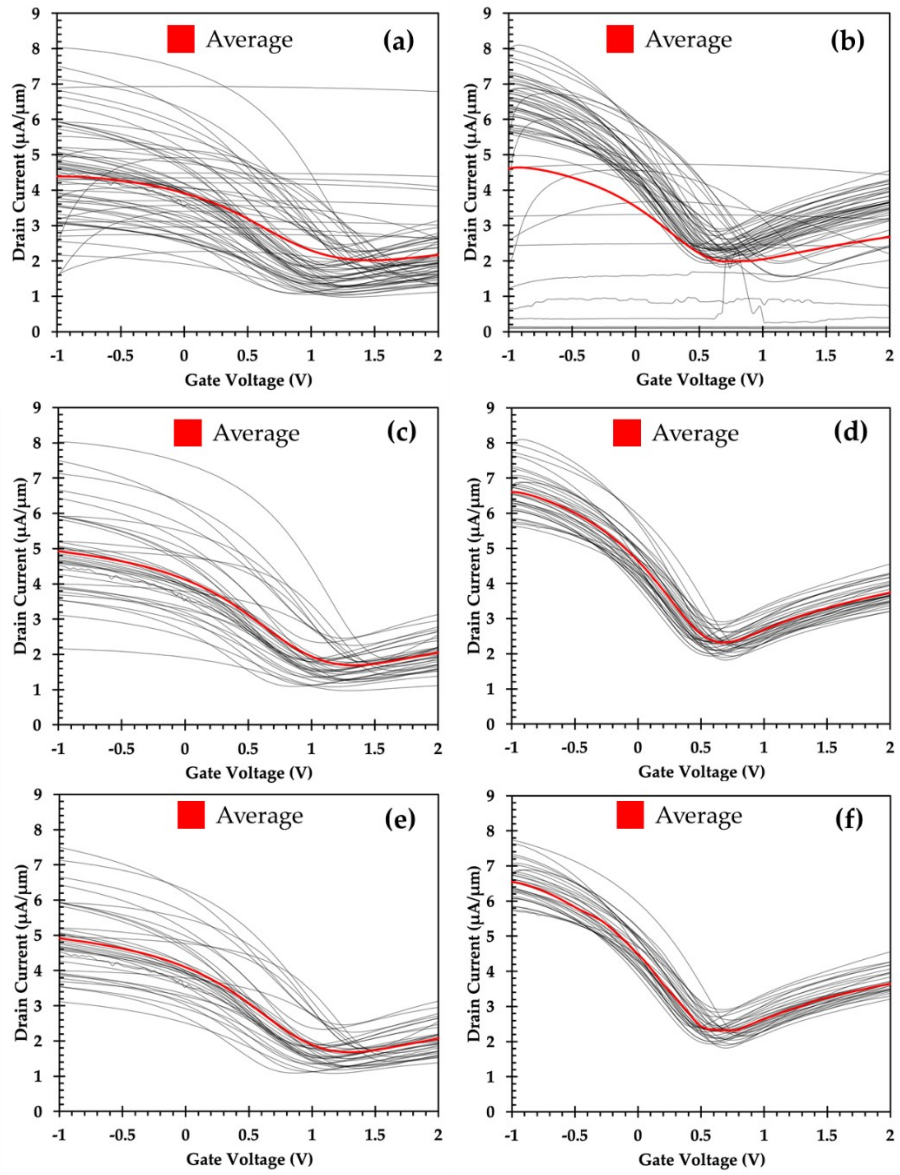

Figure S3. IDVG of tested devices for raised (a, c, e) and recessed (b, d, f) Al gate devices. (a) and (b) includes all the tested devices. (c) and (d) exclude the devices with no gate control. (e) and (f) remove devices with current values within 5% of the top and bottom performers.

3. Mobility extraction example

As described in the main text, the mobility of the holes and electrons of the individual GFETs can be extracted from the IDVG plots without the influence of R_C by extracting the β parameter and following equation S1 [1]. The parameter β is equal to $\mu_0 CoxW/L$, where μ_0 is the bias-independent low-field mobility, Cox is the oxide capacitance per unit area, and W and L are the width and length of the device. An example IDVG plot of a typical recessed GFET is shown in Figure S4(a). The parameter β can be extracted from the derived relationship of $Y^2 = \beta V_{DS} \cdot V_{GCO}^2$ where $Y = I_D/g_m^{1/2}$, and $g_m = \delta I_D/\delta V_{GS}$ as shown in Figure S4(b) [1] for holes.

$$\mu = \frac{\beta}{C_{ox}\left(\frac{W}{L}\right)} \tag{S1}$$

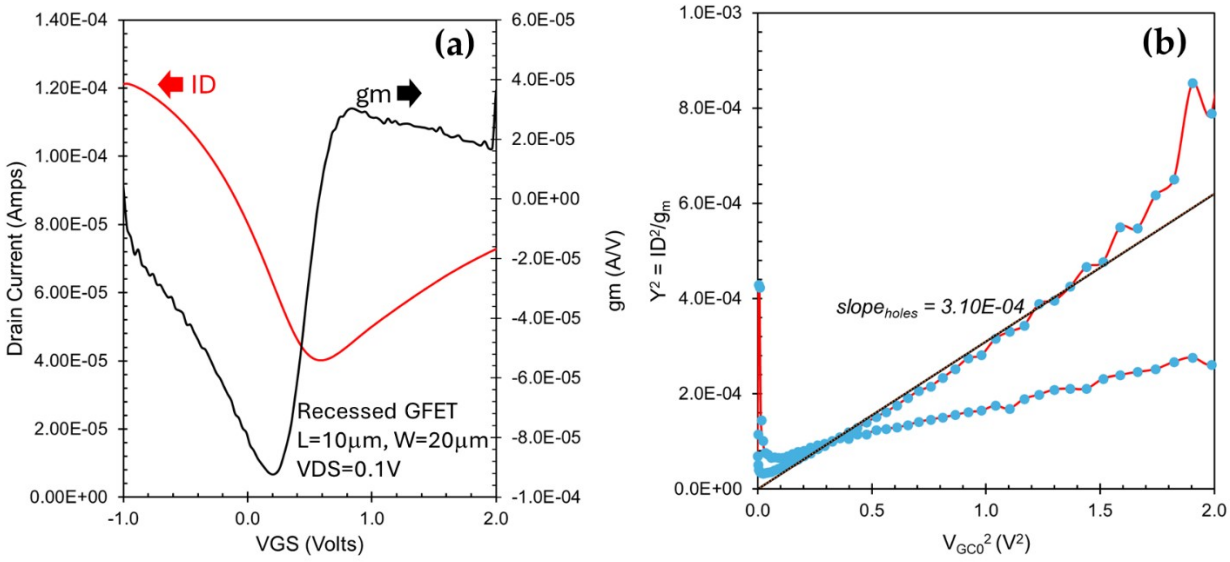

Figure S4. (a) IDVG of a typical recessed GFET with transconductance gm on the second y-axis. (b) Y^2 *vs.* V_{GC0}^2 plot, where $Y = I_D/g_m^{1/2}$, *and* $g_m = \delta I_D/\delta V_{GS}$ and $V_{GCO} = V_{GS} - V_{Dirac} - V_{DS}/2$ used to extract the slope βV_{DS} *which is used to calculate* the hole mobility without the influence of R_C [1].

From the example shown in Figure S4(b), the slope βV_{DS} is 3.10×10^{-3} A/V. Thus, the parameter $\boldsymbol{\beta}$ is 3.1×10^{-3} A/V^2 since $\boldsymbol{V_{DS}} = 0.1$ V. Measuring $Cox = 5.5\times10^{-3}$ F/m^2 on test structures as shown in the next section and considering $W/L = 2$, the mobility is calculated to be 2,820 cm^{2}V^{-1}s^{-1}.

4. CV measurements

The gate capacitance per unit area, Cox, was measured on capacitor structures formed by the channel-to-gate overlap of larger GFETs with varying widths and lengths. C-V measurements were taken with a Keithley 4200A-SCS Parameter Analyzer at 100 kHz, 30 V-rms and are shown in

Figure S5 along the capacitors size labels in terms of micrometers. The capacitance is measured while gate voltage is swept, and VD and VS are kept at 0V. These structures are larger than the GFET structures measured in the main text. The larger areas of the capacitive test structures provide consistent results as they reduce local effects that affect the capacitance of the individual devices.

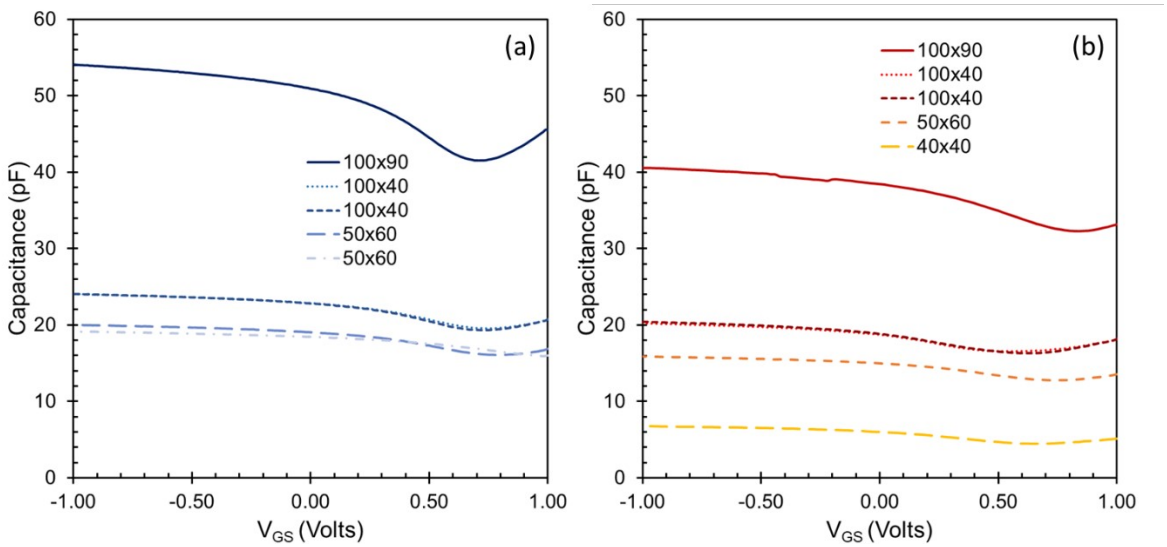

Figure S5. C-V plots of large area capacitors for (a) raised Al gate and (b) recessed Al gate structures. The listed dimensions are in units of micrometers as width × length.

The capacitance values was extracted at a hole-accumulation bias of V_{GS}=-1V for each of the tested structures and was normalized to its area for an average capacitance per unit area Cox of 5.5×10^{-3} F/m^2, as shown in Table S1 and Table S2. This average value is lower than the expected capacitance per unit area of 95.1×10^{-3} F/m^2, for a monolayer of hBN (thickness of 0.35 nm, out-of-plane relative permittivity of 3.76)[2].

Table S1. Measured capacitance of test structures fabricated with a raised aluminum gate.

Raised Al Gate					
Size (µm, L×W)	**50×60**	**50×60**	**100×40**	**100×40**	**100×90**
C (pF, V_{GS} = -1 V)	19.2	20.0	24.1	24.0	54.1
C' (F/m^2)	5.7×10^{-3}	6.0×10^{-3}	5.4×10^{-3}	5.4×10^{-3}	5.6×10^{-3}
Average (F/m^2)			5.6×10^{-3}		

Table S2. Measured capacitance of test structures fabricated with a recessed aluminum gate.

Recessed Al Gate						
Size (µm, L×W)	**50×40**	**50×40**	**50×60**	**100×40**	**100×40**	**100×90**
C (pF, V_{GS} = -1 V)	6.7	17.5	15.9	20.4	20.2	40.6
C' (F/m^2)	3.5×10^{-3}	9.0×10^{-3}	5.4×10^{-3}	5.2×10^{-3}	5.2×10^{-3}	4.6×10^{-3}
Average (F/m^2)			5.5×10^{-3}			

5. Gate Dielectric breakdown voltage measurements

In addition, as shown in Figure S6, the breakdown voltage of the dielectric is >3 V, and again higher than the expected 0.7 V associated with a monolayer of hBN with a dielectric field strength[3] of 20 MV/cm.

As seen in Figure S6, there are no significant differences in the breakdown behavior between the raised and recessed Al gate structures, although the baseline current of the recessed Al gate process seems to be slightly lower. Another observation is that there seems to be localized field breakdown as the current level increases stepwise and does not reach the tester compliance level of 100 mA. Further analysis of the test structures before and after breakdown shows that the breakdown happens as the edge of the structures where the graphene goes over the gate electrode and the electric field lines are enhanced, as shown in Figure S7(a) and the white circles in Figure S7(b). As such, the observed breakdown voltage may not correspond to the theoretical limit of the dielectric materials but provides evidence to indicate that it is unlikely that the dielectric is composed of a single monolayer of hBN.

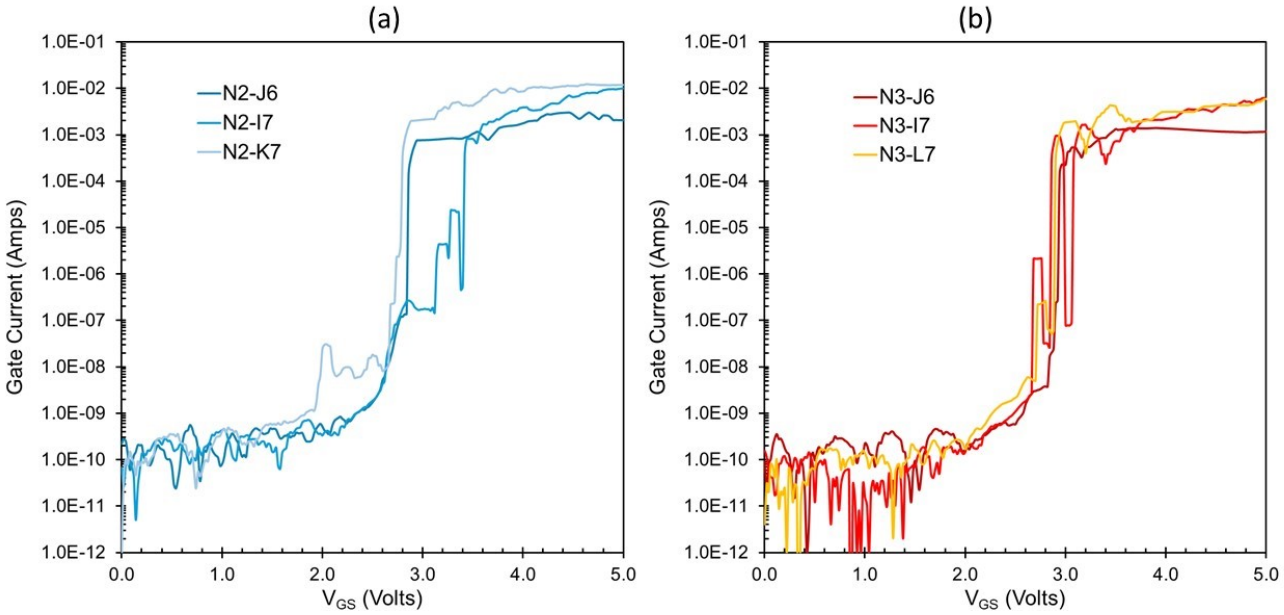

Figure S6. Breakdown voltage plots of (a) raised Al gate and (b) recessed Al gate capacitors.

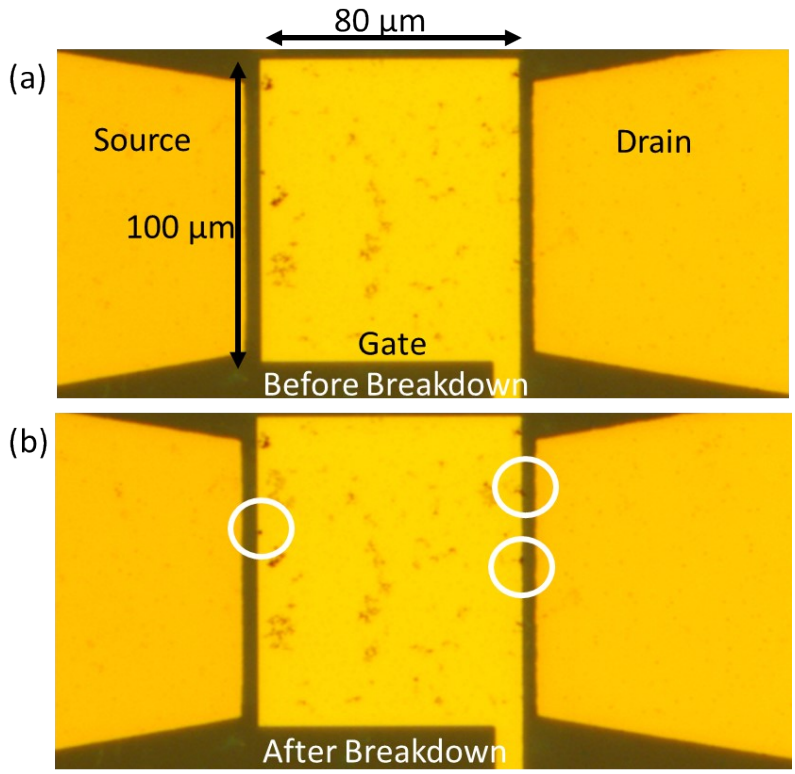

Figure S7. Microscope pictures of a 100×80 µm capacitor (a) before and (b) after breakdown. White circles in (b) indicate suspected dielectric breakdown locations at the edge of the raised Al gate electrode.

6. Cox discussion

It has been shown that a native aluminum oxide readily forms on aluminum surfaces depending on the environment conditions[4]. The thickness of this native aluminum oxide (AlOx) could vary from 1 to 10 nm[5,6]. As such, using a series capacitance approximation as shown in Figure S8, the thickness of the AlOx with a dielectric constant of 8, can be estimated to be 12 nm if the hBN film is still considered to be a monolayer.

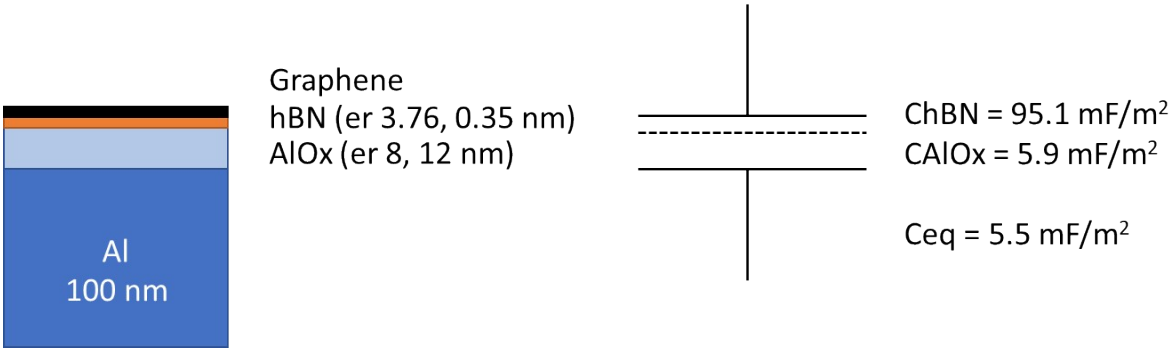

Figure S8. Illustration of the gate capacitive structure with the addition of an AlOx layer as well as estimates of the capacitance per unit area of a dielectric composed of two films with their corresponding thickness and relative dielectrics.

7. Hysteresis pulse test description and measurements

Hysteresis measurements with non-pulsed and pulsed (based 0 V) are shown in Figure S9 where dotted black line forming a stair-cased voltage sweep and red solid lines demonstrates a pulse sweep. The step time (t_{step}) for non-pulsed measurement is 200 ms for each datapoint and the pulse width time (t_{pw}) for the pulsed (base = 0 V) measurement is 500 µs for each datapoint collected. The purpose of the pulsed testing is to reduce the impact of traps, while under the assumption where the time constant associated with trap charging is greater than the pulse width[7].

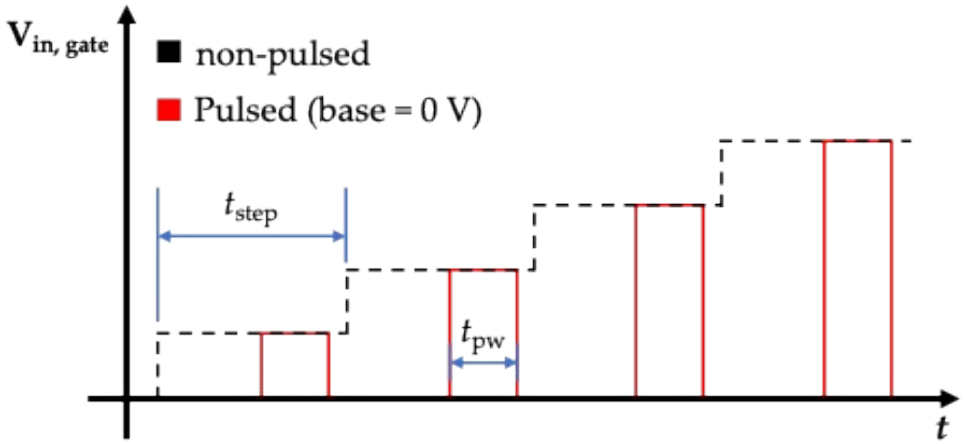

Figure S9. Gate voltage bias over time for (dotted black) non-pulsed and (solid red) pulsed measurements.

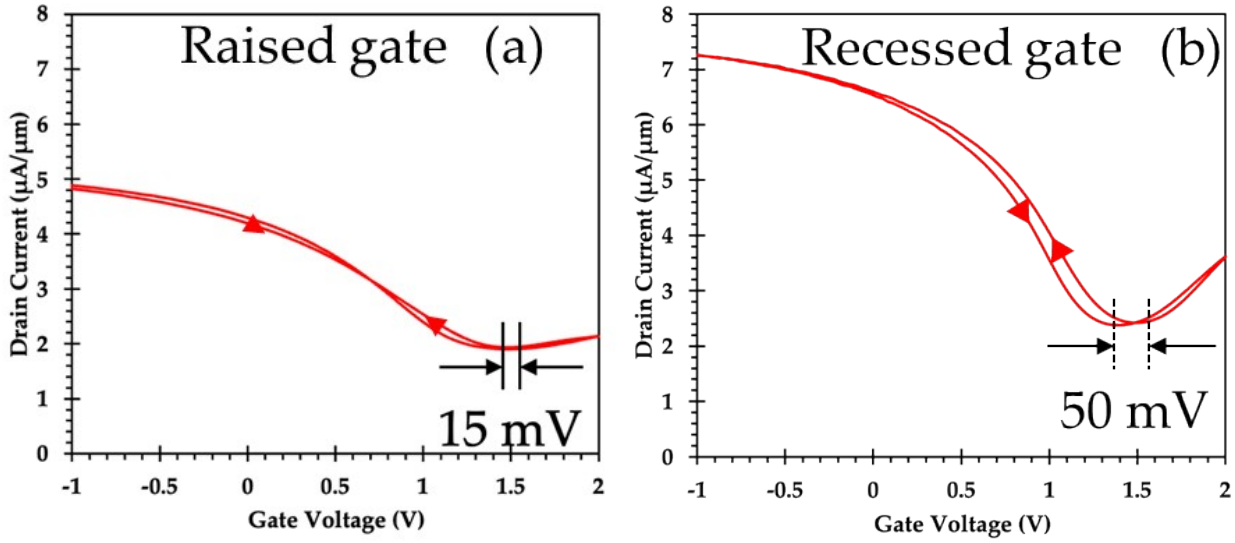

Figure S10. Hysteresis curves for raised (a) and recessed (b) Al gate GFETs obtained using a 1V-pulse method. Figure 9 in the main text presents hysteresis results with no pulse and with 0V-pulse.

8. Heatmaps of key performance parameters and yield

Within each device structure, a total of 512 devices were tested for statistical analysis and heatmap distribution shown in . Device yield and KPM variation heatmaps were created for all 256 devices tested for each structure in study. Figure S11(a) shows the yield of each device structure, with 54.4%, and 65.1%, respectively for hBN on raised Al gate, and hBN on recessed Al gate. The increased yield observed as the planarization of the gate structure through a chemical mechanical planarization process. Several factors contribute to the observed improvement in yield when compared to our prior work with a yield of 14% on Al_2O_3/raised Al gate structure [8]. First, the adoption of hBN as a wet-transferred dielectric reduces the number of fabrication processes, minimizing risk of tearing, wrinkling or doping from surface residues. Second, the CMP-recessed gate reduces surface topography variation, leading to a more uniform hBN coverage and better graphene/dielectric interface quality. As a result, a simplified process with less fabrication-induced defects and planarized surface with less topography variation leads to a higher yield, improved electrostatic control, and greater reproducibility. Additionally, a significantly reduced device-to-device variation was observed, in specifically mobility and Dirac voltage, indicating an improved process control and a better material interface. While average contact resistance improved significantly, its variation (standard deviation) remained relatively unchanged across device structures, suggesting that local variations at metal-graphene interface is minimal and may be attributed to the quality of the material interfaces. Spatial heatmaps of yield and KPM for Figure S11(a) graphene on hBN on raised Al gate, and Figure S11(b) graphene on hBN on recessed Al gate reveal that variability is not confined to a isolated region, with no clear indication of a regular distribution pattern.

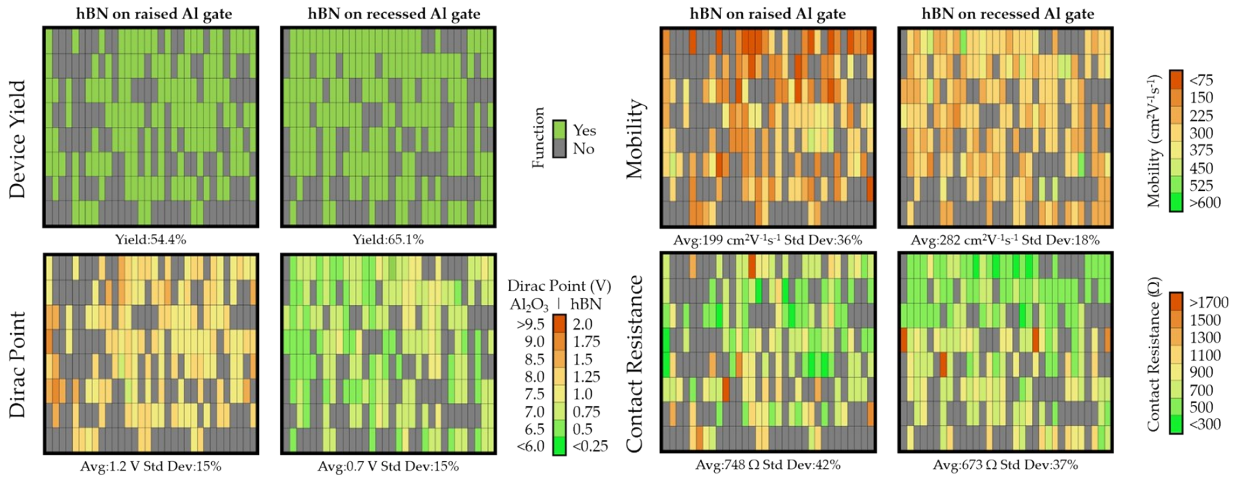

Figure S11. Device variation heatmap of device yield, mobility, contact resistance and Dirac point for a total of 512 fabricated devices **(a)** raised Al gate with hBN gate dielectric and **(b)** recessed Al gate with hBN gate dielectric, respectively.

Although an overall improvement can be observed comparing between structure to structure, a distribution trend within a structure (i.e. gate length variation from 2 µm to 12 µm from first to last row of the heatmap) seemed to be at random distribution. A clear reduction of V_{Dirac} between hBN/raised Al gate structure and hBN/recessed Al gate structures was observed. Contact resistance is also improved (lowered) when changing from a raised to a recessed gate topography. Furthermore, overall device variability is significantly reduced through the use of hBN as a dielectric and recessed gate architecture. In contrast, devices incorporating hBN dielectrics, in particular hBN/recessed Al gate structural devices, exhibit much tighter performance distributions across all key parameters along with achieving a higher yield when comparing to prior work [8]. The result suggests that while peak performance may not dramatically improve, the overall variable and reproducibility of device performance are improved.

9. Contact resistance comparison between hBN and Al_2O_3 as underlaying films

As shown in Figure S11, the contact resistance improves significantly when moving from Al_2O_3 to hBN as the contact underlayer material. The data shown for the Raised Al_2O_3 comes from extracting the contact resistance of 37 individual devices presented by our group in a 2023 report[8] . The contact resistance improves from an average of 2.59 kΩ for the devices with an Al_2O_3 underlayer to 0.75 kΩ and 0.67 kΩ for devices with hBN as the underlayer. In addition, the standard deviation of the Al_2O_3/raised gate was 78%, which is much larger than 42% and 37% for the other groups, likely due to poor interfacial quality, and increased roughness.

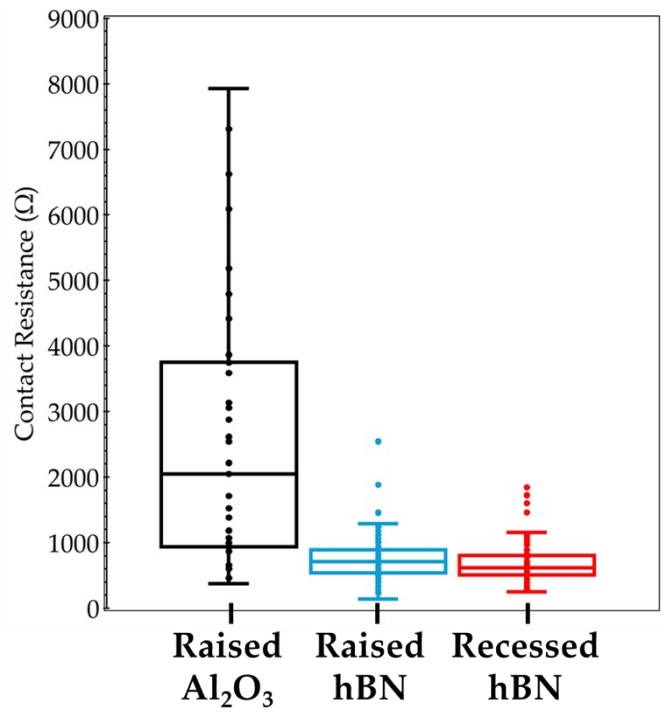

Figure S12. Box plot distributions of contact resistance values of GFETs with Al_2O_3 or hBN as the underlying film below the graphene and Ti/Au metal contacts. The groups also indicate whether a raised or recessed architecture was used.

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