## **Supplementary Information**

## Multifunctional CMOS-Integrable and Reconfigurable 2D Ambipolar Tellurene Transistors for Neuromorphic and In-Memory Computing

Bolim You<sup>ab⊥</sup>, Jihoon Huh<sup>ab⊥</sup>, Yuna Kim<sup>a</sup>, Mino Yang<sup>c</sup>, Unjeong Kim<sup>\*d</sup>, Min-Kyu Joo<sup>\*efg</sup>, Myung Gwan Hahm<sup>\*ah</sup>, Moonsang Lee<sup>\*ab</sup>

<sup>a</sup> Department of Materials Science and Engineering, Inha University, 100 Inha-ro, Michuhol-gu, Incheon 22212, Republic of Korea

<sup>b</sup> Program in Semiconductor Convergence, Inha University, 100 Inha-ro, Michuhol-gu, Incheon 22212, Republic of Korea

°Korea Basic Science Institute Seoul, 6-7, Goryeodae-ro 22-gil, Seongbuk-gu, Seoul 02841, Republic of Korea

<sup>d</sup> Department of physics, Dongguk university, Seoul 04620, Republic of Korea

<sup>e</sup> Department of Applied Physics, Sookmyung Women's University, Seoul 04310, Republic of Korea

<sup>f</sup> Institute of Advanced Materials and Systems, Sookmyung Women's University, Seoul 04310, Republic of Korea

<sup>g</sup> Electrical Engineering Division, Engineering Department, University of Cambridge, Cambridge CB3 0FA, UK

<sup>h</sup> Institute for Bio-Medical and Translational Health Care, Inha University Hospital, 27 Inhang-ro, Jung-gu, Incheon 22332, Republic of Korea

\* Corresponding authors.

E-mail addresses: ujjane.kim@dongguk.edu (U. Kim), mkjoo@sookmyung.ac.kr (M.-K. Joo),

mghahm@inha.ac.kr (M.G. Hahm), mslee@inha.ac.kr (M. Lee)

 $^{\bot}\textsc{Bolim}$  You and Jihoon Huh contributed equally to this paper.



**Figure S1.** (a) Schematic of the hydrothermal process for synthesizing atomic-layered tellurene(Te) using solvent-assisted thinning.



Figure S2. (a) Atomic force microscopy (AFM) image of a 2D Te nanoflake. The measured surface roughness values within the selected region are  $R_a = 1.72$  nm and  $R_q = 2.52$  nm. (b) Corresponding height profile taken along the white dashed line, showing a thickness of approximately 13 nm for the 2D Te flake.



**Figure S3.** (a) High-angle annular dark-field scanning transmission electron microscopy (HAADF–STEM) image of Te on a Si/SiO<sub>2</sub> substrate with a 20 nm  $Al_2O_3$  layer. (b) EDS mapping images of Al, Te, Si, O, and C.



**Figure S4.** Optical and Raman mapping images of (a) bare 2D Te and (b) 2D Te with 20 nm  $Al_2O_3$  on Si/SiO<sub>2</sub> (100 nm).



Figure S5. XPS core level spectra of (a)  $Al_{2p}$ , (b)  $O_{1s}$ , and (c)  $C_{1s}$  for  $Al_2O_3$  on 2D Te flake.

	Peak Binding energy (eV)	Height CPS	FWHM (eV)	Area under curve	Atomic %
Al <sub>2p</sub>	74.39	5546.3	1.67	10299.57	40.57
O <sub>1s</sub>	531.07	24581.16	2.07	57163.2	59.07
Te <sub>3d</sub>	576.6	300.33	3.75	4859.96	0.35

**Table S1.** Atomic percentage calculation for Al, O, and Te in Al<sub>2</sub>O<sub>3</sub>/Te. The obtained O/Al ratio of 1:1.45 indicates oxygen deficiency.



Figure S6. (a) Schematic and OM images of ambipolar 2D Te transistor fabrication method.

The source and drain electrodes with a channel length and width of 12 and 4.5  $\mu$ m, respectively, were fabricated along the [0001] direction to consider the crystal anisotropy of the Te flake. All the electrodes, including the gate electrode, were fabricated employing conventional photolithography and e-beam evaporation. The electrodes were deposited at an evaporator chamber pressure of ~10<sup>-5</sup> Torr or lower, with a deposition rate of 1 Å/s, using Ti/Au (30 nm/70 nm). The Al<sub>2</sub>O<sub>3</sub> thin film was deposited *via* thermal ALD following the fabrication of the source/drain electrodes to modulate the 2D Te from p-type to ambipolar while utilizing it as a gate dielectric layer.



**Figure S7.** Electrical characteristics of an ambipolar Te top-gate transistor. (a) Schematic of the ambipolar Te synaptic device. (b) Schematic band diagram of 2D Te/Al<sub>2</sub>O<sub>3</sub> at different gate biases. (c) Transfer curves and (d) output curves of ambipolar Te/Al<sub>2</sub>O<sub>3</sub> FET.

To verify the feasibility of the ambipolar 2D Te transistor as an artificial synaptic device, its electrical characteristics were investigated, as shown in **Figure S7**. **Figure S7a** shows the schematic of an ambipolar 2D Te FET functioning as the ambipolar modulation layer in a topgate structure. By depositing a 20 nm Al<sub>2</sub>O<sub>3</sub> thin film *via* ALD, an n-doping effect was induced in the Te channel through oxygen vacancies at the Te/Al<sub>2</sub>O<sub>3</sub> interface. Further, the dissociated methyl groups from the trimethylaluminum precursor during ALD can transfer electrons, increasing the electron concentration in Te.<sup>1, 2</sup> The change in the electron concentration in Te owing to the Al<sub>2</sub>O<sub>3</sub> passivation layer can alter the energy position of the Fermi level, resulting in a band alignment different from that of bare 2D Te (**Figure S7b**). Following Al<sub>2</sub>O<sub>3</sub> passivation, the Fermi level shifted towards the conduction band owing to the n-doping effect, causing electrons to accumulate in the 2D Te when a positive  $V_{GS}$  is applied, rendering the n-doped Fermi level closer to the conduction band.<sup>3</sup> As a result, the energy band shifted downward, which allowed electron accumulation and reduced the Schottky barrier height (SBH), thereby facilitating electron carrier movement. In this case, the device operated as an n-type FET. Similarly, when a negative  $V_{GS}$  was applied, the Fermi level became p-doped closer to the valence band, causing downward band bending and reducing the SBH, thus facilitating hole carrier movement. In this case, the device operated as a p-type FET. Consequently, 2D Te/Al<sub>2</sub>O<sub>3</sub> can operate as an ambipolar transistor under various  $V_{GS}$  values depending on band bending.

**Figure S7c** shows the ambipolar transfer characteristics of the 2D Te FET following  $Al_2O_3$  deposition at various drain voltages. At  $V_{DS}$  of 1 V, the region between the 0–5 V gate voltage was observed as the charge neutral point (CNP), with threshold voltages ( $V_{TH}$ ) of 4.65 and -2.3 V in n- and p-type, respectively. This indicated the successful modification into ambipolar characteristics *via* a thermal ALD process. The symmetrical linear operation of the output curves, as shown in **Figure S7d**, indicated that ohmic contacts were well formed at both polarities. These results confirm the successful modulation of ambipolar behavior in the 2D Te transistor after  $Al_2O_3$  deposition.



**Figure S8.** Gate terminal was modified to show short-term synaptic plasticity (STP) characteristics. N-type STP characteristics of (a) EPSC and (b) IPSC under different time durations of 10, 50, and 100 ms (read voltage: 0.1 V, amplitude: 3 V); inset: EPSC and IPSC change curves under different pulses. (c) EPSC curve under different read voltages of 1, 10, and 100 mV (amplitude: 3 V, time duration: 100 ms); inset: enlarged EPSC curve with a read voltage of 1 mV. P-type STP characteristics of (d) EPSC and (e) IPSC under different time durations of 10, 50, and 100 ms (read voltage: 0.1 V, amplitude: 3 V); inset: EPSC and IPSC change curves under different pulses. (f) EPSC curve under different read voltages of 1, 10, and 100 mV (amplitude: 3 V, time duration: 100 ms); inset: enlarged EPSC curve with a read voltage curves under different pulses. (f) EPSC curve under different read voltages of 1, 10, and 100 mV (amplitude: 3 V, time duration: 100 ms); inset: enlarged EPSC curve with a read voltage of 1 mV.

	Potentiation nonlinearity	Depression nonlinearity	Dynamic ranges $(G_{max}/G_{min})$	Asymmetry ratio	Effective conductance states
Figure 3b	1.17	1.66	4.49	0.28	100
Figure 3e	2.00	0.57	1.77	0.26	83

**Table S2.** Gate tunability performance summary of an ambipolar 2D Te synaptic transistor in terms of linearity, dynamic ranges, asymmetry ratio, and effective states.

Active materials	Structure	Polarity	Oxide	Oxide Thickness	Power	Nonlinearity	Recognition accuracy	Ref
Те	Top-gate FET	Ambipolar (N-type)	Al <sub>2</sub> O <sub>3</sub>	20 nm	3.5 fJ	1.17/1.66	94.2%	This work
Те	Top-gate FET	Ambipolar (P-type)	Al <sub>2</sub> O <sub>3</sub>	20 nm	19 fJ	2.00/0.57	94.7%	This work
$MoS_2$	Back-gate FET	Unipolar (N-type)	SiO <sub>2</sub>	90 nm	450 pJ	-1.3/-5.2	91.1%	4
$MoS_2$	Back-gate FET	Unipolar (N-type)	Al <sub>2</sub> O <sub>3</sub>	35 nm	~6 pJ	1.84/0.86	~94.2%	5
$\alpha$ -In <sub>2</sub> Se <sub>3</sub>	Back-Gate FET	Unipolar (N-type)	Ta <sub>2</sub> O <sub>3</sub>	40 nm	10 pJ	0.81/2.1	93%	6
WSe <sub>2</sub>	Back-gate FET	Unipolar (P-type)	h-BN	37.5 nm	~532 fJ	1.4/1.4	~90%	7
Nb-doped WSe <sub>2</sub>	Back-gate FET	Unipolar (P-type)	SiO <sub>2</sub>	100 nm	12.27 pJ	0.01/5.88	91.3%	8
WSe <sub>2</sub>	Bottom gate FET	Ambipolar (hybrid)	Al <sub>2</sub> O <sub>3</sub>	15 nm	-	2.2/2.1	~90%	9
MoTe <sub>2</sub>	Top-gate FET	Ambipolar	P(VDF- TrFE)	~150 nm	-	4.88/5.23	~88%	10
PDPPBTT/ZnO	Back-gate FET	Ambipolar	SiO <sub>2</sub>	100 nm	-	-	54 %/61%	11
WSe <sub>2</sub> /h- BN/MoTe <sub>2</sub>	Back-gate FET	Ambipolar	SiO <sub>2</sub>	300 nm	900 fJ	2/-1.5, -0.3/- 0.45	~92%	12

## Table S3. Performance comparison of previously reported 2D material-based synaptic device.



**Figure S9.** Retention characteristics were modified by adjusting the base of the input pulses of the artificial synaptic transistor. For the n-type 2D Te FET, (a) EPSC curves with bases at 2 and 3 V and (b) IPSC curves with bases at 4 and 5 V (read voltage: 0.1 V, amplitude: 3 V, time duration: 100 ms). For the p-type 2D Te FET, (c) EPSC curves with bases at -3 and -4 V and (d) IPSC curves with bases at -4 and -5 V (read voltage: 0.1 V, amplitude: 3 V, time duration: 100 ms).

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