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Supplementary Information - Learning and spiking dynamics in brain-like nanoscale networks.

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S1 Model Comparison

As discussed in the main text we have used two models for the memristors that are incorporated into the base model of spiking PNNs. The Type B model captures electrically driven hillock formation [1] and the Type C model captures electrochemical behaviour. [2,3] In this section we compare the two models and, in particular, demonstrate the effect that the model parameters have on the observed hysteresis in I-V and G-V curves.

S1.1 Overview

The Type B model is a model of the electric field-driven surface diffusion processes that induce the growth of conducting 'hillocks' within the PNN tunnel gaps under low applied voltages. Networks of tunnel gaps governed by this model have been shown to act as networks of memristors and perform well in reservoir computing tasks. [1,4] It has also been shown in Ref. 4 that the Type B model is equivalent to a simple memristor model that assumes linear ionic drift in a doped semiconductor [5] up to a normalisation factor. The standard parameters (Table 1, main text) were chosen in accordance with previous work [1,6] except for the conductance scaling parameter $\alpha = 10$ Ω^{-1}, which was increased to match the filament conductance of the Type A gaps (see Section S1.4 for more detail). The characteristic time scale $T = 20$ s was also increased to slow the intrinsic time scale of the Type B memristors to better match the time scale of the Type C memristors.

In contrast to the Type B model, the Type C model is not constructed explicitly from physical processes. Instead it models the memristive behaviour of junctions in networks of nanowires (presented in Refs. 2 and 3 for ZnO and Ag nanowires, respectively) with a voltage-driven rate balance equation that accounts for effects of short term plasticity (potentiation, depression, and relaxation). The Type C model incorporates the exponential function form that is typical of electrochemical memristors; the switching kinetics in experimental electrochemical memristors have been observed to obey an exponential dependence on the applied voltage. [7] Thus this model has been chosen so that its electrochemical mechanism can be contrasted with the electric field-driven processes of the Type B model. Other models of electrochemical memristors for example combine a threshold-driven switching model with an exponential voltage-dependent tunnelling conductance equation. [8]

The parameters of the Type C model are listed in Table 1 (main text). These values were chosen such that both single Type C memristors and networks of Type C memristors displayed wide yet physically-realistic I-V and G-V hysteresis over 200 timestep voltage sweeps.

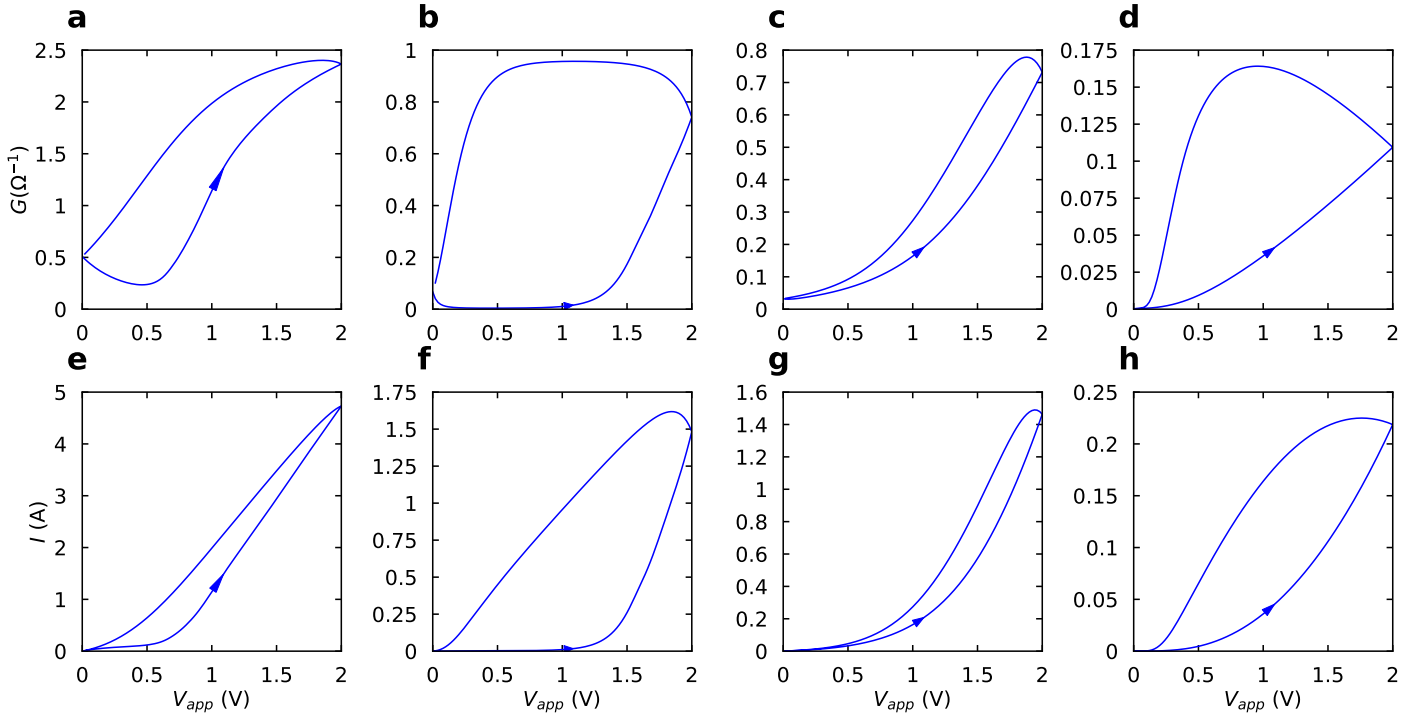

Fig. S1 A sample of possible hysteresis for networks containing 100% Type C memristors over a selection of points in the κ_0 and η parameter spaces. (a–d) The conductance-voltage (G-V) hysteresis for four different choices of parameters. (e–h) The corresponding current-voltage (I-V) hysteresis for the above G-V plots. These examples illustrate the range of memristive behaviour that is afforded by the Type C model.

S1.2 Strong Parameter Dependence of Hysteresis in Networks of Type C Memristors

An important difference between the models is that the conductance of the Type B memristors is dependent on the individual gap lengths (see Methods, Eqns. 4–6), while the state variable of the Type C memristors (and thus the conductance – see Methods, Eqns. 7–10) is only dependent on the applied voltage and not the individual gap geometries. This means the effective conductance range differs between the Type B memristors depending on the lengths of the gaps they are located in, while the Type C memristors all share the same conductance range regardless of their location. As a result, more of the Type C memristors are able to noticeably impact the dynamics of the network, since many of the Type B memristors are located in wide gaps and thus their maximum conductance is very small.

Another difference between the two selected models lies in their parameter spaces. The Type B model only possesses two parameters: one controlling the potentiation (μ) and the other controlling the depression (κ). This means that the memristive dynamics of tunnel gaps governed by this model are thus limited in their possible behaviour. In contrast, the parameter space of the Type C model affords far more flexibility in tuning the memristor behaviour. Figure S1 illustrates a series of examples of the possible hysteresis that networks with Type C memristors can be tuned to display.

S1.3 Comparison of Networks with 50% vs 100% Memristors

Figure S2 shows the network conductance and current responses to an applied voltage sweep ($V_{min} = 0$ V, $V_{max} = 2$ V, period = 200 timesteps) for (a–d) a 100% Type A gap network (solid line) and an A:B = 50:50 network (dashed line), and (e–h) a 100% Type A gap network (solid line) and an A:C = 50:50 network (dashed line). Note that the conductance and current of the A:B and A:C = 50:50 networks are scaled such that at the peak of the voltage sweep the values are equal to those of the 100% networks.

The G-V (panels (a,e)) and I-V (panels (b,f)) curves illustrate that hysteresis is present in PNNs containing differing proportions of memristors, and that the difference in hysteresis is minimal except for scaling terms to account for increasing network conductance with increasing memristor proportions.

In the A:B and A:C = 50:50 networks, the hysteresis differs depending on the specific Type A gaps that have been selected for replacement; different distributions of memristors can lead to different network memristance, especially for the Type B memristors with non-uniform conductances. When a small number of memristors are introduced into the networks, their influence can differ greatly depending on the network locations they inhabit. However, above very low memristor proportions this difference is small.

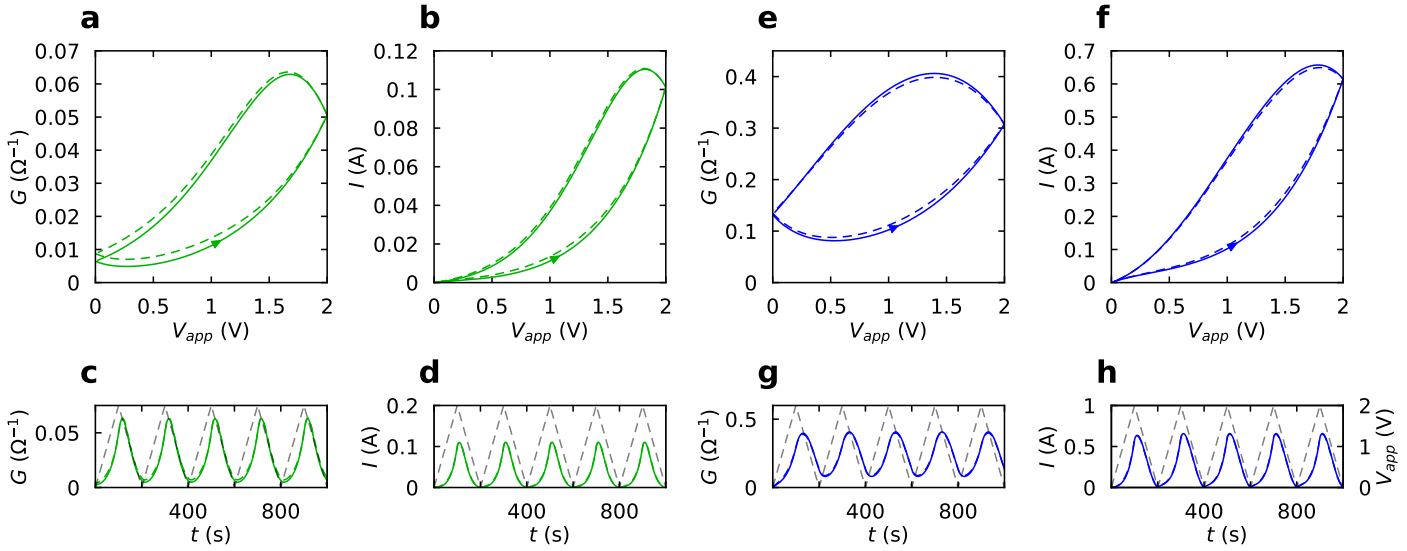

Fig. S2 Hysteresis of networks containing different proportions of memristors. (a–d) Networks with Type B memristors (green). (e–h) Networks with Type C memristors (blue). (a,e) G-V curves. (b,f) I-V curves. (c,g) G-t trace. (d,h) I-t trace. The solid (dashed) lines in (a–d) and (e–f) show the hysteretic response of networks with 100% (50%) Type B and 100% (50%) Type C memristors, respectively. Note that the dashed lines in this figure *do not* correspond to *single* memristors (as in Fig. 3 – main text), but rather *networks* with 50% Type A gaps replaced with memristors. Note for all panels the conductance and current of the A:B and A:C = 50:50 networks are scaled such that the values at the peak voltage are equal to those of the 100% networks to clearly show the hysteresis. The voltage ramps (grey dashed lines) have $V_{min} = 0$ V, $V_{max} = 2$ V, period = 200 timesteps.

S1.4 Conductance Scaling

The conductances of the Type B and Type C memristors are governed by

$$G_i = \alpha e^{-\beta(D_i - z_i)} \tag{1}$$

and

$$G(t) = G_{min}(1 - g(t)) + G_{max} g(t), \tag{2}$$

respectively (equations re-stated from main text, see Methods Eqns. 5 and 10). The relative conductances of these memristors to each other and to the Type A gaps are scaled by the values of α and G_{max}. [Note that the Type A tunnel gaps have maximum conductance $= 1\ \Omega^{-1}$ and a 'quantised' value $G_{on} = 10\ \Omega^{-1}$ when a filament is formed.[9]] Initial conductance values chosen for the Type B (Type C) memristors, $\alpha = 1\ \Omega^{-1}$ ($G_{max} = 1\ \Omega^{-1}$), were chosen to be comparable to the Type A conductances. The effect of scaling these parameter values was then investigated, and results for $\alpha = 10\ \Omega^{-1}$ and $G_{max} = 0.1\ \Omega^{-1}$ are presented here. Since the Type B memristors have non-uniform conductances, a direct comparison of their conductances relative to the uniform Type C memristors is not straightforward, and so instead we compare the resulting (relative) conductances of the networks.

Figures S3–S5 illustrate the effect on network dynamics of changing α and G_{max}. Figure S3 shows the conductance-voltage (G-V) hysteresis of networks with 100% memristors for the various parameter values. As is to be expected, the G-V curves for the networks with high-conductance memristors (bottom row) are simply scaled by an order of magnitude compared to those for low-conductance memristors (top row). Otherwise, the conductance scaling has no impact on the hysteresis of the networks – the hysteresis of networks with a lower proportions of memristors, such as A:B and A:C = 75:25 networks, is similar. [Note however that low voltages and short voltage sweeps must be used to make this comparison, to avoid spiking from the Type A gaps.]

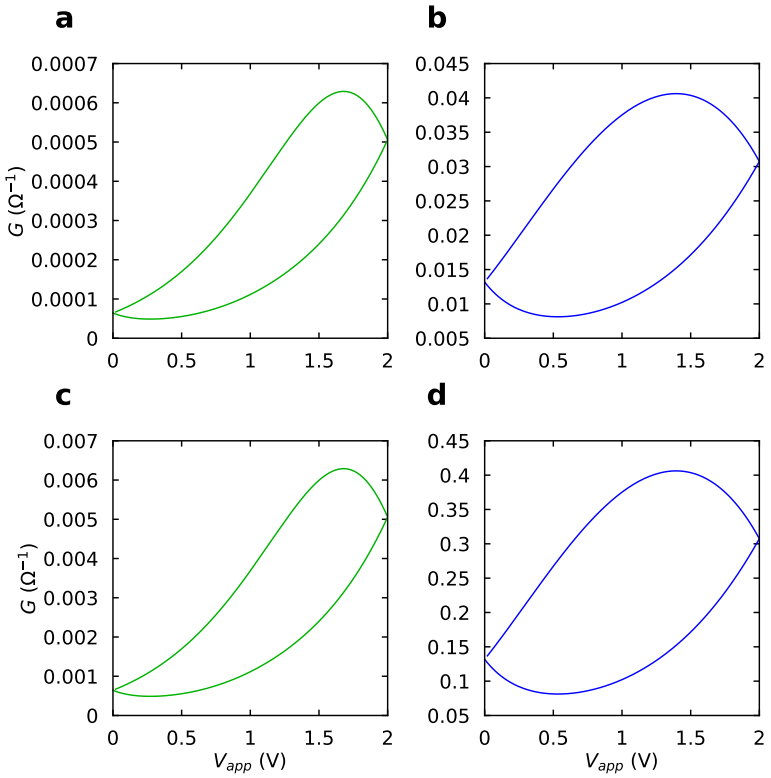

Fig. S3 Comparison of hysteresis of 100% networks of memristors for low-conductance (top row) and high-conductance (bottom row) parameters of the Type B (green, left column) and C (blue, right column) memristors. (a) The conductance-voltage (G-V) hysteresis of a network with 100% Type B memristors with $\alpha = 1\ \Omega^{-1}$. (b) The G-V hysteresis of a network of 100% Type C memristors with $G_{max} = 0.1\ \Omega^{-1}$. (c) The G-V hysteresis of a network of 100% Type B memristors with $\alpha = 10\ \Omega^{-1}$. (d) The G-V hysteresis of a network of 100% Type C memristors with $G_{max} = 1\ \Omega^{-1}$. The voltage ramps from which these hystereses were recorded have $V_{min} = 0$ V, $V_{max} = 2$ V, period = 200 timesteps.

Figure S4 compares the IEI distributions for an A:B = 75:25 network (green, left column) and an A:C = 75:25 network (blue, right column), with the same memristor conductance scaling in Fig. S3 (i.e. top row = low conductance and bottom row = high conductance). The differences in IEI distributions between the models (i.e. between the columns of the figure) are more significant than the differences between the conductance scaling (i.e. between the rows of the figure). Thus the contrast in IEI distributions between networks containing Type B memristors and those containing Type C memristors can be mainly attributed to differences between the Type B and C *models*, rather than the relative conductance scaling of the memristors.

Figure S5 shows the changes in ACFs for networks containing 25% memristors that result from the same conductance scaling as in Figs. S3 and S4 (i.e. the memristors in the networks are ordered by left column = Type B, right column = Type C, top row = low conductance, bottom row = high conductance). Similarly to Fig. S4, the difference in ACFs between the models (left column vs right column) is more significant than the differences between the conductance scaling (top row vs bottom row). This is further evidence that the contrast in spiking dynamics in networks containing the two memristor types is due to differences in the models rather than their relative conductances.

For the Type B memristors, the parameter value $\alpha = 10\ \Omega^{-1}$ was motivated as the final choice as it matches the conductance of the Type A gaps when a filament is formed, and for the Type C memristors the value $G_{max} = 1\ \Omega^{-1}$ was retained from the initial choice for simplicity. These conductance values also result in similar spiking event rates at equal applied voltages in networks containing Type B and C memristors, which ensure a fair comparison of the spiking dynamics of these networks.

The non-uniformity of the Type B memristors means that while a few reach higher conductances than the Type C memristors (see Figs. S12 and S13 below), the presence of relatively large gaps elsewhere in the network ensure that the average conductances are lower. This difference appears in the G and I scales of Fig. 3 (main paper) and in comparison of Fig. 7 (main paper) and Fig. S15, but in general the choice of memristor (Type B or C) does not strongly affect either the network conductance or observed event rate. This means the choice of parameters for the two models ($\alpha = 10\ \Omega^{-1}$ and $G_{max} = 1\ \Omega^{-1}$, respectively) is appropriate, and that the differences seen in Figs. 5 and 6 (main text) arise from the different memristive behaviour intrinsic to the two models, *not* to a mismatch in conductance parameters.

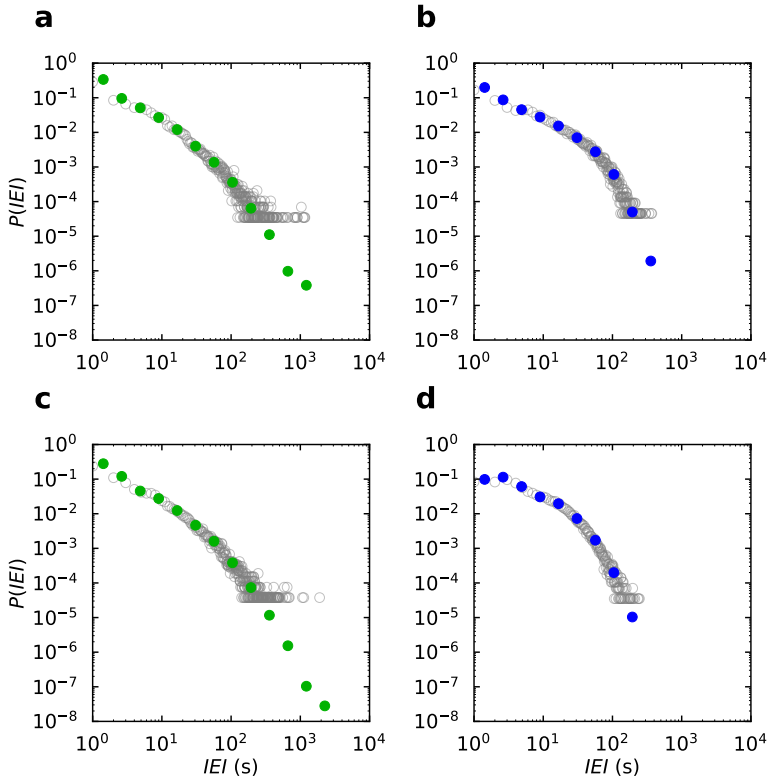

Fig. S4 Comparison of inter-event interval (IEI) probability density functions (PDFs) of networks with 25% memristors for low-conductance (top row) and high-conductance (bottom row) parameters of the Type B (left column) and C (right column) memristors. (a) The IEI distribution of a network with 100% Type B memristors with $\alpha = 1\ \Omega^{-1}$. (b) The IEI distribution of a network of 100% Type C memristors with $G_{max} = 0.1\ \Omega^{-1}$. (c) The IEI distribution of a network of 100% Type B memristors with $\alpha = 10\ \Omega^{-1}$. (d) The IEI distribution of a network of 100% Type C memristors with $G_{max} = 1\ \Omega^{-1}$. Linear-binned PDFs are plotted in grey, while logarithmic-binned PDFs are plotted in (a–b) green for the Type B networks and (c–d) blue for the Type C networks. The spiking event trains from which the IEIs were calculated were recorded as the final 400,000 timesteps of 500,000 timestep 2.5 V simulations.

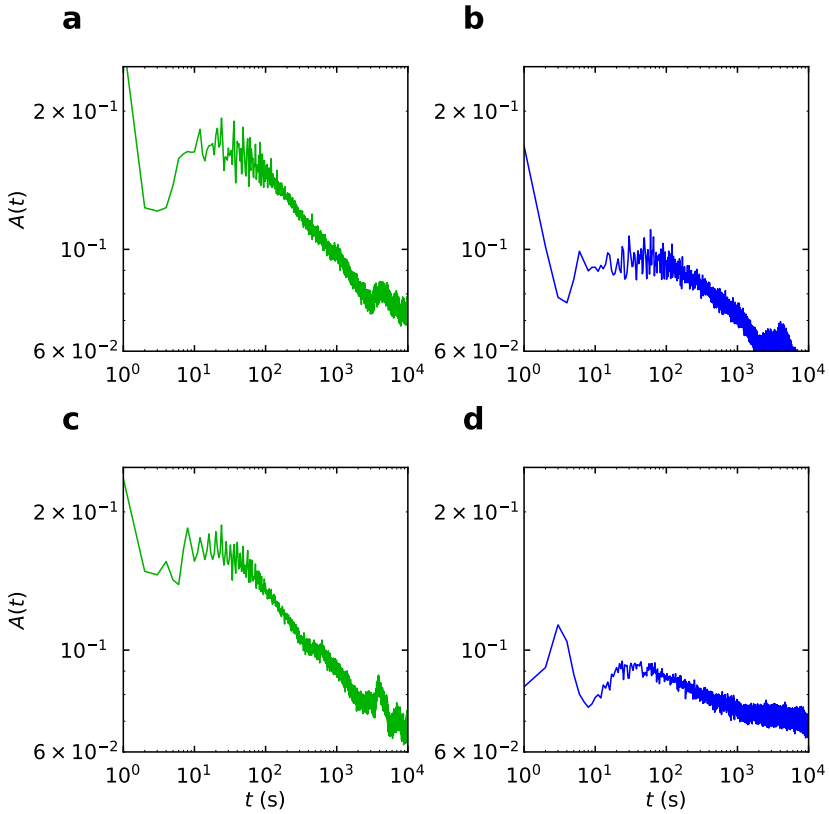

Fig. S5 Comparison of autocorrelation functions (ACFs) of networks with 25% memristors for low-conductance (top row) and high-conductance (bottom row) parameters of the Type B (left column) and C (right column) memristors. (a) The ACF of a network with 100% Type B memristors with $\alpha = 1\ \Omega^{-1}$. (b) The ACF of a network of 100% Type C memristors with $G_{max} = 0.1\ \Omega^{-1}$. (c) The ACF of a network of 100% Type B memristors with $\alpha = 10\ \Omega^{-1}$. (d) The ACF of a network of 100% Type C memristors with $G_{max} = 1\ \Omega^{-1}$. The spiking event trains from which the ACFs were calculated were recorded as the final 400,000 timesteps of 500,000 timestep 2.5 V simulations.

S2 Hysteresis of Individual Gaps

In this section we present the individual memristor hysteresis of the memristors that achieve the 1^{st}, 50^{th}, and 100^{th} highest gap voltages V_g at the peak of an applied voltage sweep ($V_{min} = 0$ V, $V_{max} = 2$ V, period = 200 timesteps). Note in this section that the subscript '$_g$' denotes a value associated with a single memristor *within a network*.

Figure S6 shows the voltage distributions (panel (a)) and the gap voltage-network voltage ($V_g - V_{app}$) hysteresis (panel (b)) of selected Type B memristors during an applied voltage sweep in an A:B = 50:50 network. The selected memristors are the ones that achieve the 1^{st}, 50^{th}, and 100^{th} highest gap voltages V_g at the sweep peak. These panels illustrate the varying dynamics between Type B memristors in the same network; in particular, note in panel (b) the overlapping $V_g - V_{app}$ hysteresis loops of the memristors with the 50^{th} (cyan) and 100^{th} (lime green) peak V_g values in the network. This overlap is an example of the complex dynamics that can emerge within the PNNs.

Figure S7 shows the individual current-memristor voltage ($I_g - V_g$) loops of the same selected Type B memristors shown in Fig. S6. Note the current scales of each hysteresis loop; the panels are ordered (a) to (c) by increasing peak memristor voltage V_g, but the magnitude of the peak current I_g is not ordered the same. This is a further example of the non-uniform conductances of the Type B memristors. Also note the relative differences between the shapes of the hysteresis loops in these panels.

Figure S8 shows the voltage distributions (panel (a)) and the gap voltage-network voltage ($V_g - V_{app}$) hysteresis (panel (b)) of selected Type C memristors during an applied voltage sweep in an A:C = 50:50 PNN. The selected memristors are the ones that achieve the 1^{st}, 50^{th}, and 100^{th} highest gap voltages V_g at the sweep peak. These panels illustrate the varying dynamics between Type C memristors in the same network; in particular, again note in panel (b) the overlapping $V_g - V_{app}$ hysteresis loops of the memristors with the 50^{th} (dark blue) and 100^{th} (cyan) peak V_g values in the network.

Figure S9 shows the individual current-memristor voltage ($I_g - V_g$) loops of the same selected Type C memristors shown in Fig. S8. Note that for these memristors, the magnitudes of the current flows *are* correlated with increased peak memristor voltage V_g; as V_g increases from panels (a) to (c), so too does the current flow through the memristor. This is further evidence of the uniformity of Type C memristors. Also note the relative similarity between the shapes of the hysteresis loops. However, a spike can be observed in the $I_g - V_g$ loop in panel (b) at around $V_g = 0.15$ V on the up-sweep, and this spike is not observable in the other panels.

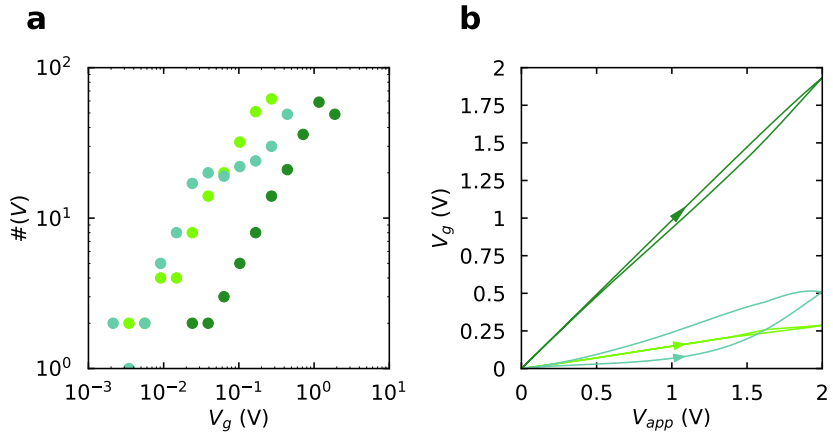

Fig. S6 Voltages across selected memristors in an A:B = 50:50 PNN during a single voltage cycle. (a) Distribution of measured voltages V_g in selected gaps during the cycle. (b) Hysteresis of V_g as a function of V_{app} in the selected gaps during the cycle. The differing observed hysteresis loops highlight the complex network behaviour. The selected memristors were the ones with the 100^{th} greatest (lime green), 50^{th} greatest (cyan), and 1^{st} greatest (dark green) gap voltages V_g at the applied voltage cycle peak. The voltages were recorded during a voltage sweep with $V_{min} = 0$ V, $V_{max} = 2$ V, period = 200 timesteps.

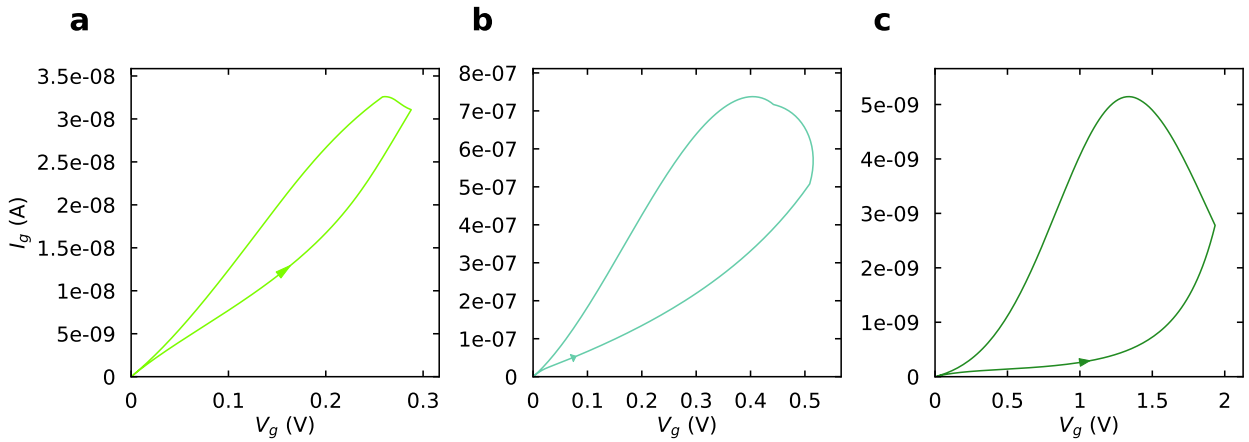

Fig. S7 $I_g - V_g$ hysteresis for the same selected Type B memristors as in Fig. S6. (a) The hysteresis of the memristor with the 100^{th} greatest V_g in the network at the applied voltage cycle peak. (b) The hysteresis of the memristor with the 50^{th} greatest V_g in the network. (c) The hysteresis of the memristor with the 1^{st} greatest V_g in the network. Note the varying shapes of the hysteresis.

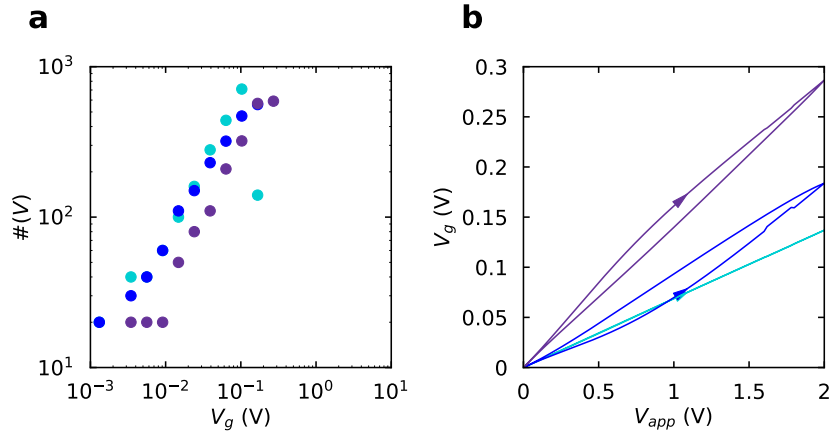

Fig. S8 Voltages across selected memristors in an A:C = 50:50 PNN during a single voltage cycle. (a) Distribution of measured voltages V_g in selected gaps during the cycle. (b) Hysteresis of V_g as a function of V_{app} in the selected gaps during the cycle. The differing observed hysteresis loops highlight the complex network behaviour. The selected memristors were the ones with the 100^{th} greatest (cyan), 50^{th} greatest (dark blue), and 1^{st} greatest (purple) gap voltages V_g at the applied voltage cycle peak. The voltages were recorded during a voltage sweep with $V_{min} = 0$ V, $V_{max} = 2$ V, period = 200 timesteps.

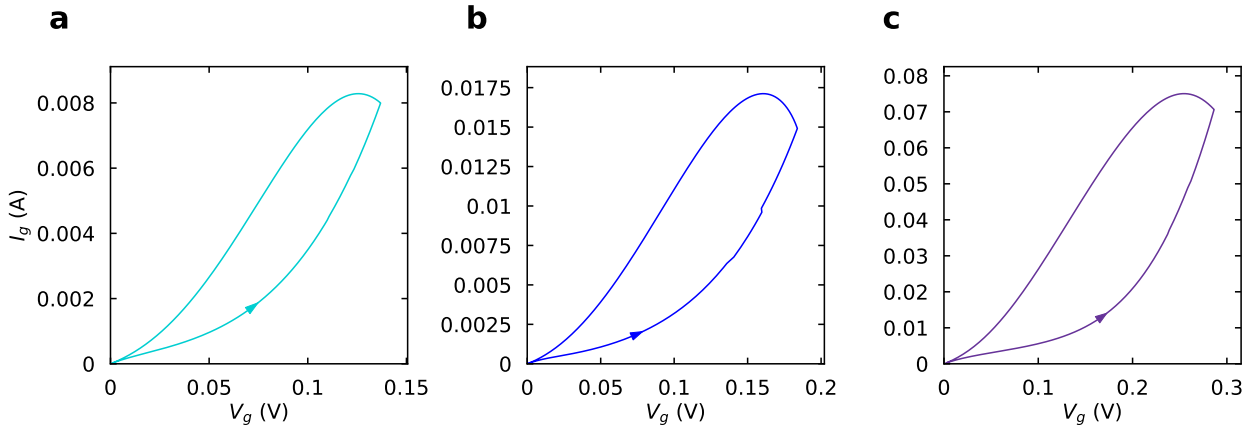

Fig. S9 $I_g - V_g$ hysteresis for the same selected Type C memristors as in Fig. S8. (a) The hysteresis of the memristor with the 100^{th} greatest V_g in the network at the applied voltage cycle peak. (b) The hysteresis of the memristor with the 50^{th} greatest V_g in the network. (c) The hysteresis of the memristor with the 1^{st} greatest V_g in the network. Note the varying shapes of the hysteresis.

S3 Detailed Comparison of Networks of Type B and C Memristors

This section discusses in detail the differences between networks containing Type B and Type C memristors, and focuses in particular on the distribution of voltage, current and conductances for all memristors in the networks.

S3.1 Voltage and Conductance Distributions

Figure S10 shows the distribution of gap voltages (in which memristors are located) in networks where different proportions (25% in panel (a) and 50% in panel (b)) of Type A gaps have been replaced with Type B (green) and Type C (blue) memristors. The distributions of voltages illustrate the different impact of the two memristor models on the network dynamics. The distribution for networks with Type B memristors extends to higher voltages, and appears to be close to a power law, i.e. in a small number of instances a handful of Type B memristors achieve very high voltages and thus likely dominates dynamics of the network. In comparison, the range of Type C voltages is smaller, consistent with a more homogeneous distribution of their properties, as discussed in Section S1. Figure S11 shows similar distributions of voltages are obtained during a voltage sweep. The main difference is that the distributions for networks with Type B memristors more closely follow a power law distribution, which is consistent with critical dynamics.

Figure S12 shows the distributions of Type B (green) and Type C (blue) memristor conductances in networks containing 25% memristors (panel (a)) and 50% memristors (panel (b)). In this example, high-conductance values were chosen, i.e. $\alpha = 10\ \Omega^{-1}$ ($G_{max} = 1\ \Omega^{-1}$) for the Type B (Type C) model. These conductances were recorded during a long simulation with a constant applied network voltage of 2 V. All four distributions in both panels resemble power laws over multiple decades, consistent with the scale-free topology of the PNNs.[10] However, the distributions of the Type B conductances (green) follow power laws more closely over a wider range (since their conductances are dependent on tunnel gap sizes, which have themselves have a broad distribution).

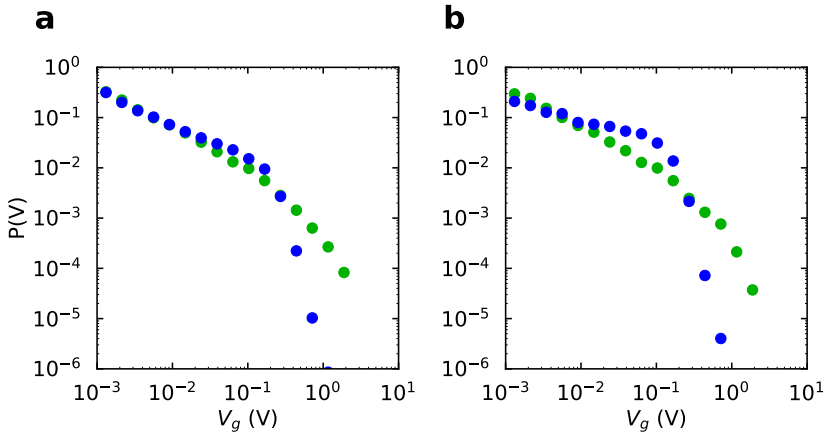

Fig. S10 Distribution of voltages (V_g) across individual memristors within simulated PNNs for constant $V_{app} = 2$ V. (a) Probability density function (PDF) for Type B (green) and Type C (blue) memristors within 25% networks. (b) Corresponding data for 50% networks. These voltages were recorded during the final 400,000 timesteps of 500,000 timestep simulations.

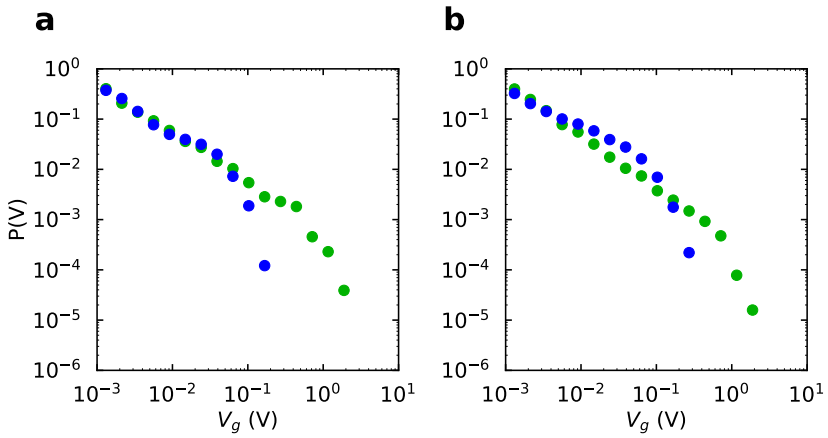

Fig. S11 Distribution of voltages across the memristors within simulated PNNs during a voltage sweep. Details are as for Fig. S10 except that the voltages were recorded during a voltage sweep with $V_{min} = 0$ V, $V_{max} = 2$ V, period = 200 timesteps.

Figure S13 shows the distribution of Type B (green) and Type C (blue) memristor conductances in networks containing 25% memristors (panel (a)) and 50% memristors (panel (b)) during a voltage sweep. The conductance parameter values are the same as in Fig. S12. These conductances were recorded during a voltage sweep with $V_{min} = 0$ V, $V_{max} = 2$ V, period = 200 timesteps. Similarly to Fig. S12, the Type B conductance distributions follow a power law over a large range with high maximum conductances, while the Type C distributions follow a power law over a narrower range. Hence the distribution of conductance values is not significantly affected by the number of memristors that are inserted into the networks. This is an explicit illustration that the range of Type B conductances is larger than the Type Cs; some Type Bs reach very high conductances, but on average the Type Cs (over a narrower range) have greater conductances.

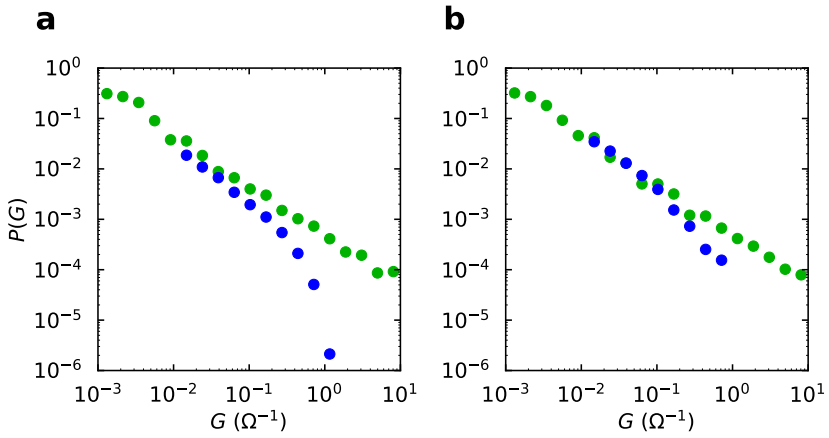

Fig. S12 Distributions of memristor conductances within PNNs for a simulation with a constant applied voltage (2 V). (a) The conductance PDFs of Type B (green) and Type C (blue) memristors within 25% networks. (b) The conductance PDFs of Type B (green) and Type C (blue) memristors within 50% networks. These conductances were recorded during the final 400,000 timesteps of 500,000 timestep simulations with constant applied network voltages of $V_{app} = 2$ V. The Type C distributions (blue) have been scaled to allow better comparison between the models.

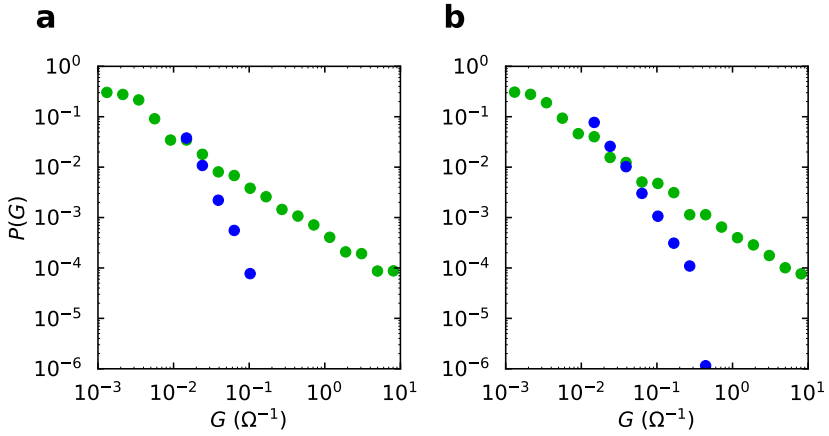

Fig. S13 Distributions of memristor conductances within PNNs during a voltage sweep ($V_{min} = 0$ V, $V_{max} = 2$ V, period = 200 timesteps). (a) The conductance PDFs of Type B (green) and Type C (blue) memristors within 25% networks. (b) The conductance PDFs of Type B (green) and Type C (blue) memristors within 50% networks. The Type C distributions (blue) have been scaled to allow better comparison between the models.

S3.2 Ordered Voltage and Current Distributions

Figure S14 shows the ordered voltages and currents (panels (a–b) and (c–d), respectively) through memristors in an A:B = 75:25 PNN (panels (a,c)) and an A:C = 75:25 PNN (panels (b,d)). The voltages and currents were recorded at the peak voltage of a 200 timestep 0-2 V voltage sweep. A selection of memristors are marked by their voltage in panels (a–b), and their corresponding currents are marked in panels (c–d) for comparison. This marking highlights the conductance non-uniformity of the Type B memristors and the uniformity of the Type C memristors. Note that the order of the coloured markers differs greatly between panels (a) and (c) for the Type B memristors, whereas the markers are in an identical order in panels (b) and (d) for the Type C memristors. The Type C voltage and current distributions are also of very similar shape in panels (b) and (d), whereas the distribution shapes further differ between panels (a) and (c) for the Type B memristors. This further highlights the conductance non-uniformity of the Type B memristors.

Further note the difference in voltage and current magnitudes between the memristor models. For the Type B memristors, in panel (a) the highest voltages are greater (up to 2 V) than the highest voltages of the Type C memristors in panel (b) (up to 0.175 V). However, the inverse is true for the memristor currents; in panel (c) the highest currents are less ($\sim 8 \times 10^{-4}$ A) than the highest currents of the Type C memristors (~ 0.0175 A).

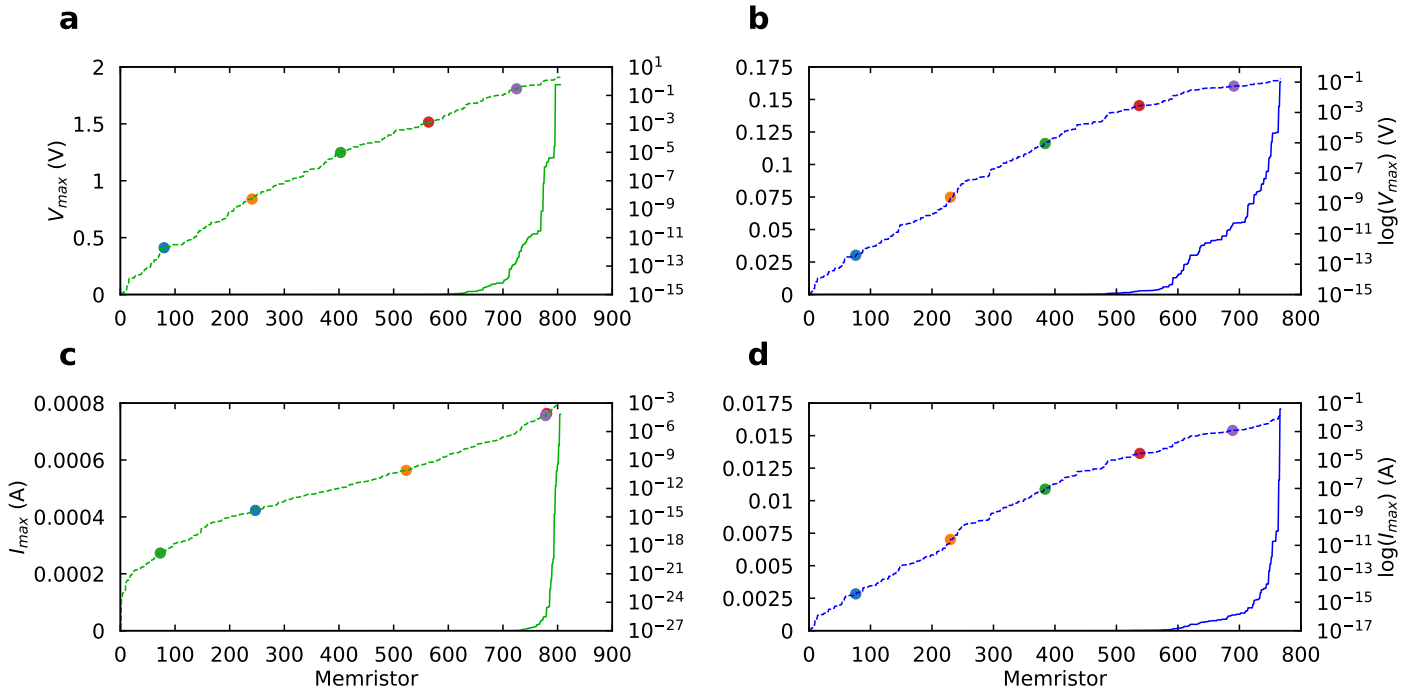

Fig. S14 The ordered distributions of (a–b) memristor voltages and (c–d) memristor currents in (a,c) an A:B = 75:25 network and (b,d) an A:C = 75:25 network. The solid lines correspond to the linear axes (left axes) while the dashed lines correspond to the logarithmic axes (right axes). Five individual memristors have been highlighted on the logarithmic axes as shown by the coloured markers in panels (a) and (b), and the corresponding currents flowing through these memristors are marked in panels (c) and (d). The voltages and currents were measured at the peak of a voltage sweep with $V_{min} = 0$ V, $V_{max} = 2$ V, period = 200 timesteps, and memristors with voltages less than 10^{-15} V have been excluded.

S4 Plasticity

The potentiation and de-potentiation of large (800×800) networks containing Type C memristors was described in Section 2.6 of the main text. Larger networks were used for those simulations in order to reduce the stochasticity that is observed in smaller (200×200) networks. For completeness, in this section we present (i) results for potentiation of large networks containing Type B memristors, showing that similar effects are observed as for Type C memristors (ii) for smaller networks containing Type B and Type C memristors, showing the stochasticity in small devices, and (iii) an explicit demonstration of de-potentiation effects.

S4.1 Potentiation in Large Networks Containing Type B Memristors

Figure S15 shows an example of potentiation of a larger (800×800) A:B = 75:25 network. The essential results are similar to those shown in Fig. 7 (main text): repeated voltage pulses lead to increases in both the average network conductance ($\langle G \rangle$) and average event rate ($\langle ER \rangle$) that are 'remembered' from pulse to pulse.

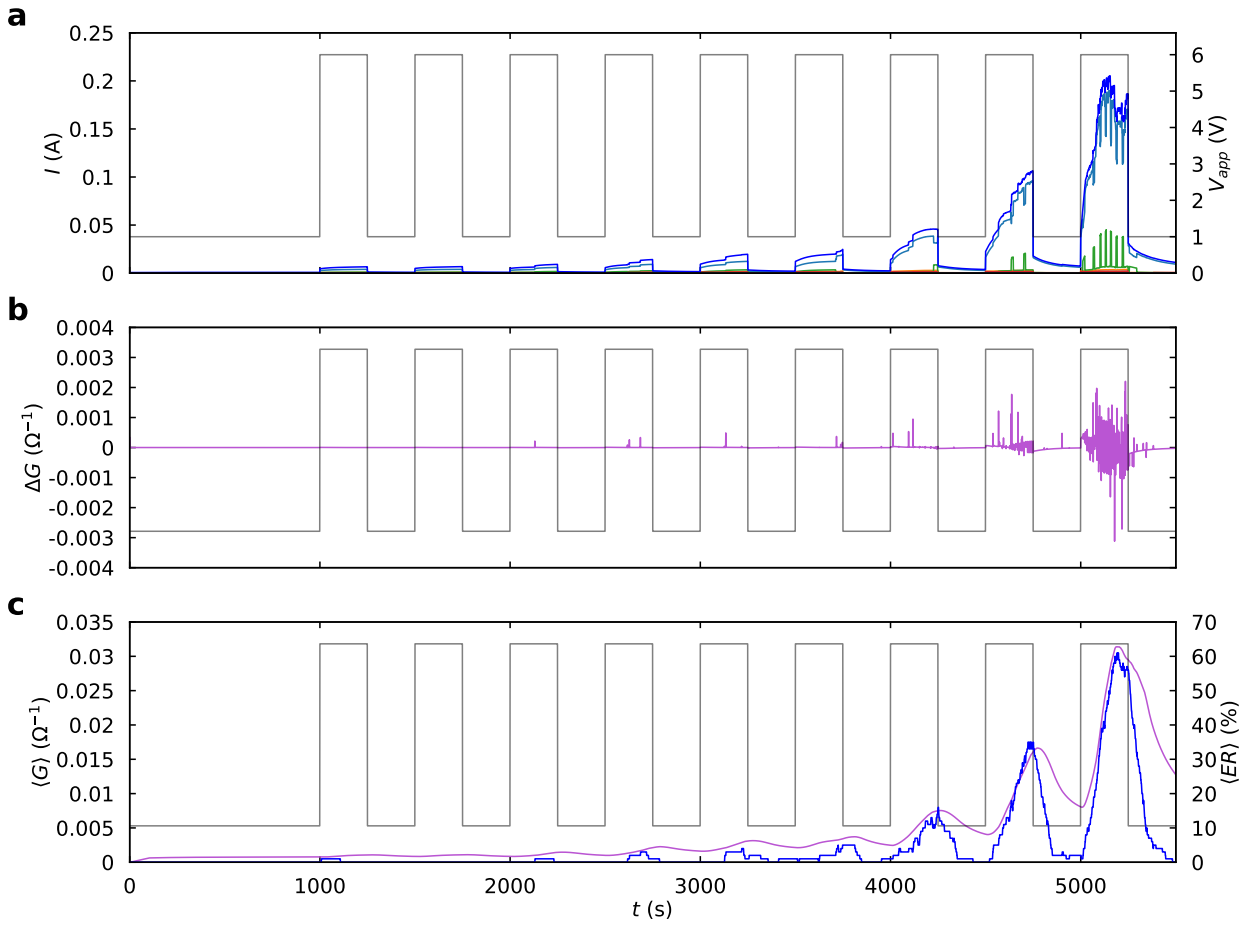

Fig. S15 Demonstration of potentiation effects within an A:B = 75:25 network. (a) The total output current (blue) and output currents from individual groups (other colours) as a function of time. The applied voltage V_{app} ($V_{min} = 1$ V, $V_{max} = 6$ V, pulse length = pulse spacing = 250 timesteps) is plotted in grey in all panels. (b) The corresponding changes in conductance ΔG, showing that amplitude and frequency of spikes increases for successive input pulses. (c) Moving averages (over 100 timesteps) of the network conductance ($\langle G \rangle$, purple) and network event rate ($\langle ER \rangle$, blue). The PNN is 800×800 pd in size.

S4.2 Potentiation in Small Networks Containing Type B Memristors

Figure S16 shows an example of potentiation of a smaller (200×200) A:B = 75:25 network. The stochastic effect of the Type A gap spiking is amplified in the smaller network, but the overall potentiation effect is still clear as repeated voltage pulses lead to increases in both $\langle G \rangle$ and $\langle ER \rangle$ that are 'remembered' from pulse to pulse. Note the different applied voltage pulses: in this case, $V_{max} = 8$ V, and the pulses are 1,000 timesteps long and separated by 1,000 timesteps. Also note the reduced event rate, which is the result of the smaller network; fewer Type A gaps means fewer spiking events.

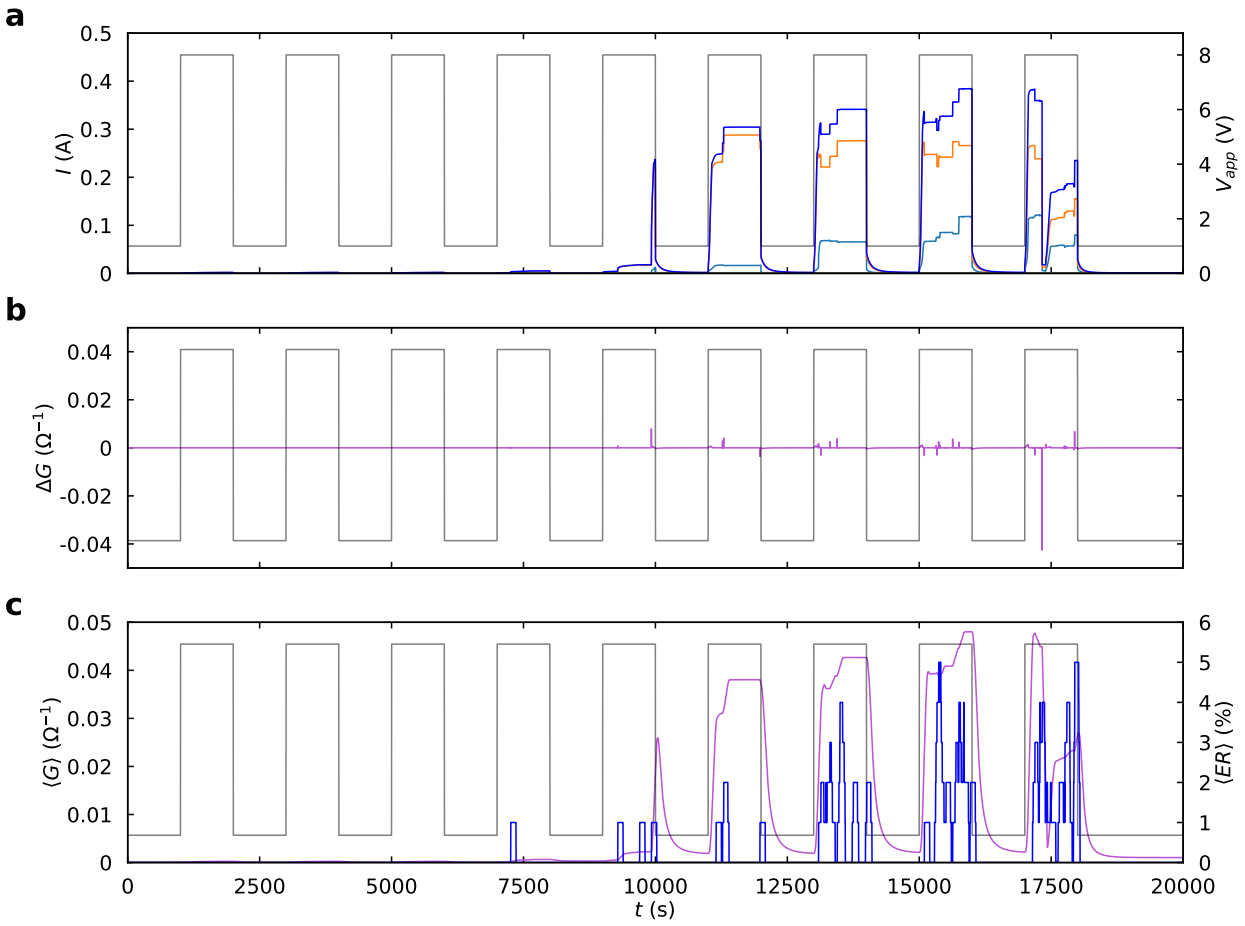

Fig. S16 Demonstration of potentiation effects within an A:B = 75:25 network. (a) The total output current (blue) and output currents from individual groups (other colours) as a function of time. The applied voltage V_{app} ($V_{min} = 1$ V, $V_{max} = 8$ V, pulse length = pulse spacing = 1,000 timesteps) is plotted in grey in all panels. (b) The corresponding changes in conductance ΔG, showing that amplitude and frequency of spikes increases for successive input pulses. (c) Moving averages (over 100 timesteps) of the network conductance ($\langle G \rangle$, purple) and network event rate ($\langle ER \rangle$, blue). The PNN is 200×200 pd in size.

S4.3 Potentiation in Small Networks Containing Type C Memristors

Figure S16 shows an example of potentiation of a smaller (200×200) A:C = 75:25 network. The stochastic effect of the Type A gap spiking is again amplified in the smaller network, but the overall potentiation effect is still clear as repeated voltage pulses lead to increases in both $\langle G \rangle$ and $\langle ER \rangle$ that are 'remembered' from pulse to pulse. Note the different applied voltage pulses: in this case the pulses are 500 timesteps long and separated by 250 timesteps. Again, note the reduced spiking event rate.

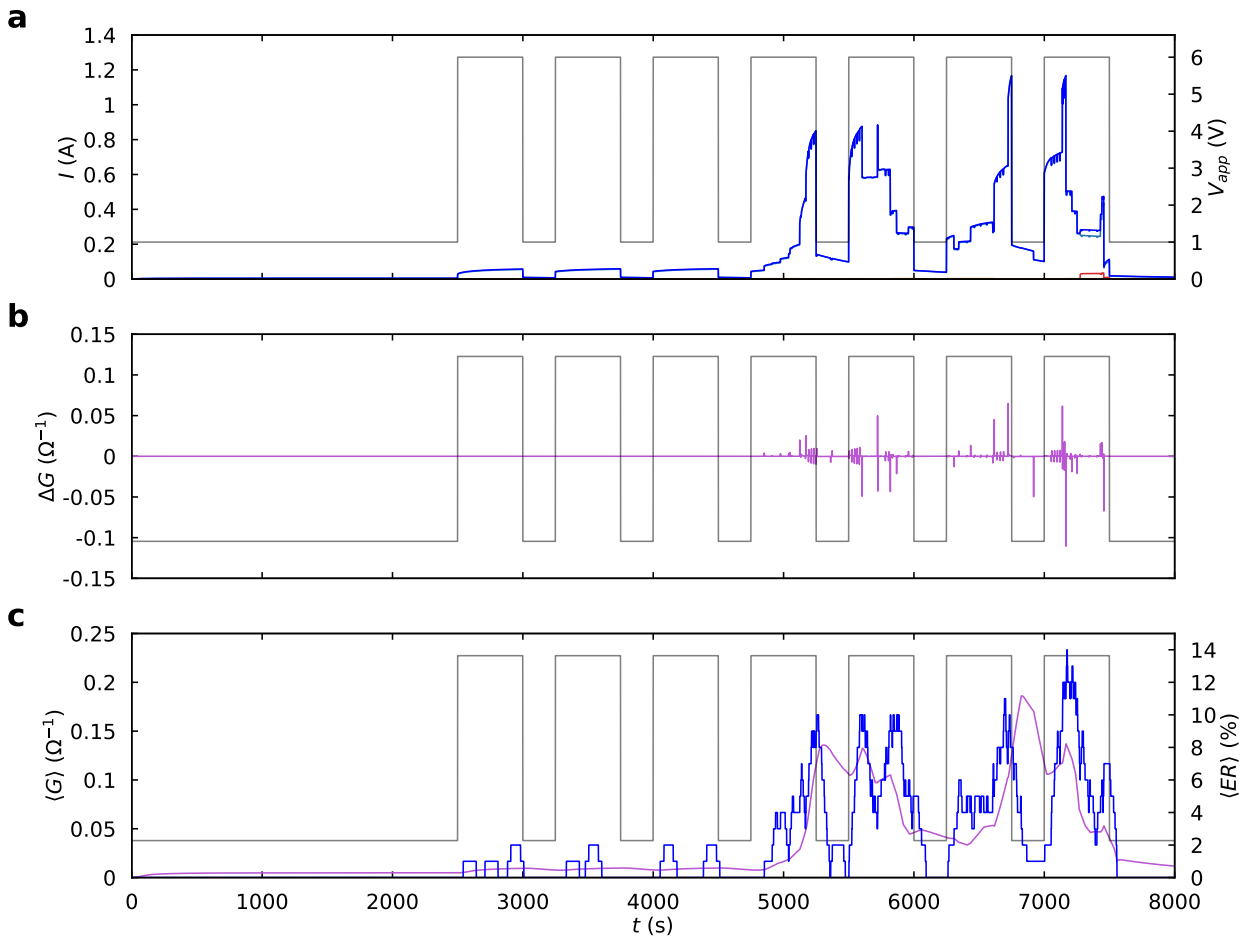

Fig. S17 Demonstration of potentiation effects within an A:C = 75:25 network. (a) The total output current (blue) and output currents from individual groups (other colours) as a function of time. The applied voltage V_{app} ($V_{min} = 1$ V, $V_{max} = 6$ V, pulse length = 500 timesteps, pulse spacing = 250 timesteps) is plotted in grey in all panels. (b) The corresponding changes in conductance ΔG, showing that amplitude and frequency of spikes increases for successive input pulses. (c) Moving averages (over 100 timesteps) of the network conductance ($\langle G \rangle$, purple) and network event rate ($\langle ER \rangle$, blue). The PNN is 200×200 pd in size.

S4.4 De-potentiation

In this section we clarify de-potentiation effects in the large (800×800) A:C = 75:25 networks discussed in the main paper (Section 2.6). Similar results are obtained for the networks discussed in Sections S4.1 – S4.3 but for the sake of brevity those results are not shown here.

Figure S18 shows the transient nature of the potentiation effect induced in an A:C = 75:25 network. In panels (a) and (b), seven voltage pulses (which are identical to the pulses in Fig. 7 in the main paper) potentiate the PNN. Figure S18a shows that the network remains potentiated (i.e. it responds similarly) for further pulses with an increased spacing. On the other hand Figure S18b shows a smaller response if there is a large delay before a single later pulse is applied (compare the event rates in panels (a) and (b) at ∼9500 s). For comparison, in panel (c) no initial potentiating pulses are applied, showing that the response of an un-potentiated network to the later pulse is minimal. Note that similar potentiation and de-potentiation effects observed in both the current and event rate.

The comparison of all three panels in Fig. S18 highlights how the potentiation induced with initial voltage pulses can be sustained with continued stimulus, but will de-potentiate over time if insufficient stimulus is applied. This de-potentiation corresponds to brain-like 'forgetting' in the PNN, which is equally important to memory formation as 'learning'.[11]

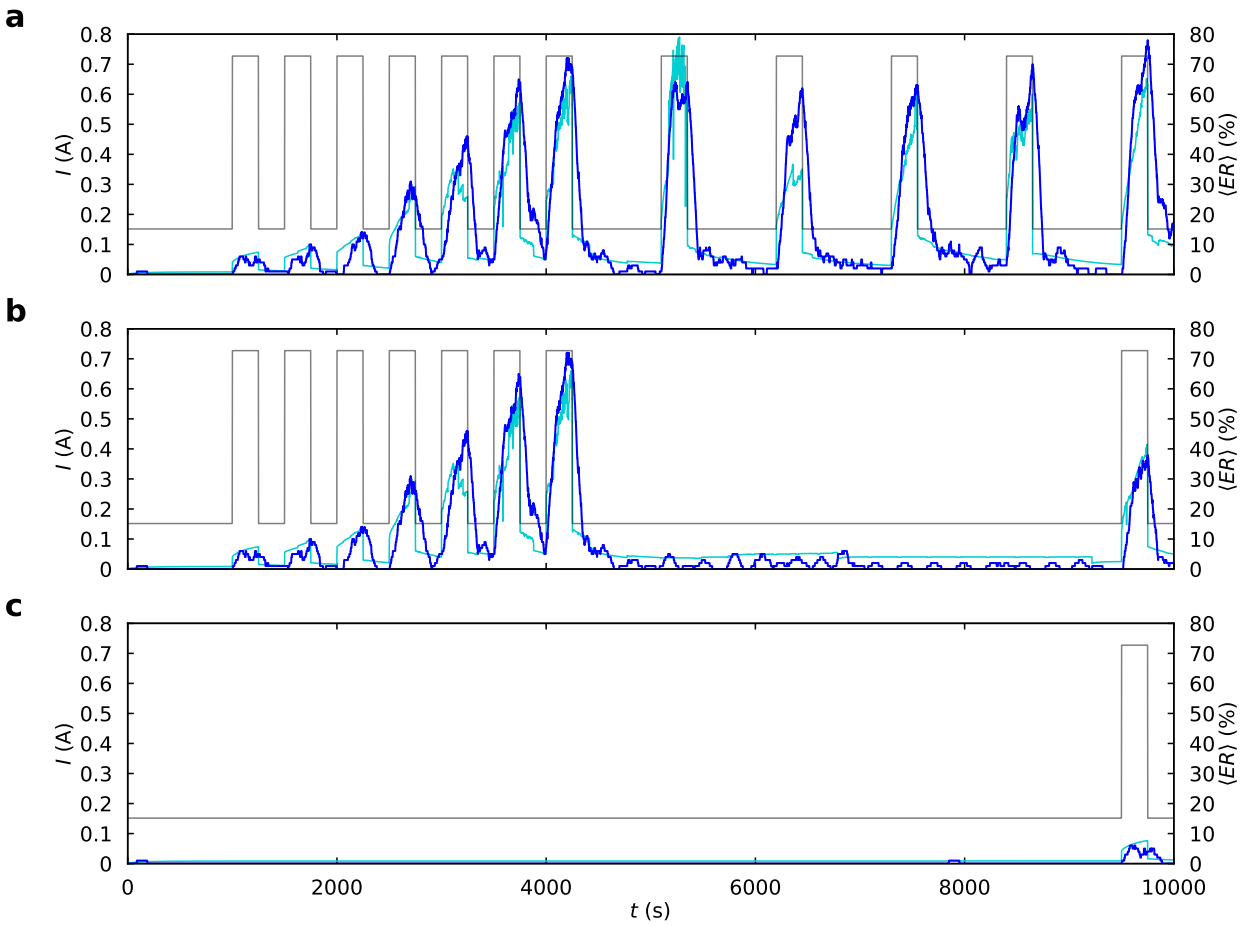

Fig. S18 Demonstration of depression effects within an A:C = 75:25 network. (a) Network response to seven initial voltage pulses and five subsequent pulses separated by 850 timesteps. (b) Network response to seven initial voltage pulses and a single subsequent pulse after a 5,250 timestep gap (at timestep 9,500). (c) Network response to a single voltage pulse after 9,500 timesteps. The total current sum of the PNN output groups is plotted in cyan and the 100 timestep moving average of the event rate ($\langle ER \rangle$) is plotted in blue. The PNN is 800×800 pd in size. The voltage applied to the input electrode is plotted in grey but not associated with either vertical axis; all pulses are $V_{min} = 1.25$ V to $V_{max} = 6$ V. The initial voltage pulses shown in (a–b) are separated by 250 timesteps, and all pulses are 250 timesteps long.

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