Supplementary material

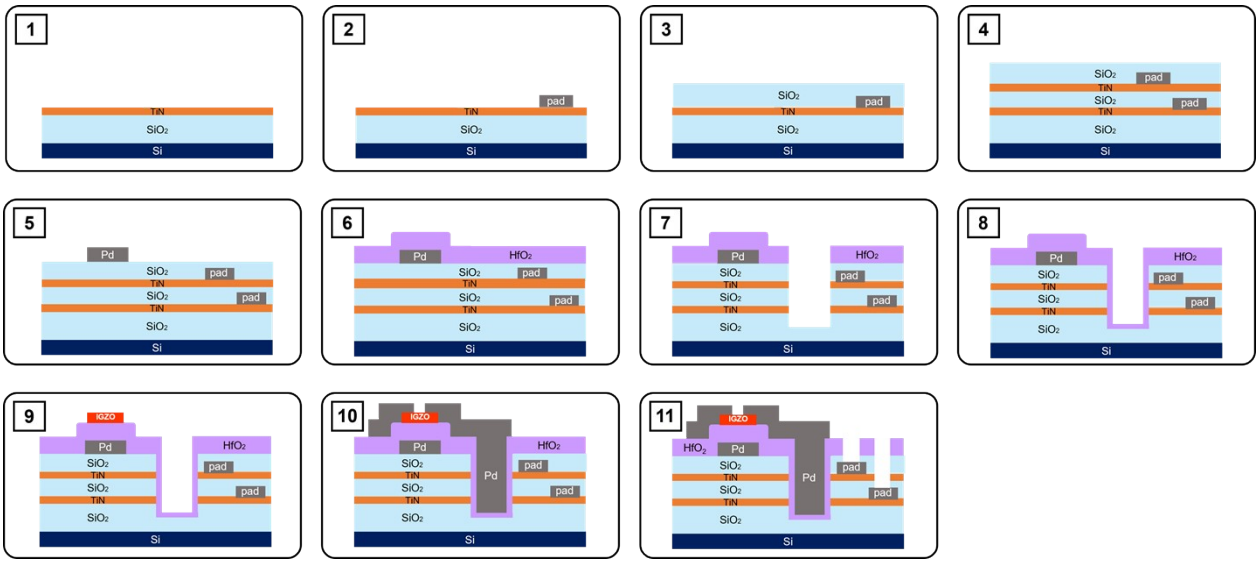

Figure S1. Step-by-step process for constructing a 3D VRRAM that is combined with an oxide FET.

Fabrication process

The step-by-step fabrication process: 1) TiN (7nm) electrode is deposited using PVD on a standard Si/SiO_2 wafer; 2) Pt (20 nm) pads are deposited on top of TiN using PVD; 3) SiO_2 (25 nm) passivation layer deposited using CVD; 4) Steps (1) – (3) are repeated until the target level of stacks is achieved; 5) Pd (30 nm) acting as a local back gate with Cr (5 nm) adhesion layer deposited using PVD; 6) HfO_x (30 nm) dielectric material by ALD; 7) Making a trench utilizing an etching procedure; 8)HfO_x (5 nm) as a switching layer utilizing ALD; 9) IGZO (13 nm) via sputtering and its pattering using H_2SO_4; 10) Deposition of Pd (90 nm) source, drain and metal electrode on top of Ti (2 nm) adhesion layer; 11) Utilizing etching to open pathways to bottom layers.

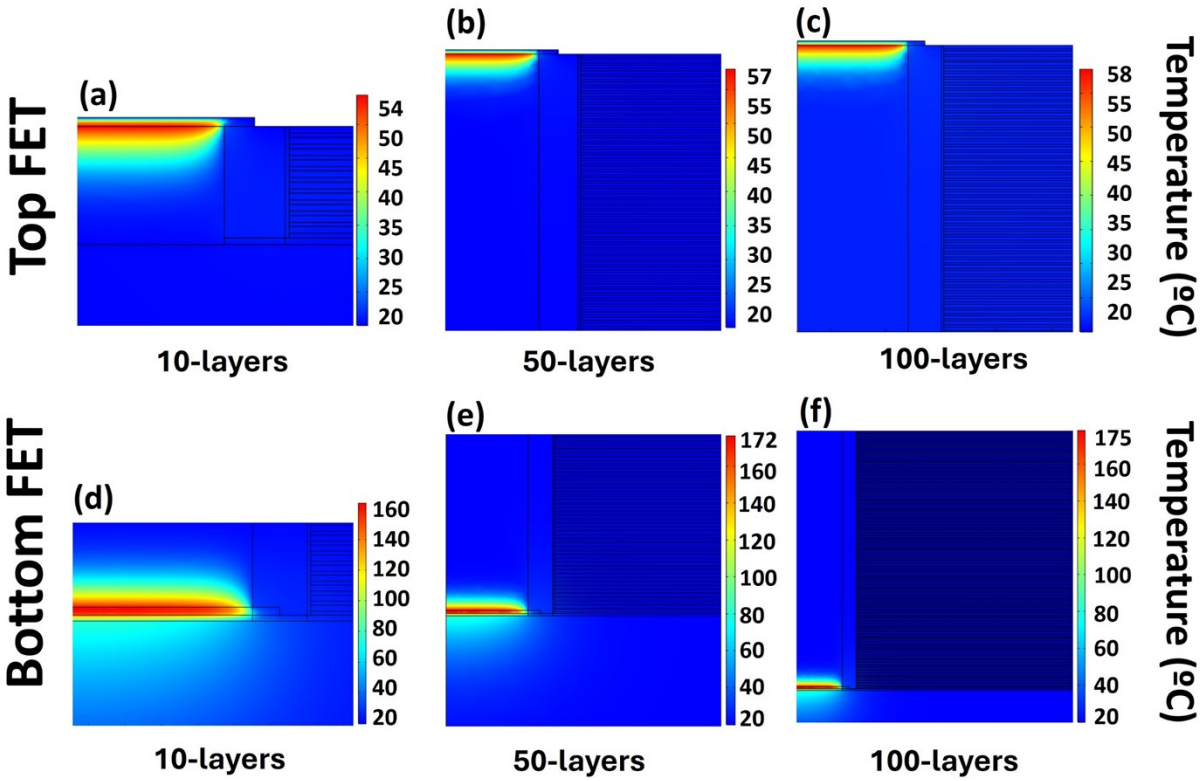

Figure S2. Temperature distribution for Top and Bottom FET configurations with different layer compositions

For the Top FET model maximum temperatures achieved were 54, 57 and 58 ºC within one 20 ns pulse. For the Bottom FET model maximum temperatures achieved were 163, 172 and 175 ºC within one 20 ns pulse.

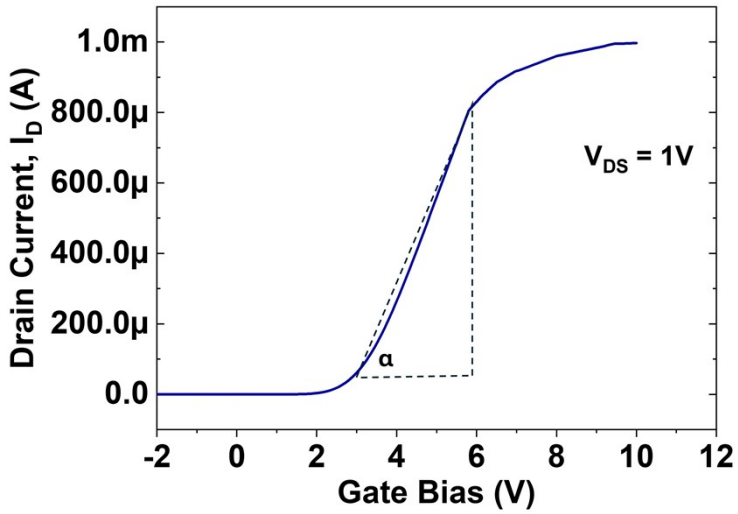

Figure S3. Drain current during gate voltage sweep

To calculate the mobility of the FET it is possible to use linear region of the $I_D - V_{GS}$ plot:[1]

$$\mu = m_{lin} \times \frac{L}{W} \times \frac{1}{V_{DS}} \times \frac{1}{C_i} \qquad (1)$$

Where m_{lin} = tan α, L – channel length, W - channel width, C_i - gate insulator capacitance per unit area. From this equation the mobility is estimated to be µ = 18.16 $cm^2/(V*s)$.

Notes and references

1. Y. Zhou, X. Wang and A. Dodabalapur, *Advanced Electronic Materials*, 2023, **9**, 2200786.