Supplementary material:

Temperature-dependent Resistive Switching Statistics and Mechanisms in Nanoscale ~~Silicon Oxide~~ Graphene-SiO_2-Graphene Memristors

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1.Estimate the graphene nanogap size ~~using Simmons' model~~

After the electromigration of graphene nanoconstriction, the tunneling current is measured as plotted in Fig. S1(red dots). In Simmons model[1], the tunneling current at the low bias$(V < \Phi/e)$ is expressed by the Simmons' equation:

$$I = \frac{qA}{4\pi^2\hbar d^2}\left\{\begin{array}{l}\left(\Phi - \frac{eV}{2}\right)exp\left[-\frac{2d\sqrt{2m_e}}{\hbar}\times\sqrt{\Phi - \frac{eV}{2}}\right] \\ -\left(\Phi + \frac{eV}{2}\right)exp\left[-\frac{2d\sqrt{2m_e}}{\hbar}\times\sqrt{\Phi + \frac{eV}{2}}\right]\end{array}\right\}\#(S1)$$

where A is the tunneling area, d is the tunneling distance, m_e is the mass of electron, e is the charge of electron, $\hbar$ is the Planck's constant. The tunneling current is well fitted (blue curve) by Simmons' equation with the fitting parameter $d = 1.5nm$ and $\Phi = 0.49eV$.

At higher bias $(V > \Phi/e)$, the distortion of potential barrier is significant, and it is expressed as Fowler-Nordheim tunneling[2] (F-N tunneling):

$$I \sim V^2 \exp\left(-\frac{4d\sqrt{2m_e\Phi^3}}{3\hbar e}\cdot\frac{1}{V}\right).\#(S2)$$

In the case of F-N tunneling, the plot of $ln(1/V^2)$ versus $1/V$ should be linear with negative slope, and this can be seen in Fig.S1(b) when the voltage greater than 0.5V. Therefore, the distoration of the barrier can be ignored when it is lower than 0.5V. The tunneling current obtained from the bias voltage measurement below 0.5V can be fitted through the Simmons model to obtain the size of the graphene nanogap, which is consistent with the measurement range of ±0.4V of the low bias voltage in Fig. S1(a).

To confirm the presence of the graphene nanogap, we perform AFM measurements as shown in Fig. S1(c), and the gap size in Fig. S1(d) is estimated to be 2.1nm wide, which is closed to our electrical measurements. Therefore, graphene nanogaps with dimensions on the order of 2 nm have been experimentally demonstrated.

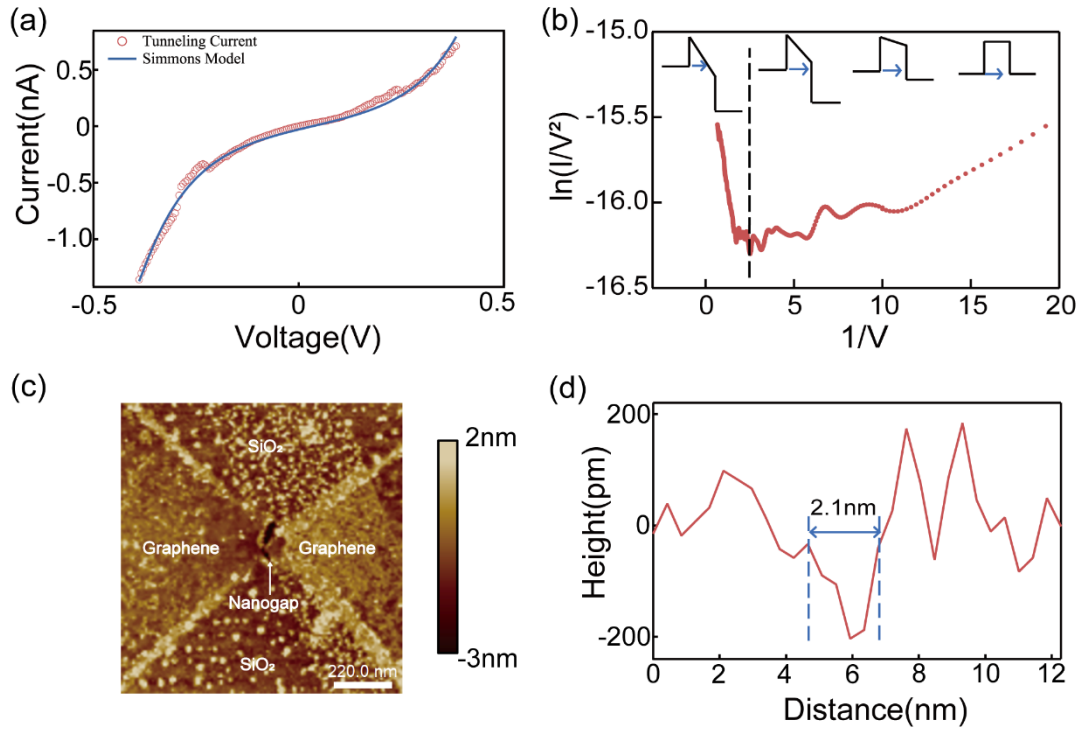

Fig.S1 (a) The measured tunneling current after the electromigration of the graphene nanostripe (red dots) and the fitting line with the Simmons' equation (blue curve). (b) Fowler-Nordheim plot of a tunneling I-V characteristic at voltage from 0V to 1.5V. (c) AFM image of the graphene nanogap. (d) Height across the graphene channel and over the graphene nanogap. The gap size is estimated to be 2.1nm wide.

2.Different conductance evolution of graphene nanogap on SiO_2 and Si_3N_4 substrate

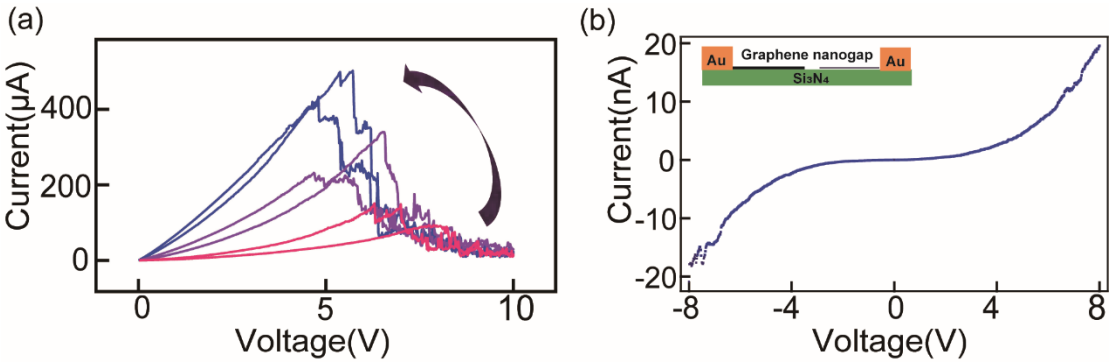

Fig. S2 (a) Stepwise conductance evolution of the device of graphene nanogap on SiO_2 substrate in elctroforming process. (b) Device of graphene nanogap on Si_3N_4 substrate, only shows a tunneling current behavior.

3.Temperature dependent SET voltage Weibull slope $\beta_{V_{SET}}$

From the main text, the evolution of defect switching probability follows the relationship:

$$\lambda \propto \left(\frac{t}{\tau_T}\right)^{\alpha} \#(S2)$$

Where the characteristic time follow the relationship:

$$\tau_T = \tau_{T0}\left(V/t_{gap}\right)^{-m} \#(S3)$$

In the ramping voltage stress $V(t) = Rt$, combine Eq. (S2) and Eq.(S3), we can obtain the defect switching probability as:

$$\lambda \propto \left(t \cdot \tau_{T0}\left(Rt/t_{gap}\right)^{m}\right)^{\alpha} \propto t^{(m+1)\alpha} \#(S4)$$

As shown in Fig. S4, the SET process can't be operated stably at the temperature below 240K, so the defect switching process adheres to the Arrhenius-law as

$$\frac{\partial \lambda}{\partial t} \propto (m+1)\alpha \cdot t^{(m+1)\alpha - 1} \propto \exp\left(-\frac{E_{a1}}{k_B T}\right) \#(S5)$$

Substitute Eq. (1) from the main text to the Eq. (S5), we can obtain the relationship between SET voltage Weibull slope and the environmental temperature as:

$$\frac{\beta_{V_{SET}}}{N} t_{SET}^{\frac{\beta_{V_{SET}}}{N} - 1} \propto exp\left(-\frac{E_{a1}}{k_B T}\right) \#(S6)$$

This is an inverse function of $\beta_{V_{SET}}$ with respect to T. To fit the experimental data with Eq. (S6), we solve the function numerically with bisection method and fit it with our experimental data.

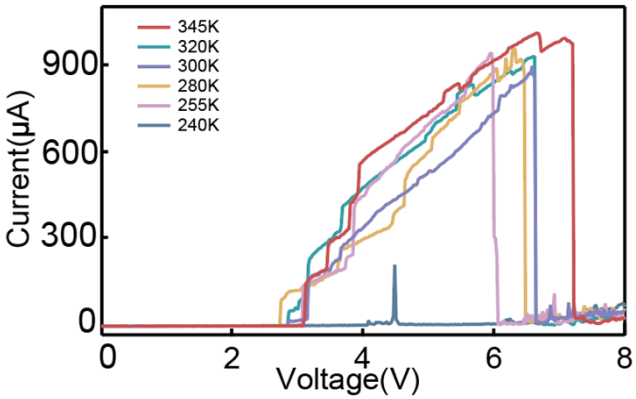

Fig. S3 RS operations at different temperatures, unstable SET operation is observed at the temperature of 240K.

4. RESET process in ambient atmosphere

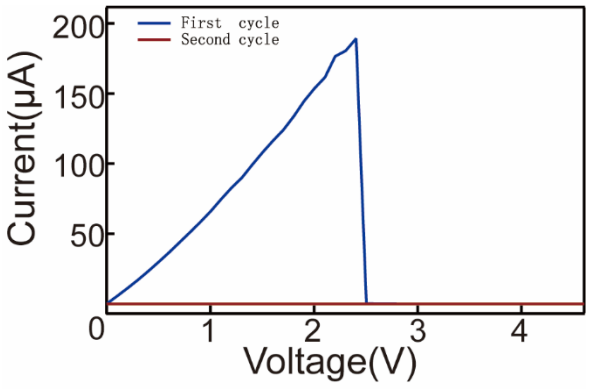

Fig. S4 RESET process in ambient atmosphere only for one cycle, lower RESET voltage compared to the device in vacuum as shown in Fig. 1d, and in the second cycle the device can not operate the SET procedure.

5. Verification of unipolar resistive switching

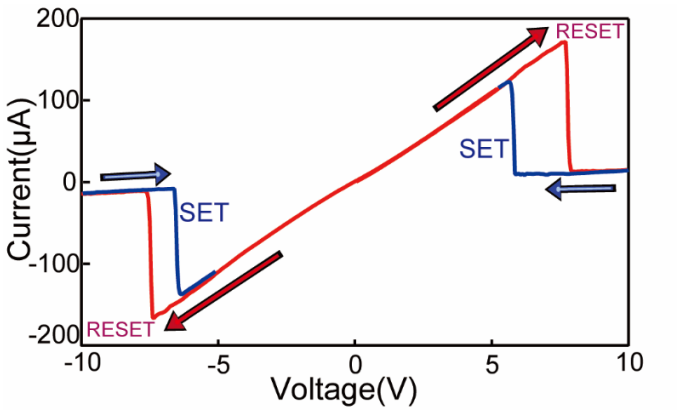

Fig. S5 Unipolar resistive switching behavior of the device operated at positive and negative voltage stress

6. RS at different temperatures

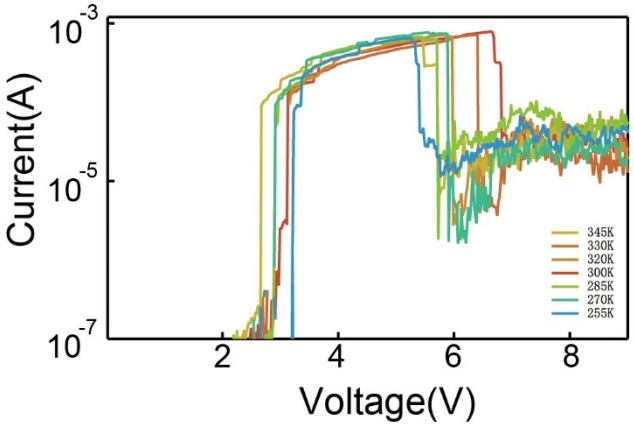

Fig. S6 Resistive switching behavior at different temperatures (from 250K to 350K), no significant conductance increases at LRS.

7. The application potential for neuromorphic computing

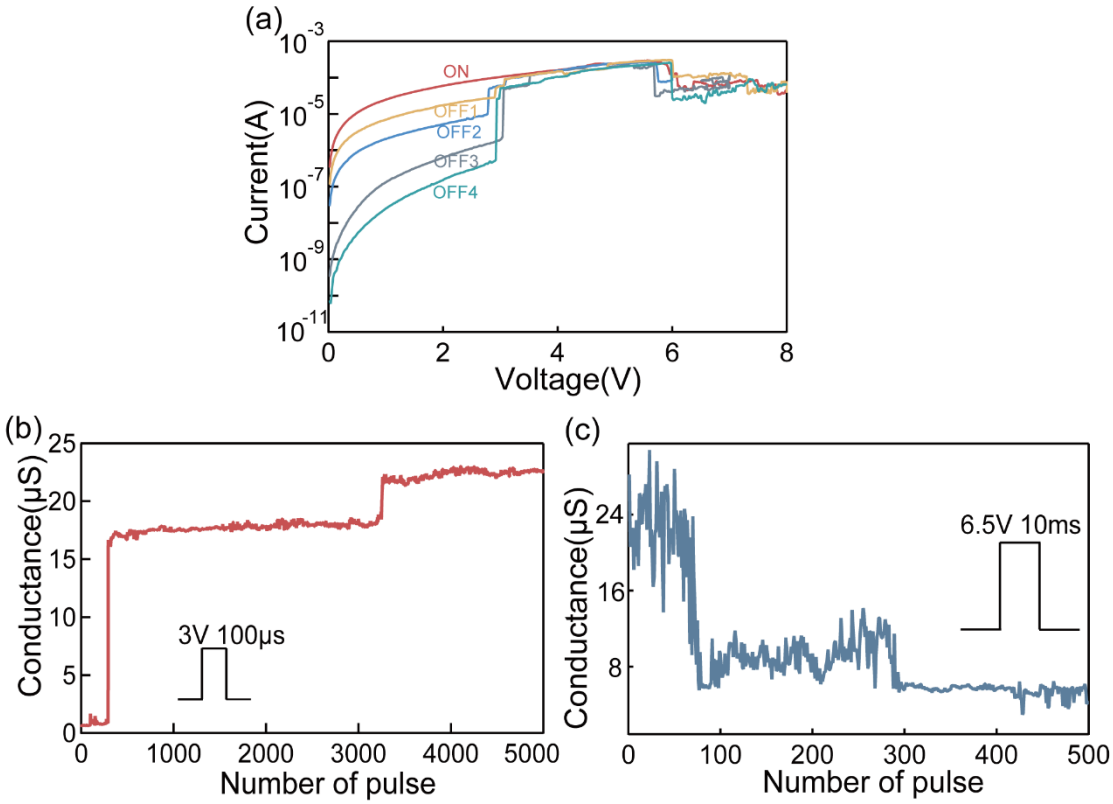

Fig. S7 (a) Multilevel resistive switching characteristics of nanoscale graphene-SiO_2-graphene memristors. (b) Long-term plasticity (LTP) and (c) long-term depression (LTD) of conductance under different number of voltage pulse, showing discrete plasticity.

REFERENCE

1. J. G. Simmons, *Journal of Applied Physics*, 2004, **34**, 1793-1803.
2. J. M. Beebe, B. Kim, J. W. Gadzuk, C. Daniel Frisbie and J. G. Kushmerick, *Physical Review Letters*, 2006, **97**.