Supporting Information for Sub-5-nm one-dimensional post-transition-metal monochalcogenide gate-all-around MOSFETs

Xiao-Lu Duan,[1] Yan-Dong Guo,[1,2,*] Ye-Wei Chen,[1] Yue Jiang,[3,4,†] Hao-Ran Hu,[1] Man-Jun Jiang,[1] Xing-Yu Ma,[1] Jie-Ling Hu,[1] Cheng-Biao Lin,[1] Fan Guo,[5,‡] Hong-Li Zeng,[2,6,7] and Xiao-Hong Yan[6,7]

[1] *College of Electronic and Optical Engineering, Nanjing University of Posts and Telecommunications, Nanjing 210046, China*
[2] *National Laboratory of Solid State Microstructures, Nanjing University, Nanjing 210093, China.*
[3] *Jiangsu Physical Science Research Center, Nanjing 210093, China*
[4] *College of Science, Jinling Institute of Technology, Nanjing 211169, China*
[5] *Suzhou Laboratory, Suzhou 215000, China*
[6] *College of Natural Science, Nanjing University of Posts and Telecommunications, Nanjing 210046, China*
[7] *Key Laboratory of Radio Frequency and Micro-Nano Electronics of Jiangsu Province, Nanjing 210023, China*

Contents

* yandongguo@njupt.edu.cn
† jiangyue@jit.edu.cn
‡ guof@szlab.ac.cn

I The test of doping concentration for the InSe GAA-FETs

To improve the efficiency of carrier injection, we calculated the transport characteristics at different carrier concentrations. Due to the nearly consistent configuration and band size of the optimized nanowire MX (M = In, Ga; X = Se, Te, S) structures, we selected InSe GAA-FETs at $L_g = 5$ nm, $UL = 0$ nm as our test subjects. We examined four different carrier concentrations: 0.005, 0.02, 0.05, and 0.1 e/atom. The corresponding transport characteristic curves for the InSe GAA-FETs are shown in Fig. S1(a) and Fig. S1(b). For n-type, the slopes are relatively consistent at low concentrations, but the slope decreases at 0.1 e/atom. For p-type, the slope does not change significantly with concentration. For both n- and p-type, the on-state current levels are consistent. Combining this with Fig. S1(c), the doping concentration for p-type is determined to be 0.1 e/atom. As shown in Table S1, at a carrier concentration of 0.1 e/atom, the InSe GAA-FETs achieve the highest on-state current and lowest subthreshold swing, leading to the determination of 0.1 e/atom as the optimal p-type doping concentration. In subsequent studies, we will not expand on n-type because its subthreshold swing is significantly greater than that of p-type and far exceeds the Boltzmann limit, which does not meet the requirements for future transistors, while the subthreshold swing of p-type is well below the Boltzmann limit.

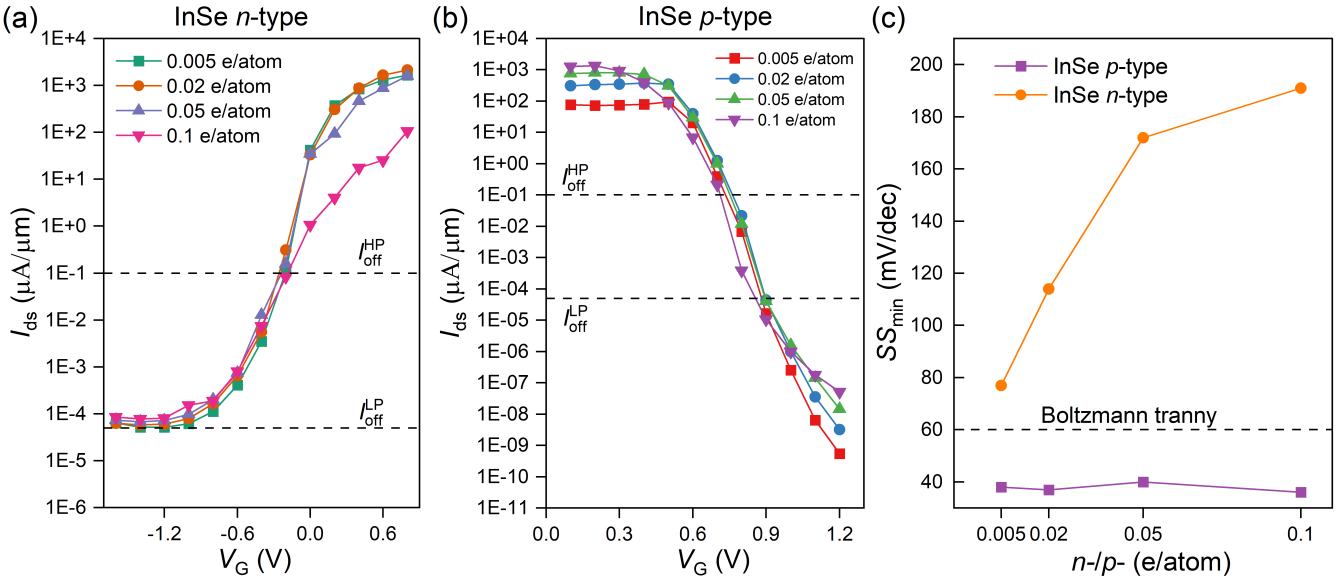

FIG. S1. Transport characteristic curves of InSe GAA-FETs at various doping concentrations for n-type (a) and p-type (b). Minimum subthreshold swing (SS_{min}) of InSe GAA-FETs for both n-type and p-type at different doping concentrations (c).

TABLE S1. Performance of p-type InSe GAA FETs under different doping concentrations. Doping concentration (e/atom). I_{on} (μA/μm): the on-state current. I_{off} (μA/μm): the off-state current. SS (mV/decade): Subthreshold Swing.

doping concerntration	I_{on} (HP)	I_{off} (HP)	I_{on} (LP)	I_{off} (LP)	SS
0.005	74	0.1	73	5E-05	38
0.02	324	0.1	342	5E-05	37
0.05	777	0.1	804	5E-05	40
0.1	1295	0.1	1147	5E-05	36

II The reason for the discontinuities in the I-V characteristics of GaSe and GaS GAA-FETs

The discontinuity in the GaSe and GaS GAA-FETs arises mainly from the abrupt change in the effective Schottky barrier height (Φ_B) at the metal-semiconductor interface, which is modulated by the gate voltage. This change is

further influenced by the gate dependent local density of states (LDOS) near the Fermi level, especially prominent in 1D systems due to quantum confinement. The LDOSs for 1D GaSe and GaS GAAFETs are shown in Fig. S2 and Fig. S3 below, respectively.

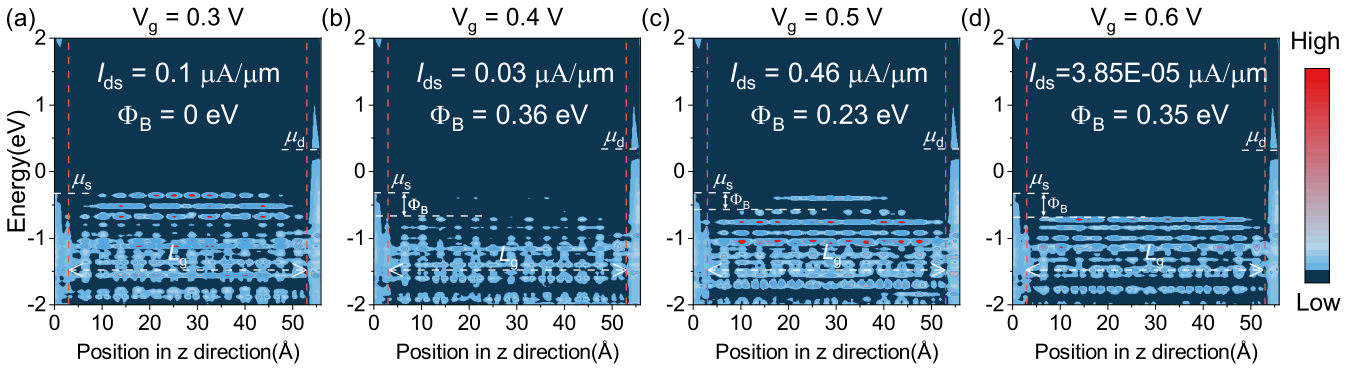

FIG. S2. Local density of states (LDOS) for p-type GaSe GAA-FETs with a gate length of 5 nm at gate voltages of 0.3, 0.4, 0.5, and 0.6 V.

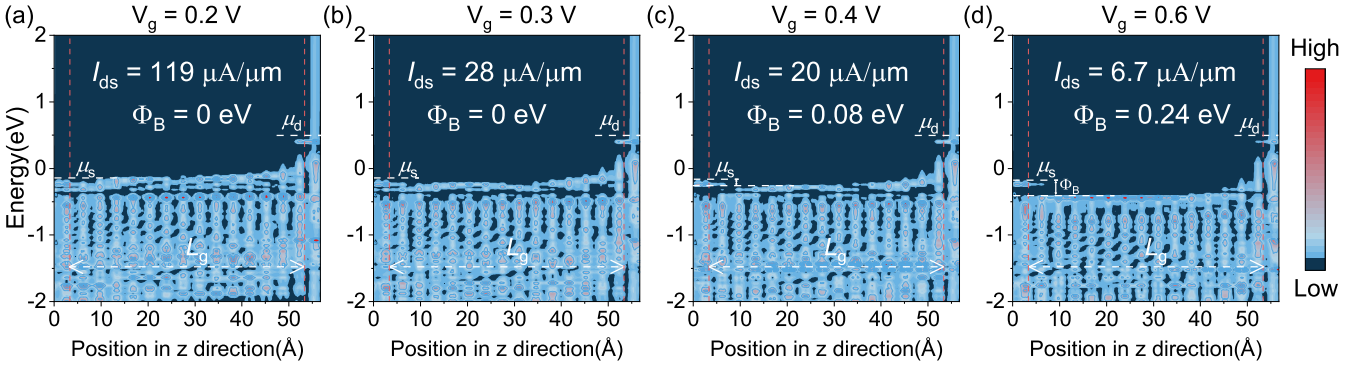

FIG. S3. Local density of states (LDOS) for p-type GaS GAA-FETs with a gate length of 5 nm at gate voltages of 0.3, 0.4, 0.5, and 0.6 V.

III The transport properties of MTe GAA-FETs with different gate lengths

The projected local density of states (PLDOS) and spectral currents of GaTe GAA-FETs for HP at gate lengths of 5 and 3 nm from off-state to on-state are shown in Fig. S4. The parameters of the transport characteristics for different gate lengths are shown in Table S2.

With the reduction in gate length, the barrier rises from 0.27 eV to 0.43 eV in the off-state, and the current is dominated entirely by tunneling current, resulting in a more pronounced short-channel effect. When the gate voltage is reduced by 0.64 V to switch the device to the on-state, the barrier increases by 0.46 eV and 0.43 eV, respectively. Correspondingly, the on-state current decreases from 2470 μA/μm to 1692 μA/μm, the gate control capability is impaired, and the thermoelectric current drops drastically—falling from the order of 10^{-5} to the order of 10^{-9}.

In the transport characterization, we observe that the increase in $SS_{\min}$ from 58 mV/dec to 102 mV/dec, corresponding to the change in gate length from 5 to 3 nm, is due to the stronger short-channel effect. This effect leads to significant tunneling from the source to the drain electrodes, making the tunneling current more challenging to regulate with gate voltage. This conclusion is supported by the PLDOS and spectral currents of GaTe GAA-FETs with gate lengths of 5 and 3 nm in the off-state.

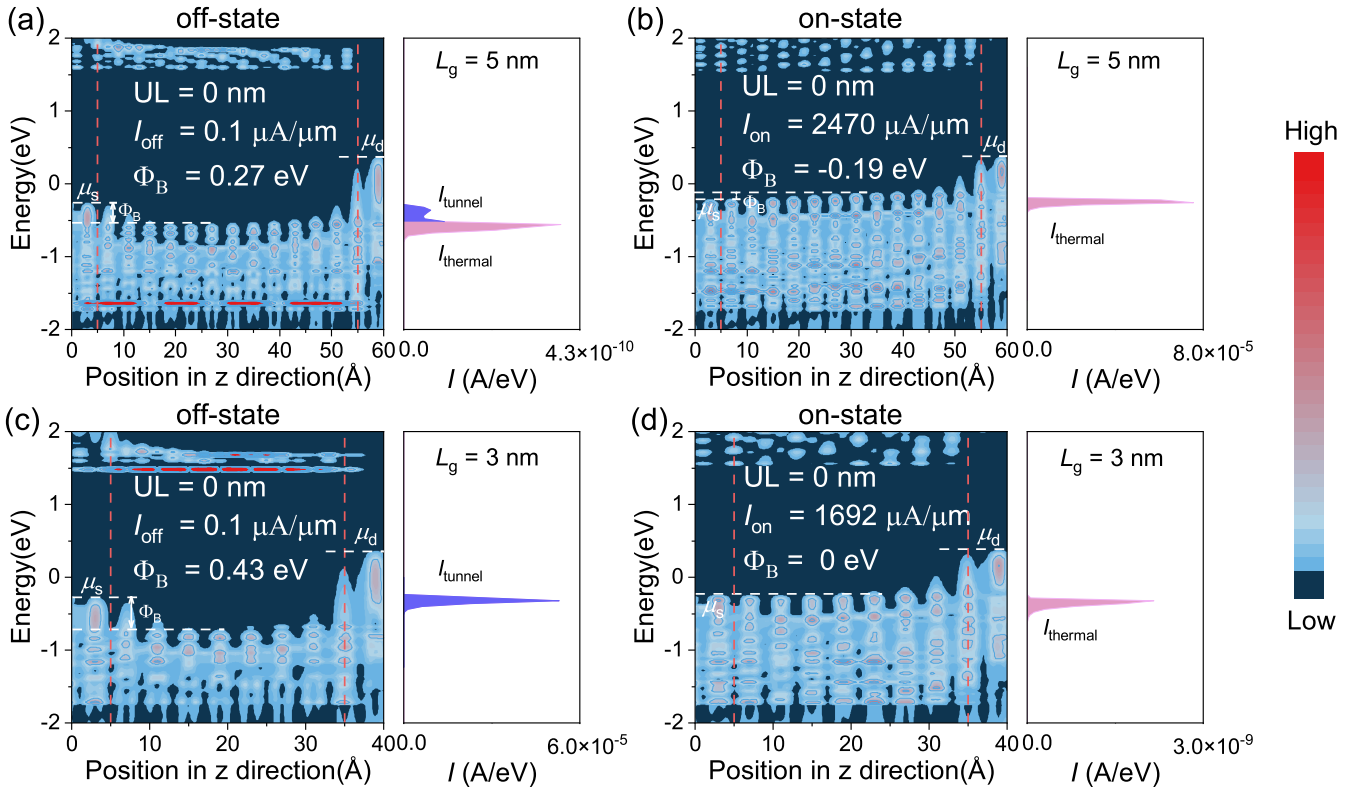

FIG. S4. LDOS and spectral currents of GaTe GAA-FETs with gate lengths of 5 nm (a, b) and 3 nm (c, d) in both off-state and on-state.

TABLE S2. Benchmark of the ballistic performance of the *p*-type MTe (M = Ga, In) GAA-FETs at different gate lengths against the ITRS requirements for HP and LP devices of the next decades.

Material	L_g (nm)	I_{on} (μA/μm)	I_{on}/I_{off}	SS (mV/decade)	C_t (fF/μm)	τ (ps)	PDP (fJ/μm)
InTe (HP)	5	1669	1.67×10^4	46	0.1211	0.0464	0.0496
	4	1650	1.65×10^4	73	0.1149	0.0446	0.0470
	3	1025	1.03×10^4	120	0.0815	0.0509	0.0334
	2	30	3.00×10^3	245	–	–	–
GaTe (HP)	5	2470	2.47×10^4	58	0.1216	0.0315	0.0498
	4	2473	2.47×10^4	82	0.1160	0.0300	0.0475
	3	1692	1.69×10^4	102	0.0951	0.0360	0.0390
	2	52	5.20×10^2	228	–	–	–
ITRS (HP)	5.1	900	–	–	0.60	0.423	0.24
InTe (LP)	5	1229	2.46×10^7	46	0.0866	0.0451	0.0355
	4	182	3.64×10^6	73	–	–	–
GaTe (LP)	5	1125	2.25×10^7	58	0.0930	0.0529	0.0381
	4	0.37	7.40×10^3	82	–	–	–
ITRS (LP)	5.1	298	–	–	0.69	1.493	0.28

IV The impact of underlap on transport properties of MTe GAA-FETs

To investigate how the structural parameters of the gate-channel region underlap influence the transport characteristics of transistors, we systematically calculated the electrical performance of transistors with gate lengths of 5, 4, 3, 2, and 1 nm under conditions of 0, 1, and 2 nm underlap. The transport characteristic curves for InTe and GaTe GAA-FETs with gate lengths of 5 and 2 nm are shown in Fig. S5, with detailed parameter data provided in Table

S3 and Table S4.

For a longer gate length of 5 nm, the *I-V* characteristics of InTe GAA-FETs exhibit slightly lower slopes compared to those of GaTe GAA-FETs. This difference can be attributed to variations in intrinsic carrier mobility and the interface properties of the materials. As the gate length is reduced to 2 nm, the slopes converge and increase significantly due to a pronounced short-channel effect. This effect is particularly evident in the *SS*, at a 5 nm gate length with no underlap, the *SS* value for InTe GAA-FETs deteriorates from 46 mV/dec to 245 mV/dec, while for GaTe GAA-FETs, it rises sharply from 58 mV/dec to 228 mV/dec. The excellent electrostatic control of the GAA structure means that the transport characteristics of the 5 nm gate-length devices are less affected by changes in underlap length. Conversely, the slope of the 2 nm short-gate device significantly decreases as the underlap length increases. These findings indicate that a moderate increase in underlap length can effectively reduce the short-channel effect and enhance the efficiency of gate voltage regulation of carrier transport by broadening the modulation range of the gate electric field in the channel region.

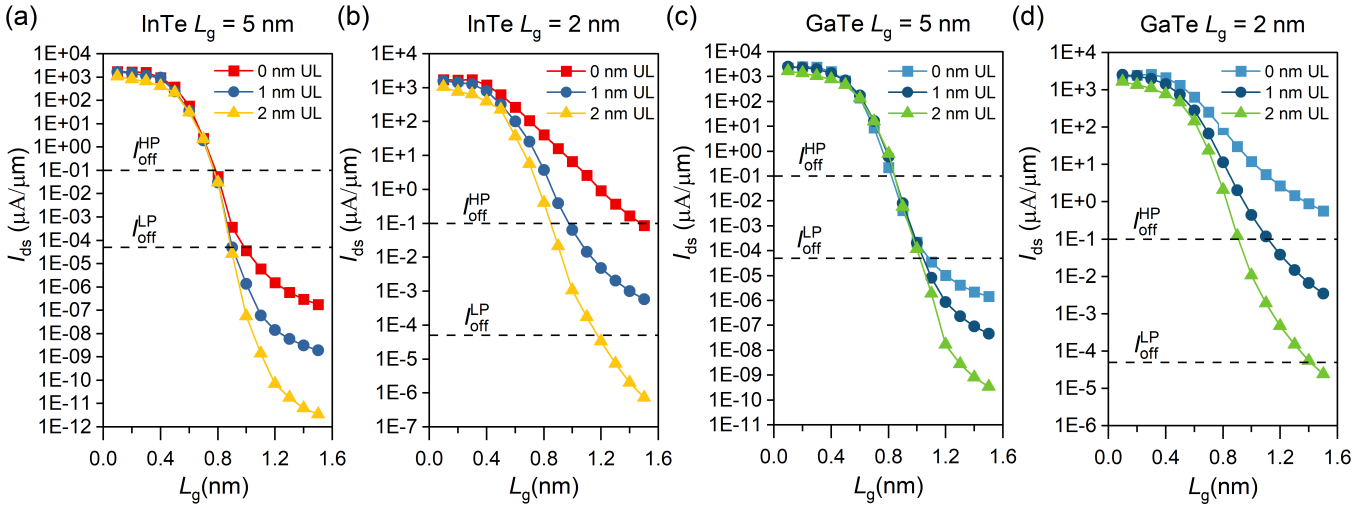

FIG. S5. *I-V* characteristics of InTe GAA-FETs with different underlap lengths for gate length $L_g = 5$ nm (a) and $L_g = 2$ nm (b). *I-V* characteristics of GaTe GAA-FETs with different underlap lengths for $L_g = 5$ nm (c) and $L_g = 2$ nm (d).

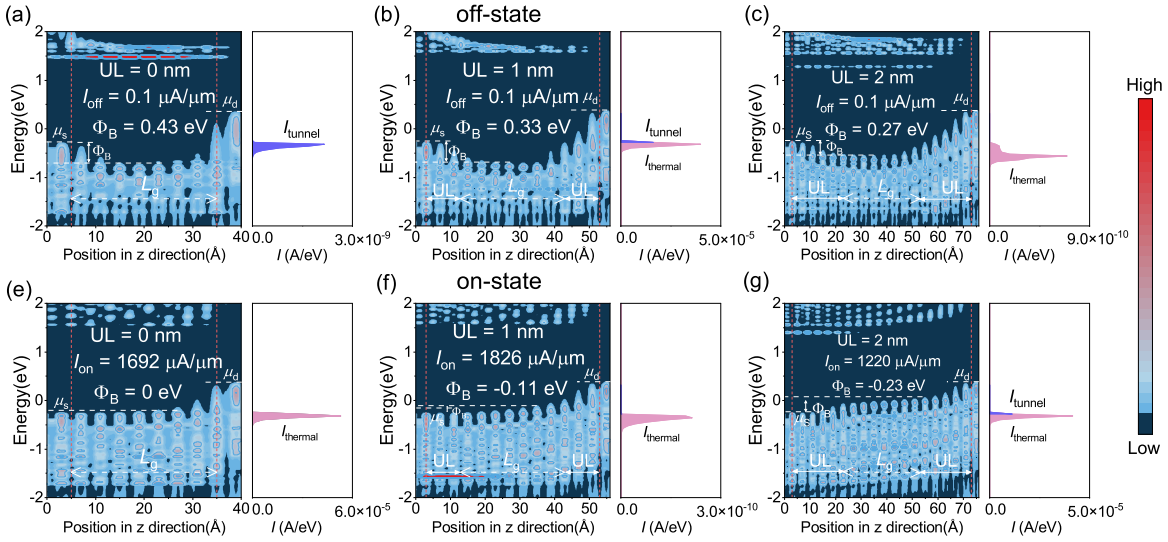

FIG. S6. Local density of states (LDOS) and the spectral current in the channel region for 3 nm L_g p-type GaTe GAA-FETs for HP applications in the off state (a)-(c) and on state (d)-(f) for UL=0, 1 and 2 nm, respectively.

To provide a more fundamental physical understanding of the phenomenon that the on-state current first increases and then decreases as UL increases at a gate length of 3 nm. We have performed additional quantum transport analysis

focusing on the local density of states (LDOS) and spectral current for the key gate length of 3 nm at different UL values (Fig. S6).

The energy offset between the source's Fermi level and the conduction band minimum is denoted by the electron activation energy Φ_B, which represents the energy required for carriers to inject from the electrode into the channel. Without the UL region, the I_{off} is tunneling-dominated (on the order of 10^{-9}), indicating a high yet thin potential barrier that favors electron tunneling but hinders hole injection. After introducing a 1 nm UL region, the off-state potential barrier drops from 0.43 to 0.33 eV, and the current mechanism switches to thermal emission-dominated transport (on the order of 10^{-5}). This shows that the UL region broadens and lowers the potential barrier, enabling the device to conduct current more efficiently via thermal emission in the on-state. Meanwhile, the on-state potential barrier decreases from 0 to -0.11 eV. A negative barrier height means the valence band maximum exceeds the source Fermi level, forming an intra-band channel for holes with ultra-high injection efficiency. As a result, the I_{on} rises from 1692 to 1826 μA/μm. These results confirm that a moderate UL region in short-channel devices can significantly enhance carrier injection efficiency by optimizing the barrier profile and reducing its height, thereby boosting I_{on}.

When the underlap length increases from 1 nm to 2 nm, the on-state potential barrier is further reduced to -0.23 eV (theoretically more favorable for carrier injection), but the I_{on} decreases from 1826 to 1220 μA/μm. The UL region is essentially a low- or lightly-doped area uncovered by the gate electrode. After passing through the channel (strong inversion region) from the source, carriers must traverse the UL region to reach the drain. A longer UL leads to higher resistance in this region. When the UL region is excessively long, the negative impact of the introduced series resistance outweighs the benefits of barrier optimization and injection improvement. The increased resistance restricts current transport, ultimately reducing the total I_{on}.

The behavioral differences depend on the severity of the short-channel effect (SCE). For $L_g = 5$ nm, the relatively long channel leads to weak SCE and an insignificant source-side potential barrier. Introducing UL thus mainly increases series resistance, with negligible injection improvement gains, causing I_{on} to decrease monotonically with UL. For $L_g = 3$ nm, severe SCE induces a high source-side barrier and intense tunneling, which drastically limits on-state performance. Here, the significant gains from barrier optimization using a moderate UL exceed the disadvantages of series resistance, leading to a non-monotonic I_{on} trend of first increasing and then decreasing with UL.

TABLE S3. Benchmark of the ballistic performance of the *p*-type 1D InTe GAA-FETs at different gate lengths and underlap against the ITRS requirements for HP and LP devices of the next decades.

	L_g (nm)	UL (nm)	I_{on} (μA/μm)	I_{on}/I_{off}	SS (mV/decade)	C_t (fF/μm)	τ (ps)	PDP (fJ/μm)
InTe (HP)	5	0	1669	1.67×10^4	46	0.1211	0.0464	0.0496
		1	1570	1.57×10^4	36	0.0380	0.0155	0.0156
		2	918	9.18×10^3	35	0.0207	0.0145	0.0085
	4	0	1650	1.65×10^4	73	0.1149	0.0446	0.0470
		1	1507	1.51×10^4	50	0.0376	0.0160	0.0154
		2	933	9.33×10^3	41	0.0205	0.0141	0.0084
	3	0	1025	1.03×10^4	120	0.0815	0.0509	0.0334
		1	159	1.59×10^3	63	–	–	–
		2	891	8.91×10^3	55	0.0195	0.0140	0.0080
	2	0	30	3.00×10^2	245	–	–	–
		1	1035	1.04×10^4	102	0.0293	0.0181	0.0120
		2	710	7.10×10^3	77	0.0173	0.0156	0.0071
	1	0	0	0	523	–	–	–
		1	152	1.52×10^3	132	–	–	–
		2	592	5.92×10^3	111	–	–	–
ITRS (HP)	5.1	–	900	–	–	0.60	0.423	0.24
InTe (LP)	5	0	1229	2.46×10^7	46	0.0866	0.0451	0.0355
		1	1298	2.60×10^7	36	0.0325	0.0160	0.0133
		2	710	1.42×10^7	35	0.0178	0.0161	0.0073
	4	0	182	3.64×10^6	73	–	–	–
		1	1001	2.00×10^7	50	0.0306	0.0196	0.0125
		2	543	1.09×10^7	41	0.0173	0.0204	0.0071
	3	0	2	3.18×10^4	120	–	–	–
		1	165	3.30×10^6	63	–	–	–
		2	498	9.96×10^6	55	0.0170	0.0218	0.0070
ITRS (LP)	5.1	–	298	–	–	0.69	1.493	0.28

TABLE S4. Benchmark of the ballistic performance of the p-type 1D GaTe GAA-FETs at different gate lengths and underlap against the ITRS requirements for HP and LP devices of the next decades.

	L_g (nm)	UL (nm)	I_{on} (μA/μm)	I_{on}/I_{off}	SS (mV/decade)	C_t (fF/μm)	τ (ps)	PDP (fJ/μm)
GaTe (HP)	5	0	2470	2.47×10^4	58	0.1216	0.0315	0.0498
		1	2147	2.15×10^4	57	0.0424	0.0127	0.0174
		2	1221	1.22×10^4	47	0.0219	0.0115	0.0090
	4	0	2473	2.47×10^4	82	0.1160	0.0300	0.0475
		1	2135	2.14×10^4	61	0.0417	0.0125	0.0171
		2	1245	1.25×10^4	49	0.0218	0.0112	0.0089
	3	0	1692	1.69×10^4	102	0.0951	0.0360	0.0390
		1	1826	1.83×10^4	92	0.0383	0.0134	0.0157
		2	1220	1.22×10^4	66	0.0216	0.0113	0.0089
	2	0	52	5.20×10^2	228	–	–	–
		1	873	8.73×10^3	137	0.1984	0.1454	0.0812
		2	1162	1.16×10^4	87	0.0206	0.0113	0.0084
	1	2	788	7.88×10^3	121	–	–	–
ITRS (HP)	5.1	–	900	–	–	0.60	0.423	0.24
GaTe (LP)	5	0	1125	2.25×10^7	58	0.0930	0.0529	0.0381
		1	1115	2.23×10^7	57	0.0356	0.0204	0.0146
		2	716	1.43×10^7	47	0.0203	0.0181	0.0083
	4	0	0.37	7.40×10^3	82	–	–	–
		1	619	1.24×10^7	61	0.0346	0.0358	0.0142
		2	654	1.31×10^7	49	0.0203	0.0198	0.0083
	3	1	1.00	2.00×10^4	92	–	–	–
		2	352	7.04×10^6	66	0.0296	0.0538	0.0121
	2	0	52	1.04×10^6	228	–	–	–
ITRS (LP)	5.1	–	298	–	–	0.69	1.493	0.28

V Device Performance under the IRDS (2024) and ITRS (2013) Standards

Two performance benchmark against the most recent IRDS 2024 edition and ITRS 2013 edition for our key p-type InTe and GaTe GAA FETs at the 5-nm node with various UL lengths are as follows.

TABLE S5. Benchmark of the ballistic performance of the p-type 1D GaTe and InTe GAA FETs at different gate lengths and underlap against the ITRS (2013) and IRDS (2024) requirements for HP devices of the next decades.

	L_g (nm)	UL (nm)	I_{on} (μA/μm)	I_{off} (μA/μm)	I_{on}/I_{off}	SS (mV/decade)	C_t (fF/μm)	τ (ps)	PDP (fJ/μm)
GaTe	5	0	2470	0.1	2.47E+04	58	0.1216	0.0315	0.0498
		1	2147	0.1	2.15E+04	57	0.0424	0.0127	0.0174
		2	1221	0.1	1.22E+04	47	0.0219	0.0115	0.0090
InTe	5	0	1669	0.1	1.67E+04	46	0.1211	0.0464	0.0496
		1	1570	0.1	1.57E+04	36	0.0380	0.0155	0.0156
		2	918	0.1	9.18E+03	35	0.0207	0.0145	0.0085
ITRS		–	900	0.1	9.00E+03	60	0.60	0.423	0.24
GaTe	5	0	2457	0.01	2.46E+05	58	0.1140	0.0297	0.0467
		1	2099	0.01	2.10E+05	57	0.0411	0.0125	0.0168
		2	1188	0.01	1.19E+05	47	0.0217	0.0117	0.0089
InTe	5	0	1630	0.01	1.63E+05	46	0.1019	0.0400	0.0418
		1	1402	0.01	1.40E+05	36	0.0334	0.0153	0.0137
		2	768	0.01	7.68E+04	35	0.0182	0.0152	0.0075
IRDS		–	827	0.01	8.27E+04	70	0.31	0.64	0.33

TABLE S6. Benchmark of the ballistic performance of the p-type 1D GaTe and InTe GAA FETs at different gate lengths and underlap against the ITRS (2013) and IRDS (2024) requirements for LP devices of the next decades.

	L_g (nm)	UL (nm)	I_{on} (μA/μm)	I_{off} (μA/μm)	I_{on}/I_{off}	SS (mV/decade)	C_t (fF/μm)	τ (ps)	PDP (fJ/μm)
	5	0	1125	5E-05	2.25E+07	58	0.0930	0.0529	0.0381
GaTe		1	1115	5E-05	2.23E+07	57	0.0356	0.0204	0.0146
		2	716	5E-05	1.43E+07	47	0.0203	0.0181	0.0083
	5	0	1229	5E-05	2.46E+07	46	0.0866	0.0451	0.0355
InTe		1	1298	5E-05	2.60E+07	36	0.0325	0.0160	0.0133
		2	710	5E-05	1.42E+07	35	0.0178	0.0161	0.0073
ITRS		–	298	5E-05	1.80E+07	60	0.69	1.493	0.28
	5	0	1373	1E-04	1.37E+07	58	0.0945	0.0441	0.0387
GaTe		1	1296	1E-04	1.30E+07	57	0.0361	0.0178	0.0148
		2	851	1E-04	8.51E+06	47	0.0205	0.0155	0.0084
	5	0	1330	1E-04	1.33E+07	46	0.0886	0.0426	0.0363
InTe		1	1298	1E-04	1.30E+07	36	0.0325	0.0160	0.0133
		2	710	1E-04	7.10E+06	35	0.0178	0.0161	0.0073
IRDS		–	614	1E-04	6.14E+06	70	0.31	0.86	0.33