Supplementary Information

Artificial synaptic behaviors of mobile silver-doped vanadium-cerium oxide memristor with embedded silver nanoclusters for neuromorphic computing applications

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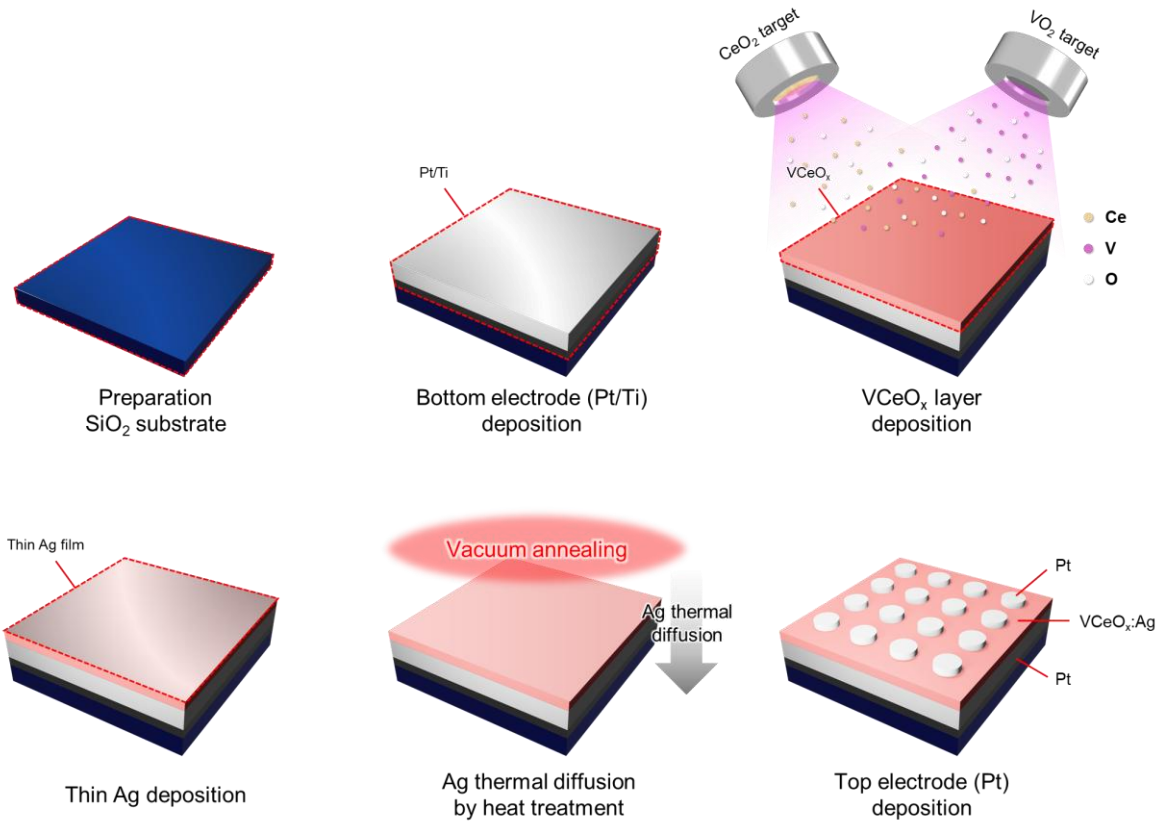


Figure S1 | Fabrication scheme for the Pt/VCeO$_x$:Ag/Pt memristor.

The Pt/VCeO$_x$:Ag/Pt memristor was fabricated as following the series of processing that includes the deposition of a Ti/Pt bottom electrode on a SiO_2/Si substrate by e-beam evaporation, a ~45 nm-thick VCeO$_x$ layer by co-sputtering using VO_2 and CeO_2 targets in an RF sputtering system, and a 3 nm-thick Ag layer on top of VCeO$_x$ by e-beam evaporation, followed by vacuum annealing at 200 °C to induce the diffusion of Ag into VCeO$_x$ layer, and formation of a 100 μm dot-patterned Pt top electrode by e-beam evaporation using a shadow mask.

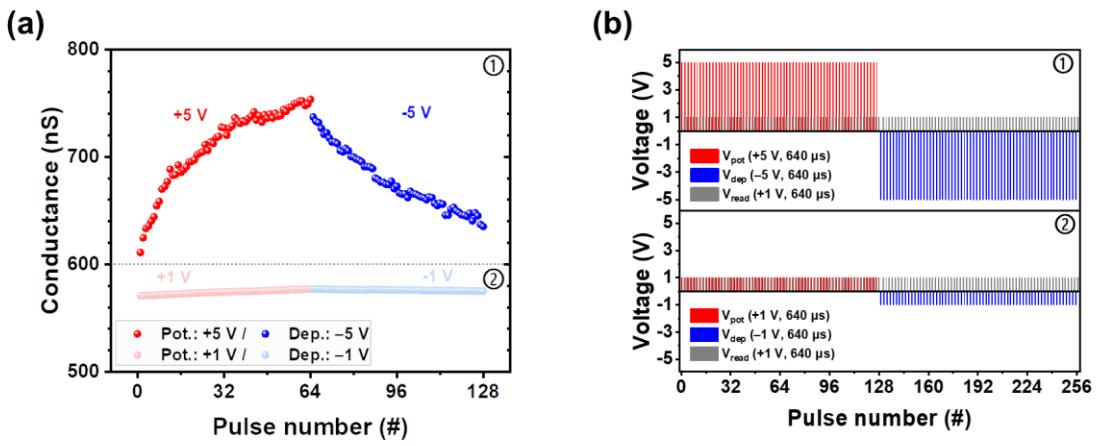


Figure S2 | Read disturbance evaluation. (a) Conductance modulation curves measured under two different pulse schemes: Scheme 1 (+5 V for potentiation / –5 V for depression, each followed by a +1 V read pulse) and Scheme 2 (+1 V for potentiation / –1 V for depression, each followed by a +1 V read pulse), (b) Schematic representation of the pulse sequences for each condition.

To examine read disturbance whether the read operation at +1 V influences the conductance modulation characteristics, the conductance change for weight update was compared under two different pulse schemes: Scheme 1 (+5 V for potentiation / –5 V for depression, each followed by a +1 V read pulse) and Scheme 2 (+1 V for potentiation / –1 V for depression, each followed by a +1 V read pulse). It reveals that the conductance change was negligible at Scheme 2 by applying +1 V for potentiation and –1 V for depression, indicating that the read operation by applying at +1 V read pulse in the standard scheme does not disturb the weight update behavior.

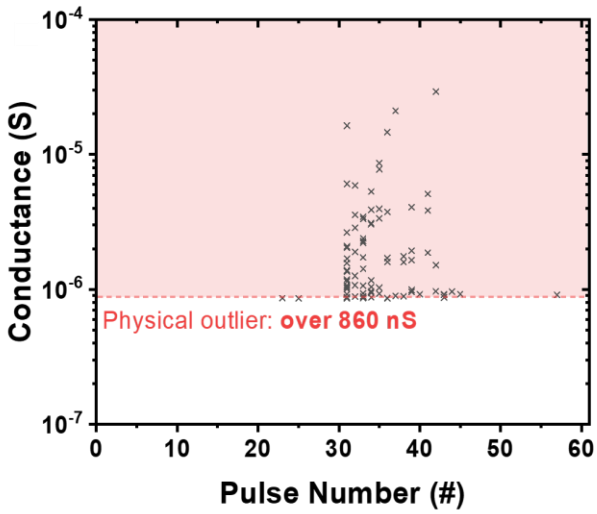


Figure S3 | Conductance outliers excluded from cycle-to-cycle variability analysis.

Conductance values exceeding 860 nS observed during potentiation and depression cycling are classified as physical outliers and excluded from the cycle-to-cycle variability analysis in **Figure 2c**. These sporadic high-conductance events are likely attributed to transient distribution of Ag atoms or stochastic charge transport dynamics, and do not represent the typical analog conductance change behavior of the device.

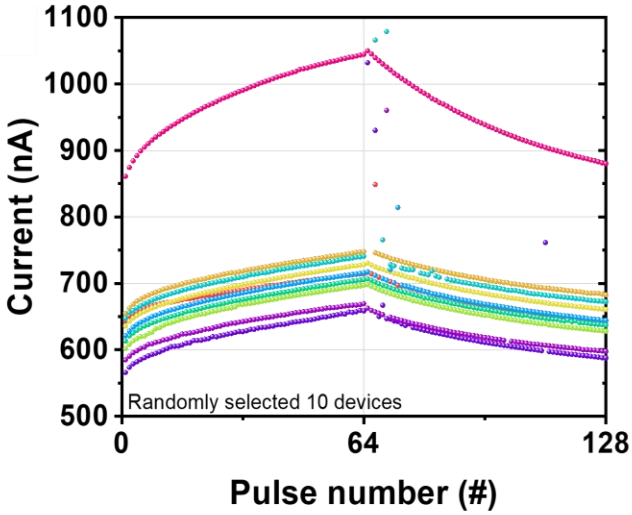


Figure S4 | Conductance modulation curves for device-to-device variability evaluation.

Figure S4 displays the conductance modulation curves for 10 randomly selected devices, obtained under the same stimulation protocol used in the main text: potentiation pulses of +5 V for 640 μs, depression pulses of −5 V for 640 μs, and intermediate read pulses of +1 V for 640 μs. While one device shows a relatively higher current level compared to the others, the overall trend of gradual and symmetric conductance change is well preserved across all devices.

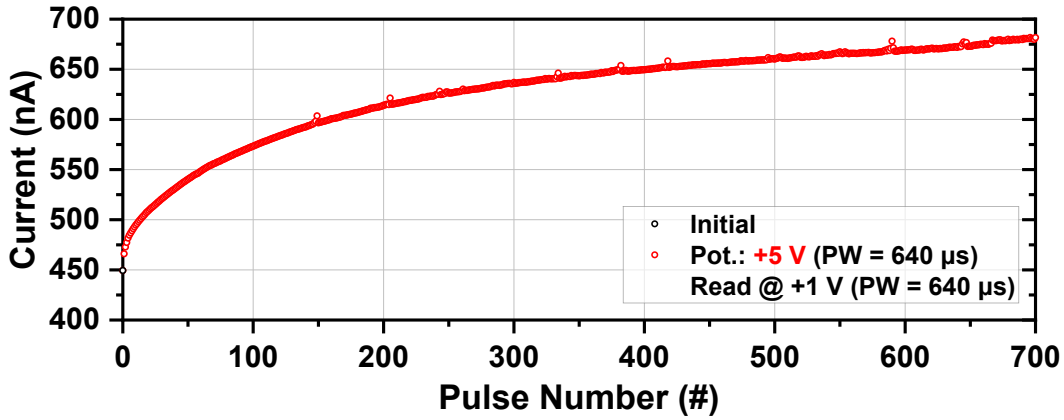


Figure S5 | Conductance modulation beyond 9-bit resolution.

Figure S5 demonstrates the highly resolved multilevel conductance modulation with over 700 distinguishable states of Pt/VCeO$_x$:Ag/Pt memristor, corresponding to a resolution beyond 9 bits. This result was obtained by applying consecutive potentiation pulses under the same voltage and duration conditions described in the main text (+5 V, 640 µs). The fine and monotonic current increments confirm the feasibility of extended analog conductance change, which is essential for high-precision synaptic weight updates in neuromorphic computing. Notably, despite the high pulse amplitude and prolonged electrical stress, the device exhibits a gradual increase in conductance without any abrupt current jumps or permanent breakdown, further confirming that the switching is governed by a non-filamentary mechanism even under these rigorous conditions. Such high-resolution update capability is particularly beneficial for tasks that require dense and accurate weight representation in spiking neural networks (SNNs).

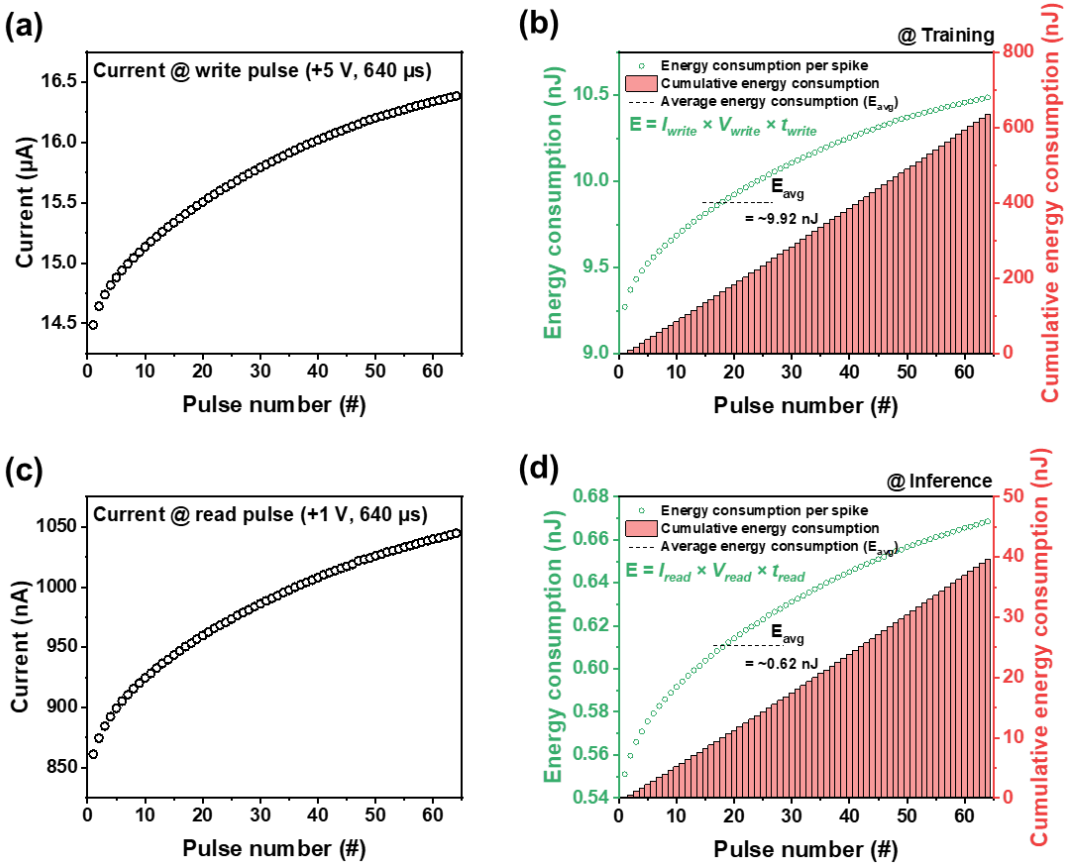
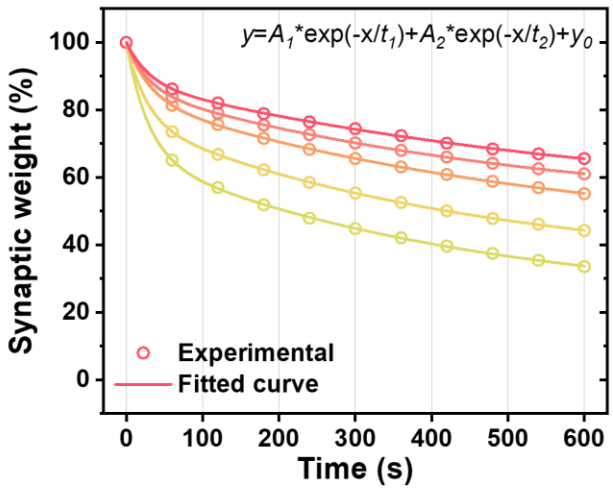


Figure S6 | Device energy consumption calculation.

The energy consumption for training and inference operations of Pt/VCeO$_x$:Ag/Pt memristor synapse was calculated. Due to the dynamic nature of conductance modulation and its nonlinearity, the current response and consequent instantaneous power vary at each successive potentiation or depression pulse. To account for this variability, the energy consumed during each individual pulse was computed and then numerically integrated over the full pulse sequence. The total integrated energy (E_{total}) was subsequently divided by the total number of pulses (P_{max}) to yield an average energy consumption per synaptic event (E_{avg}) as illustrated in the following equation,

$$E_{avg} = \frac{E_{total}}{P_{max}} = V \cdot t \cdot \frac{1}{P_{max}} \sum_{i=1}^{P_{max}} I_i$$

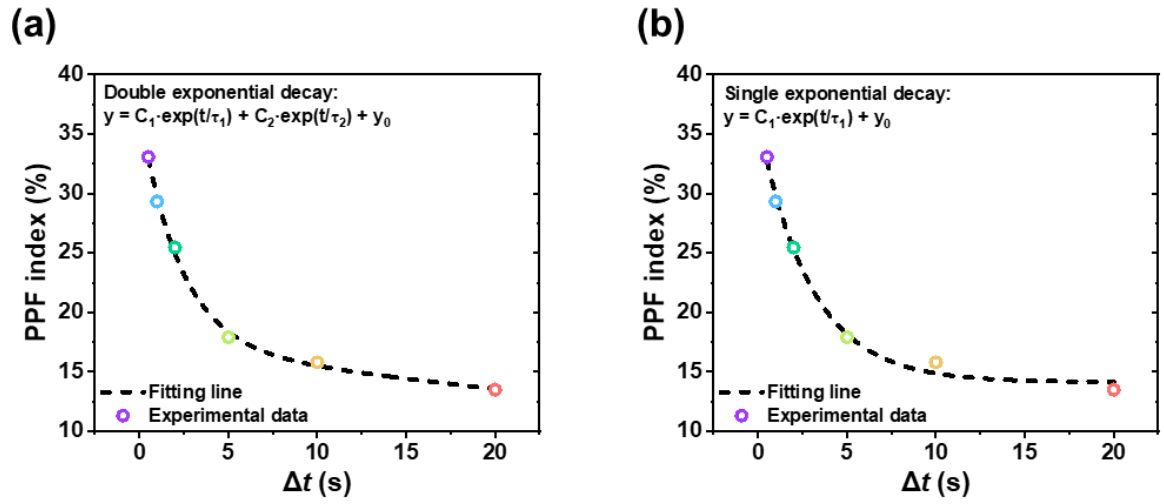
where V, t, and I_i are the pulse amplitude, pulse width, and the current response, respectively. Using this method, an average energy consumption was calculated to be approximately 9.92 nJ/event during training (write operation with gradual conductance modulation), and 0.62 nJ/event during inference (read operation under low-voltage bias) in the given range of current.



Pulse #	A_1 (A_{STM})	τ_1 (τ_{STM}) [s]	A_2 (A_{LTM})	τ_2 (τ_{LTM}) [s]	y_0 [%]	R^2
100	33.18	28.31	44.64	444.03	22.18	0.99993
200	23.13	25.74	44.11	448.42	32.76	0.99998
300	16.53	30.42	42.42	549.07	41.05	0.99995
400	13.83	28.09	37.36	539.50	48.81	0.99997
500	11.99	29.11	37.82	664.83	50.18	0.99985

Figure S7 | Double exponential decay function fitting of normalized retention curves for STP-to-LTP analysis.

Normalized retention curves (0–100%) for different potentiation pulse counts (100, 200, 300, 400, and 500 pulses) obtained from **Figure 4e** were fitted with a double exponential decay function with the form $y = A_1 \cdot \exp(-t/\tau_1) + A_2 \cdot \exp(-t/\tau_2) + y_0$, where A_1 and τ_1 correspond to the short-term memory (STM) component, and A_2 and τ_2 to the long-term memory (LTM) component. The fitted curves (solid lines) and original data (symbols) are shown for each case. Extracted parameters—A_1, A_2, τ_1, τ_2, and residual offset y_0—are listed for each pulse condition, illustrating the progressive enhancement of LTM retention with increased stimulation.



	Double exponential decay	Single exponential decay
C_1	20.01965 ± 1.85221	22.01843 ± 1.022
τ_1	2.28549 ± 0.56939	2.95252 ± 0.38379
C_2	5.64352×10^5 ± --	–
τ_2	3.318900×10^6 ± --	–
y_0	-5.64335×10^5 ± --	14.12859 ± 0.62704

Figure S8 | Comparison of double vs. single exponential decay function fitting of PPF index. PPF index fitting by (a) double exponential decay function and (b) single exponential decay function.

Although the experimental data could be fitted with double exponential decay function, the extracted fitting parameters were not physically meaningful. For example, the slow decay time constant (τ_2) exceeded several million seconds, and the amplitude and offset terms (C_2, y_0) nearly canceled each other, indicating model overparameterization. In contrast, the single exponential decay model provided both a good visual fit and interpretable parameter values, indicating that fitting with a single exponential decay function provides a more appropriate and interpretable description of the experimental results.

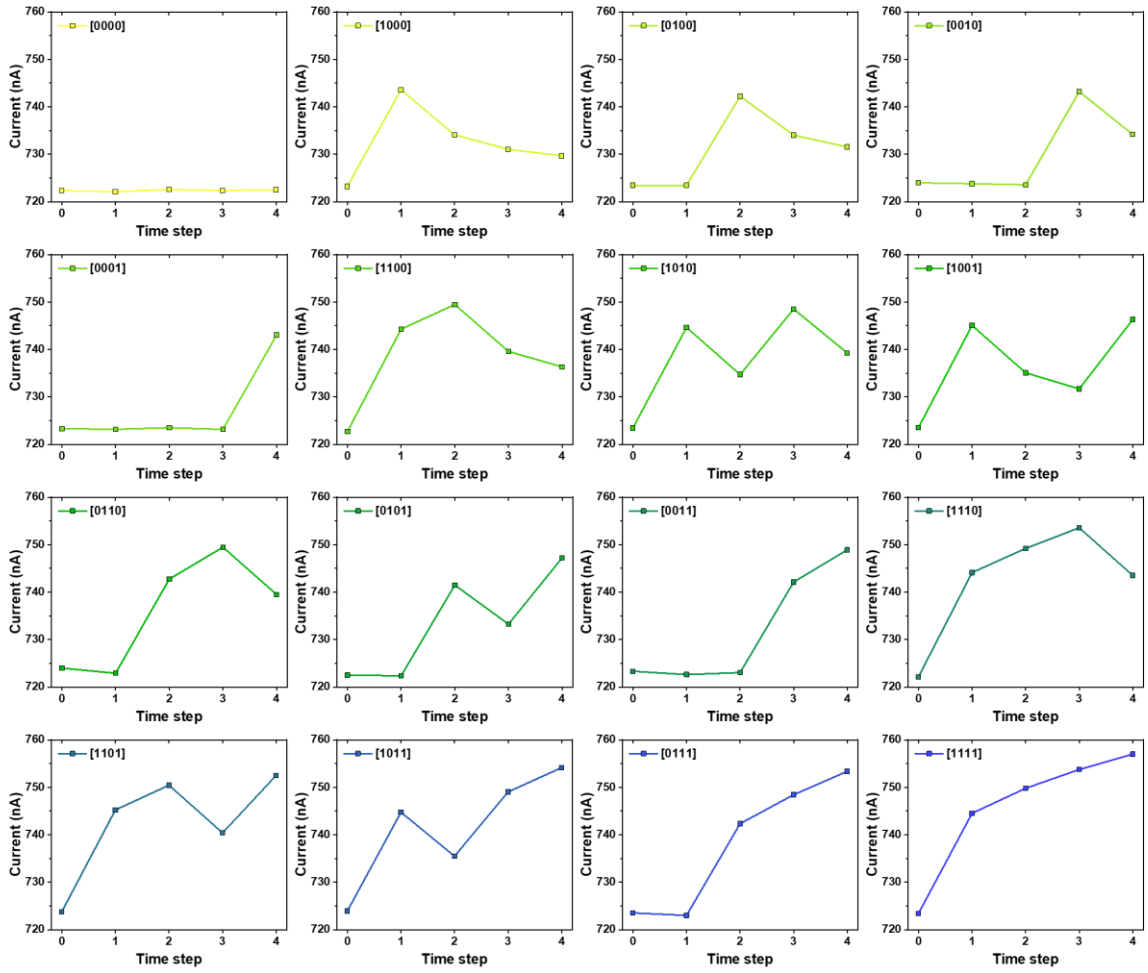


Figure S9 | Individual current response curves of the Pt/VCeO$_x$:Ag/Pt memristor under each 4-bit pulse stream from [0000] to [1111].

To validate the reproducibility and temporal separability of each reservoir state, individual current profiles were measured for all 16 distinct 4-bit pulse streams (from [0000] to [1111]), each comprising 4-time steps. The resulting temporal current trajectories demonstrate consistently increasing and decaying trends across different streams, indicating high reproducibility and temporal resolution. This behavior supports the device's suitability for multi-level encoding in physical reservoir computing.

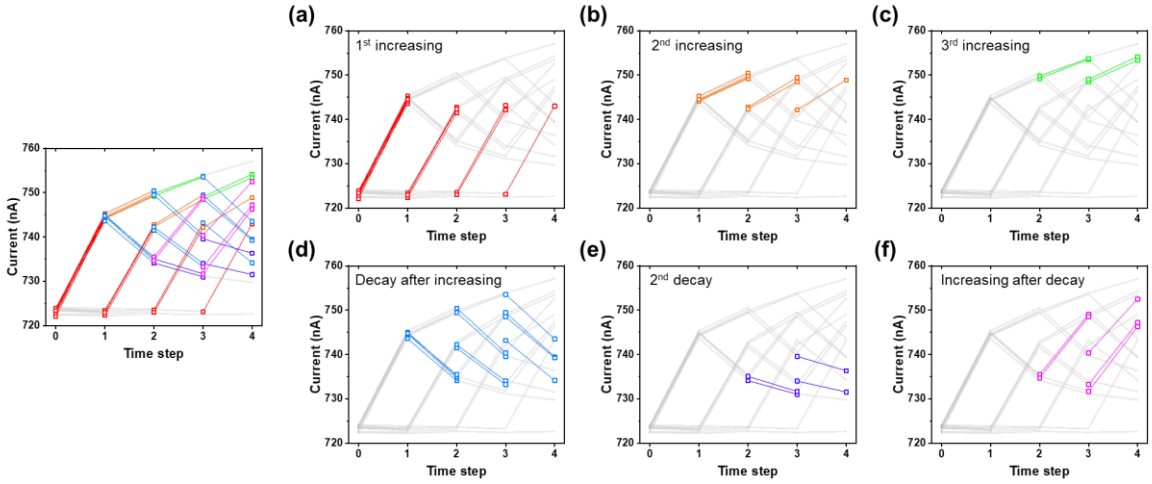


Figure S10 | Consistency of dynamic conductance changes across 4-bit input streams in reservoir state evolution.

To investigate the temporal consistency of conductance modulation within the memristor-based reservoir computing system, current responses were categorized and analyzed according to their increasing and decaying components across different 4-bit input sequences. Despite variations in bit pattern and activation order, distinct slope clusters are disclosed, implying consistent dynamic behavior across structurally similar pulse streams. The data are grouped according to shared temporal features for detailed comparison:

(a) 1st conductance increasing components.
(b) 2nd conductance increasing components.
(c) 3rd conductance increasing components.
(d) 1st decay components after conductance increasing.
(e) 2nd decay components.
(f) Increasing components after decay.

This grouped visualization of slope for increasing and decaying components emphasizes that the memristor maintains predictable and temporal coherence across structurally analogous input patterns, which is a key advantage for ensuring input discriminability and temporal consistency in physical reservoir computing systems. This consistent and predictable response supports robust temporal encoding and improves separability of reservoir states, facilitating reliable classification in neuromorphic tasks.

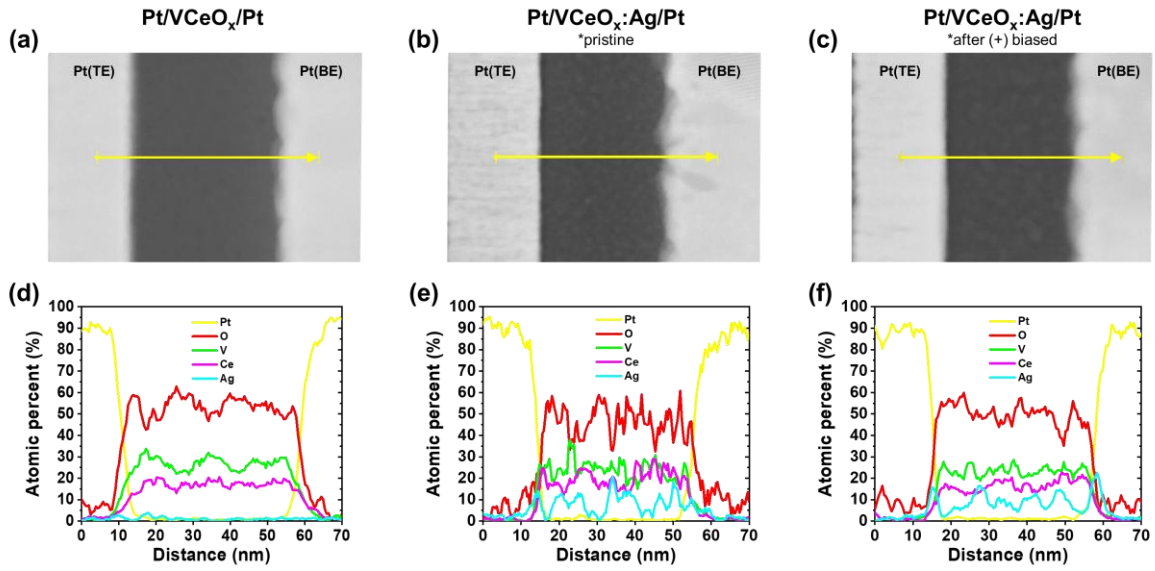


Figure S11 | Compositional analysis of Pt/VCeO$_x$/Pt and Pt/VCeO$_x$:Ag/Pt memristors. (a–c) Cross-sectional scanning transmission electron microscopy (STEM) images of (a) undoped (Pt/VCeO$_x$/Pt) device, (b) Ag-doped device (Pt/VCeO$_x$:Ag/Pt) in its pristine state, and (c) Ag-doped device after application of +5 V × 100 pulses, with yellow arrows indicating the locations of energy-dispersive spectroscopy (EDS) line scans. (d–f) Corresponding EDS line scan profiles along the indicated regions, highlighting compositional differences across the VCeO$_x$ layer. Quantitative analysis of the EDS line profiles indicates a uniform V/Ce atomic ratio of approximately 1.5:1 throughout the switching layer.

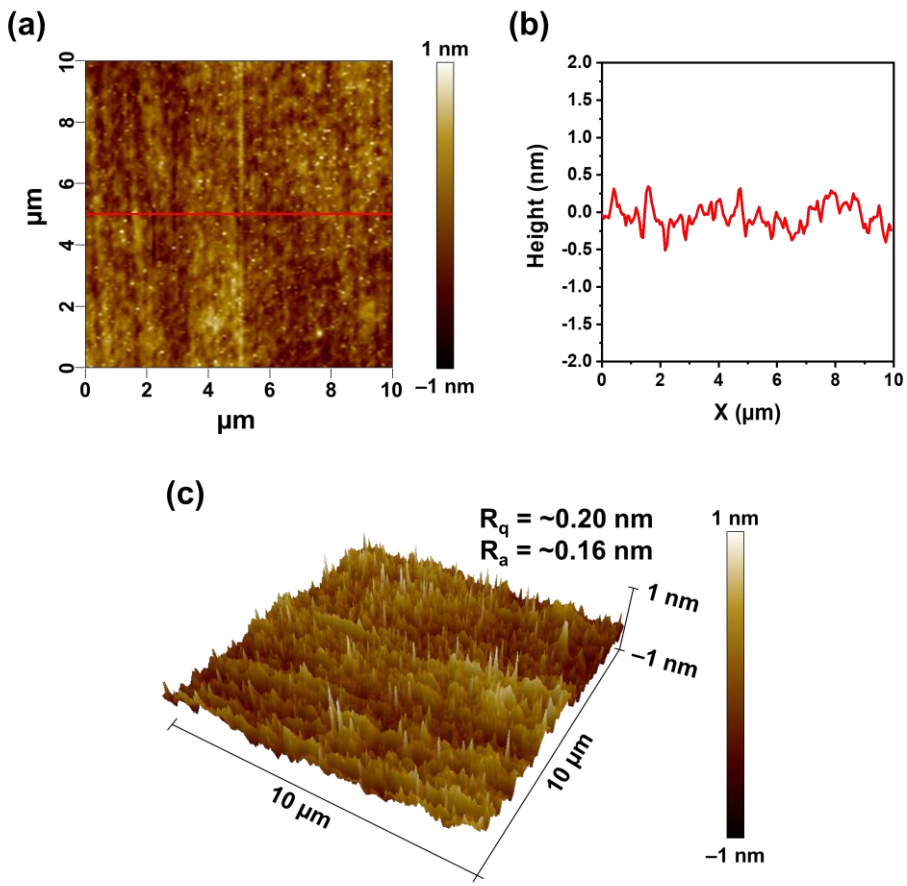


Figure S12 | Surface morphology analysis of $VCeO_x$:Ag layer by atomic force microscopy (AFM). (a) AFM topography image acquired over a 10 µm × 10 µm area, showing a uniformly smooth surface without any significant surface features. (b) Line profile extracted along the red line in (a), providing a quantitative assessment of surface height variation. (c) 3D surface morphology map reconstructed from topography data.

The root-mean-square roughness (R_q) and average roughness (R_a) were measured to be approximately 0.2 nm and 0.16 nm, respectively, indicating an atomically flat surface. Such flatness is attributed to the amorphous nature of the $VCeO_x$:Ag layer, which is desirable to achieve a structurally stable and reproducible interface with the top Pt electrode.

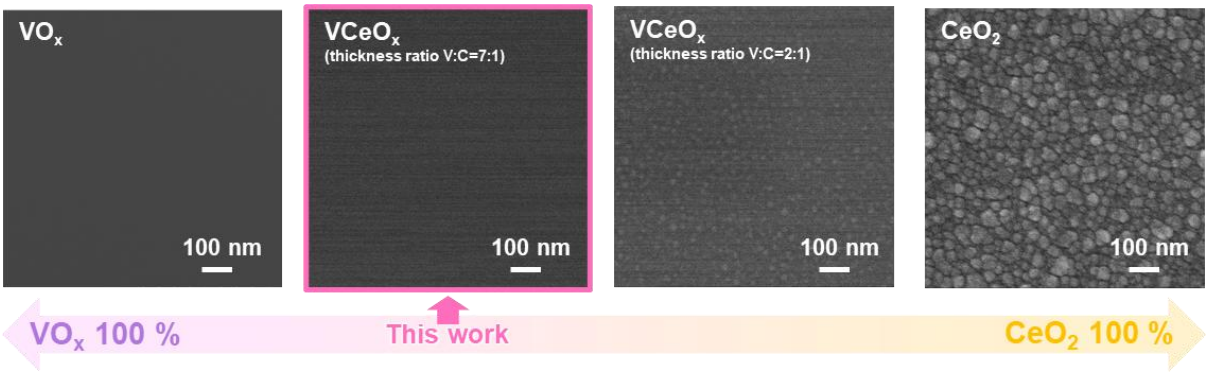


Figure S13 | Scanning electron microscopy (SEM) images of VO_x, $VCeO_x$, and CeO_2 layers with V/Ce composition variations.

Figure S13 shows the SEM images of oxide layers with different V/Ce compositions. The VO_x layer exhibits a featureless and smooth surface consistent with an amorphous structure. As the Ce content increases, small grain-like features begin to emerge, then nanocrystalline grains (~20–30 nm in size) with clear grain boundaries are observed in the CeO_2 layer, indicating a fully polycrystalline structure. These results confirm that increasing Ce content enhances crystallinity and surface roughening. This mixed-oxide approach with optimizing the composition effectively preserves the structural advantage of VO_x, namely its smooth and amorphous surface that supports uniform ion migration, as well as incorporating the electronic benefits of CeO_2 such as its wide bandgap, which helps suppress excessive leakage current.

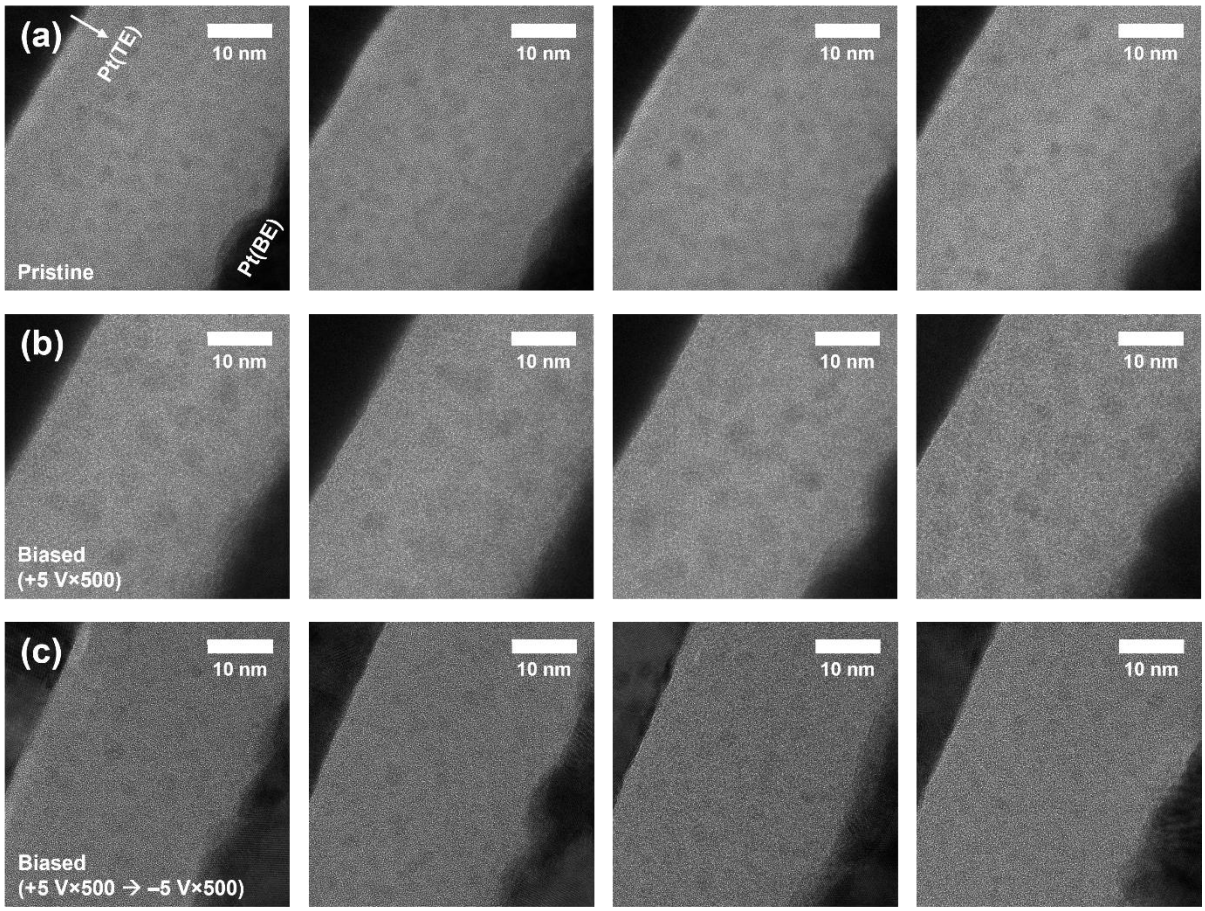


Figure S14 | Bias-dependent TEM analysis of Pt/VCeO$_x$:Ag/Pt memristors. (a) pristine state, (b) after 500 potentiation pulses (+5 V, 640 μs), and (c) after sequential application of 500 potentiation pulses followed by 500 depression pulses (–5 V, 640 μs).

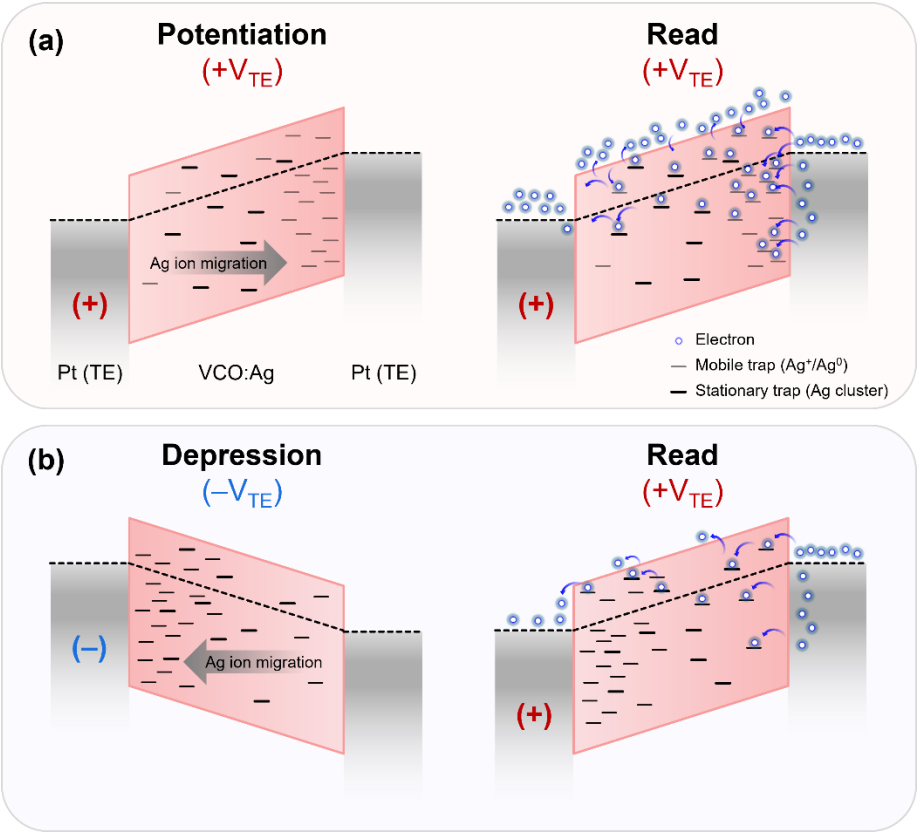


Figure S15 | Schematic illustration of the conduction in potentiation and depression via distributed Ag ions and nanoclusters.

Figure S15 illustrates the different resistances between potentiation and depression with respect to the distribution of Ag ions and nanoclusters, where the device resistance is primarily determined by the interfacial state near the bottom electrode under a fixed read bias (+V at top electrode). When it comes to potentiation, Ag ions accumulate at the bottom interface, drastically enhancing electron injection and transport in synergy with Ag clusters. Although the top interface is ion-depleted, the large amounts of injected electrons can be transported by hopping through stationary nanoclusters or being excited to the conduction band. On the other hand, in the case of depression, Ag ions are depleted from the bottom interface, which significantly reduces the amounts of injected electrons at the same read bias. This limited injection at the bottom interface leads to the decreased resistance state. Consequently, the device achieves asymmetric, polarity-dependent switching because the injection efficiency at the bottom interface outweighs the resistance changes in other regions.

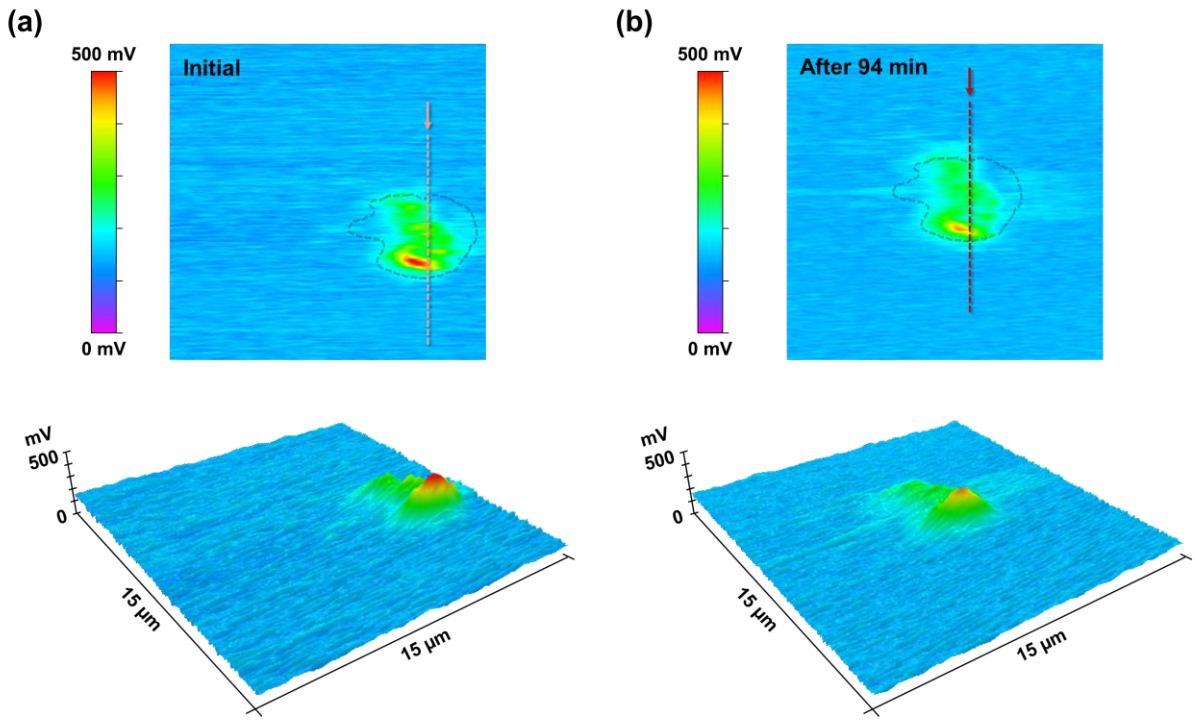


Figure S16 | Original 2D & 3D data of time-dependent Kelvin probe force microscopy (KPFM) results. 2D and 3D surface potential maps of the Ag-doped $VCeO_x$ layer (a) immediately after applying a bias of +5 V × 100 pulses (0 min, initial state) and (b) corresponding maps acquired 94 min after bias application. The overall surface potential decreases with time and exhibits a slight lateral broadening, indicating a gradual relaxation and spatial redistribution of the bias-induced surface potential contrast.

Supplementary Note 1 | Normalization and standardization of nonlinearity factors for benchmarking.

For the purpose of benchmarking with previously reported studies, which commonly reported synaptic nonlinearity in the form of the exponential fitting parameter A (i.e., A=1/v), all nonlinearity factors in this study were converted to the A-form for consistent comparison in the benchmark graph. For studies that employed NeuroSim-based modeling, the conversion between nonlinearity factor formats was performed using the lookup table.[S1, S2] Furthermore, to ensure consistency across different studies, values extracted from unnormalized pulse domains were converted by dividing the reported A values by the maximum number of pulses (P_{max}) used in the potentiation or depression experiments. This normalization step enables all A values to be interpreted on a common pulse index scale ranging from 0 to 1.

Table S1 provides a detailed summary of the conversion process for each referenced study included in the benchmark plot of **Figure 2g**. Specifically, it lists (i) the original format in which the nonlinearity factor was reported (e.g., v, A, or other), (ii) whether normalization of the pulse domain was required, (iii) the method used for converting the original value to the standardized A-form, and (iv) the final A value used in the benchmarking analysis in **Figure 3b**.

Table S1 | Summary of reported and converted nonlinearity factors used in benchmarking.

This table provides reference-by-reference details of the conversion process, including the original reported values and the final normalized A values used in **Figure 2g**.

Main text reference	(i) Reported format	(ii) Pulse normalization	(iii) Conversion applied	(iv) Final A value
[11]	v_p = 2.28 v_d = 2.46	Yes	$v \rightarrow A$ conversion (A= 1/v)	A_p = 0.439 A_d = 0.407
[40]	A_p = 2.31 A_d = −1.32	-	-	A_p = 2.31 A_d = -1.32
[49]	A_p = 2.4 A_d = −4.6	No	Pulse normalization by dividing P_{max}	A_p = 0.008 A_d = −0.015
[50]	NL_{pot}: 2.18 NL_{dep}: 1.36	Yes	$NL \rightarrow A$ conversion (by using lookup table)	A_p = 0.3093 A_d = 0.199
[51]	NL_{LTP}: 1.8 NL_{LTD}: −1.3	Yes	$NL \rightarrow A$ conversion (by using lookup table)	A_p = 0.6185 A_d = -0.9569
[52]	A_{LTP}: 0.5077 A_{LTD}: 0.5996	Yes	-	A_p = 0.5077 A_d = 0.5996
[53]	v_p = 0.15 v_d = 0.35	No	1. $v \rightarrow A$ conversion (A=1/v) 2. Pulse normalization by dividing P_{max}	A_p = 0.667 A_d = 0.2857
[54]	NL_{pot} = 2.4 NL_{dep} = 1.55	Yes	$NL \rightarrow A$ conversion (by using lookup table)	A_p = 0.4992 A_d = 0.7974
[55]	NL_{pot} = 9.97 NL_{dep} = 7.93	No	Pulse normalization by dividing P_{max}	A_p = 0.199 A_d = 0.159
[56]	A_{pot} = 0.9997 A_{dep} = N/A	Yes	-	A_p = 0.9997 A_d = N/A (~ 0)
[57]	A_p = 8.28 A_d = 7.09	No	Pulse normalization by dividing P_{max}	A_p = 0.1656 A_d = 0.1418
[58]	NL_{LTP} = 2.45 NL_{LTD} = 0.38	Yes	$NL \rightarrow A$ conversion (by using lookup table)	A_p = 0.4879 A_d = 3.3187
[59]	α_{LTP} = 0.008 α_{LTD} = −0.014	No	1. $\alpha \rightarrow A$ conversion (eqn. by α=1.726/(A+0.162) provided in [54]) 2. Pulse normalization by dividing P_{max}	A_p = 0.431 A_d = -0.247
[60]	NL_{LTP} = 0.68 NL_{LTD} = 1.98	Yes	$NL \rightarrow A$ conversion (by using lookup table)	A_p = 1.8494 A_d = 0.6156
[61]	NL_{LTP} = 2.38 NL_{LTD} = 0.97	Yes	$NL \rightarrow A$ conversion (by using lookup table)	A_p = 0.5038 A_d = 1.291
This work	v_p = 1.33 v_d = 1.30	Yes	$v \rightarrow A$ conversion (A=1/v)	A_p = 0.752 A_d = 0.771

Table S2 | Comparison of performance parameters among recently reported metal-embedded memristors.

Ref. No.	Device structure	Embedded element	Switching mechanism	Synaptic property	G_{max}/G_{min} [a)]	# of states	Endurance	Linearity (pot/dep)	Operation voltage & switching speed	Pattern recognition accuracy
S3	TaN/Al_2O_3:Ag:ZnO/ITO	Ag NCs	Filamentary	pot & dep	~2.2	7 bits	-	-	Pot.: +0.5 V, 150 ms Dep.: −0.5 V, 150 ms	-
S4	TiN/Ti/TiO_{2-x}/Pt(or Ta)-NCs/TiO_{2-x}/Au	Pt or Ta NCs	Modulation of filament diameter	pot & dep, STDP	Pt: ~9 Ta: ~2	3 bits	$> 10^7$ (Digital, Pulse switching cycle)	-	Pot.: +5 V, 10 µs Dep.: −5 V, 10 µs	-
S5	Al/PVPy:Au NPs/ITO	Au NPs	Charge trapping-detrapping	SRDP, STP (including PPF, PTP), LTP, learning-forgetting-relearning behavior	-	3 bits	-	-	+5V, 100 ms	-
S6	TaN/TiN/Ti/Al:HfO_2/TiN/TaN	Al	Filamentary	pot & dep	~2.6	6 bits	-	η_p=~22% η_d=~60%	Pot.: +2.5V, 100 µs Dep.: −2.4V, 100 µs	-
S7	Al/Au@Al_2O_3/ITO	Au@Al_2O_3	Charge trapping-detrapping	LTP & LTD, SRDP, SADP	-	4 bits	> 27000 (> 1000 cycle)	-	+15 V, 100 ms	-
S8	Pt/Al:HfO_2/TiN	Al	Filamentary	pot & dep, STDP, LTP&LTD	~11.2	4 bits	-	-	ISPP, 100 µs	-
S9	Pt/HfO_x:Mg/TiN	Mg	Filamentary	pot & dep	~8.4	6 bits	-	-	Pot.: +0.7V, 60 ns Dep.: −0.9V, 60 ns	-
S10	ITO/HfAlO/TiN-NP/HfAlO/ITO	TiN-NP	Filamentary	pot & dep, STDP, SRDP, SADP	~4	6 bits	$> 10^3$ (Digital, DC switching cycle) > 2800 (35 cycle)	-	Pot.: +0.3 V to +1.1 V, 100 µs (ISPP) Dep.: –0.78 V to –1.58 V, 100 µs (ISPP)	-

S11	ITO/HfAlO/TaN-NP/HfAlO/ITO	TaN NP	Filamentary	pot & dep, SRDP, SADP	~1.6	5 bits	$> 10^3$ (Digital, DC switching cycle) > 1000 (> 5 cycle)	-	Pot.: −0.6 V ~ −1.18 V, 100 µs Dep.: +0.8 V ~ +1.62 V, 100 µs	-
S12	ITO/HfAlO/Pt-NPs/HfAlO/ITO	Pt-NPs	Filamentary	pot & dep, LTP & LTD, STDP	~2.5	5 bits	> 500 (Digital, DC switching cycle)	-	Pot.: +0.4 V ~ +1.18 V, 100 µs ep.: −0.6V ~ −1.38 V, 100 µs	-
S13	Al/SF:Au NPs/ITO	Au NPs	Filamentary	pot & dep	~2.2	4 bits	-	-	Pot.: −0.2 V ~ −0.65 V (ISPP), 100 µs Dep.: +1.1 V ~ +1.3 V (ISPP), 100 µs	-
S14	TiN/HfO_x/TiN-NCs/HfO_x/TiN	TiN-NCs	Filamentary	pot & dep, EPSC, LTP & LTD, PPF, STDP, SRDP, SADP	10.4 (single cell) 1.85 (VRRAM)	5 bits	> 500 (Digital, DC switching cycle)	-	Pot.: −2.2 V, 1 ms Dep.: +2.5 V, 1 ms (single cell) Pot.: −3.2 V, 1 ms Dep.: +3.5 V, 1 ms (VRRAM)	MNIST ~ 95 % (VRRAM)
S15	Pt/Ti/HfO_x/TiN-NCs/HfO_x/TiN	TiN-NCs	Filamentary	pot & dep, EPSC, SRDP, SADP, STDP	~ 16.5	5 bits	$> 10^4$ (Digital, pulse switching cycle)	-	Pot.: −1.7 to −2.18 V (ISPP), 10 µs Dep.: 1.8 to 2.29 V (ISPP), 10 µs	MNIST ~ 95 % (VRRAM)
S16	ITO/$HfTiO_x$/Au-NP/$TiSiO_x$/TaN	Au-NP	Filamentary	pot & dep, SADP, STDP, STP to LTP transition, STM function (SRDP, SDDP), experience-dependent plasticity	~ 1.9	5 bits	$> 10^5$ (Digital, pulse switching cycle)	-	+3.8 V / 1 ms	MNIST 82.36 % (fully memristor-oriented RC system)
This work	**Pt/$VCeO_x$:Ag/Pt**	**Ag**	**Metal cation (Ag^+) redistribution**	**pot & dep, SRDP, SADP, PPF, STM to LTM transition**	**~ 1.2**	**9 bits**	**> 18000 (> 300 cycle)**	**v_p = 1.33 v_d = 1.30**	**Pot.: +5 V, 640 µs Dep.: −5 V, 640 µs**	**MNIST 90.6 % (RC system)**

[a)] Dynamic range values were visually estimated from published conductance curves in original paper when not numerically reported.

Supplementary References

S1. P. -Y. Chen, X. Peng and S. Yu, *IEEE International Electron Devices Meeting (IEDM)*, 2017. DOI: 10.1109/IEDM.2017.8268337.

S2. X. Peng, S. Huang and S. Yu, DNN+Neurosim V2.1. https://github.com/neurosim/DNN_NeuroSim_V2.1 (accessed 2025 September).

S3. D. T. Wang, Y. W. Dai, J. Xu, L. Chen, Q. Q. Sun, P. Zhou, P. F. Wang, S. J. Ding and D. W. Zhang, *IEEE Electron Device Lett.,* 2016, **37**, 878–881. DOI: 10.1109/Led.2016.2570279.

S4. P. Bousoulas, I. Karageorgiou, V. Aslanidis, K. Giannakopoulos and D. Tsoukalas, *Phys. Status Solidi,* 2017, **215,** 1700440. DOI: 10.1002/pssa.201700440.

S5. S. R. Zhang, L. Zhou, J. Y. Mao, Y. Ren, J. Q. Yang, G. H. Yang, X. Zhu, S. T. Han, V. A. L. Roy and Y. Zhou, *Adv. Mater. Technol.,* 2018, **4**, 1800342. DOI: 10.1002/admt.201800342.

S6. S. Chandrasekaran, F. M. Simanjuntak, R. Saminathan, D. Panda and T. Y. Tseng, *Nanotechnology,* 2019, **30**. 445205 DOI: 10.1088/1361-6528/ab3480.

S7. F. M. Ma, Z. W. Xu, Y. Liu, Y. T. Zheng, W. Chen, H. L. Hu, T. L. Guo, F. S. Li, C. X. Wu and T. W. Kim, *IEEE Electron Device Lett.,* 2019, **40**, 1610–1613. DOI: 10.1109/Led.2019.2934895.

S8. S. Roy, G. Niu, Q. Wang, Y. Wang, Y. Zhang, H. Wu, S. Zhai, P. Shi, S. Song and Z. Song, *Interfaces,* 2020, **12**, 10648–10656. DOI: doi.org/10.1021/acsami.9b21530.

S9. L. Li, K. Xue, L. Zou, J. Yuan, H. Sun and X. Miao, Appl. Phys. Lett., 2021, **119**, 153505**.** DOI: 10.1063/5.0065840

S10. C. Mahata and S. Kim, *Chaos Solitons Fractals,* 2021, **153**, 111518**.** DOI: 10.1016/j.chaos.2021.111518.

S11. C. Mahata, H. Algadi, M. Ismail, D. Kwon and S. Kim, *J. Mater. Sci. Technol.,* 2021, **95**, 203–212. DOI: 10.1016/j.jmst.2021.03.079.

S12. H. Algadi, C. Mahata, T. Alsuwian, M. Ismail, D. Kwon and S. Kim, *Mater. Lett.,* 2021, **298**. 130011**.** DOI: 10.1016/j.matlet.2021.130011.

S13. L. Wang, Y. T. Wang and D. Z. Wen, *J. Alloys Compd.* 2022, **892**, 162180**.** DOI: 10.1016/j.jallcom.2021.162180.

S14. S. Yang, T. Kim, S. Kim, S. Kim, T. H. Kim, M. Ismail, C. Mahata, S. Kim and S. Cho, *Adv. Mater. Interfaces*, 2023, **10,** 2300290. DOI: 10.1002/admi.202300290.

S15. S. Y. Yang, T. Kim, S. Kim, D. W. Chung, T. H. Kim, J. K. Lee, S. Kim, M. Ismail, C. Mahata, S. Kim and S. J. Cho, *Nanoscale*, 2023, **15**, 13239-13251. DOI: 10.1039/d3nr90165c.

S16. C. Mahata, G. Kim, H. So, M. Ismail, C. C. Hsu, S. Kim and S. Kim, *Adv. Funct. Mater.,* 2024, **35**, 2416862. DOI: 10.1002/adfm.202416862.