Supporting Information

Silicon/Graphite Composite Host for Tuned Lithiophilicity in Li Metal Anodes

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Figure S1. CE tests of a) Cu, b) $Cu-Si_{05}Gr_{95}$ and c) $Cu-Si_{15}Gr_{85}$ tested at a current density of 1 mA cm⁻² for 1 mAh cm⁻² Li plating/stripping. And voltage-time profile of d) Cu, as well as e) nucleation overpotentials of Cu-Si_{05}Gr_{95} and Cu-Si_{15}Gr_{85} tested at 1 mA cm⁻².



Figure S2. CE test of a) Cu-Si₁₀Gr₉₀@Li and b) corresponding voltage-time profile as well as c) Voltage-Areal capacity plot evaluated at a current density of 1 mA cm⁻² and 3 mAh cm⁻² Li plating/stripping.



Figure S3. SEM cross section along with EDX analysis of a) of Cu-Si₀₀Gr₁₀₀@Li, b) Cu-Si₁₀Gr₉₀@Li, c) Cu-Si₂₀Gr₈₀@Li and d) Cu-Si₁₀₀Gr₀₀ after 10 plating/stripping cycles (on the plated state) using a current density of 1 mA cm⁻² and a plating capacity of 1 mAh cm⁻².



Figure S4. CE test of a) Cu@Li and b) Li cycled in a full cell against Sulfur cathode using 0.2C rate capability for 150 cycles.



Figure S5. Voltage-Areal capacity plots at cycles a) 5, b) 25, c) 50 and d) 100 of Cu-Si₀₀Gr₁₀₀@Li-S, Cu-Si₂₀Gr₈₀@Li-S and Cu-Si₁₀Gr₉₀@Li-S cells at 0.2C.



Figure S6. Voltage-Areal capacity plots at 3^{rd} cycles of Cu-Si₀₀Gr₁₀₀@Li-S, Cu-Si₂₀Gr₈₀@Li-S and Cu-Si₁₀Gr₉₀@Li-S cells at C-rates of a) 0.1, b) 0.2, c) 0.5 and d) 1C.



Figure S7. Applied equivalent circuit for fitting EIS data of Sulfur full cells.

Sample	Cycle No.	R _s (ohm)	R _{sei} (ohm)	R _{ct} (ohm)	R _{SEI+CT} (ohm)
Cu-Si ₀₀ Gr ₁₀₀ @Li-Sulfur	1 st	4.75	8.88	5.47	14.34
	100 th	5.46	12.6	7.92	20.52
Cu-Si ₂₀ Gr ₈₀ @Li-Sulfur	1 st	5.73	8.41	3.78	12.19
	100 th	8.37	10.47	6.41	16.88
Cu-Si ₁₀ Gr ₉₀ @Li-Sulfur	1 st	4.99	5.3	1.52	6.82
	100 th	5.38	7.9	2.3	10.2

 $\label{eq:stable} \begin{array}{l} \mbox{Table S1}. \ \mbox{EIS fitted data table containing R_s, R_{SEI}, R_{CT} values for each Cu-Si_{00}Gr_{100}@Li-S$, Cu-Si_{20}Gr_{80}@Li-S$ and Cu-Si_{10}Gr_{90}@Li-S$ cells. \end{array}$



Figure S8. Cyclic performance of Cu@Li-NMC.



Figure S9. Voltage-Areal capacity graphs of $Cu-Si_{00}Gr_{100}$ @Li-NMC, $Cu-Si_{10}Gr_{90}$ @Li-NMC and $Cu-Si_{20}Gr_{80}$ @Li-NMC full cells at various cycles including a) 10, b) 25, c)50, d)100 and e)150 at 0.2C.



Figure S10. Voltage-Areal capacity plots at 3rd cycles of Cu-Si₀₀Gr₁₀₀@Li-NMC, Cu-Si₂₀Gr₈₀@Li-NMC and Cu-Si₁₀Gr₉₀@Li-NMC cells at C-rates of a) 0.1, b) 0.2, c) 0.5 and d) 1C.



Figure S11. Applied equivalent circuit for fitting EIS data of NMC full cells.

Sample	Cycle No.	R _s (ohm)	R _{SEI} (ohm)	R _{ct} (ohm)	R _{sei+ct} (ohm)
Si ₀₀ Gr ₁₀₀ @Li-NMC	1 st	3.9	8.5	59.5	68
	100 th	7.93	42.58	204.4	246.98
Si ₂₀ Gr ₈₀ @Li-NMC	1 st	3.4	5.36	45.01	50.37
	100 th	8.3	27.65	130.9	158.55
Si ₁₀ Gr ₉₀ @Li-NMC	1 st	2.9	3.8	20.28	24.08
	100 th	8.9	11.5	48.99	60.49

 $\label{eq:solution} \begin{array}{l} \mbox{Table S2. EIS fitted data table containing R_s, R_{SEI}, R_{CT} values for each $Cu-Si_{00}Gr_{100}@Li-NMC$, $Cu-Si_{20}Gr_{80}@Li-NMC$ and $Cu-Si_{10}Gr_{90}@Li-NMC$ cells$. } \end{array}$



Supporting Information



Figure S12. Voltage-capacity plots for the initial five charge/discharge cycles of a) Cu-Si₀₅Gr₉₅, b) Cu-Si₁₀Gr₉₀ c) Cu-Si₁₅Gr₈₅ d) Cu-Si₂₀Gr₈₀ and e) Cu-Si₁₀₀Gr₀₀ half cells prior to Li plating/stripping. f) the average CE for the initial charge/discharge cycles.