Supporting Information

Top Gate Overlaid Carbon Nanotube Transistor Electronic Synapses Arrays for High-Performance Image Recognition

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Supplementary information

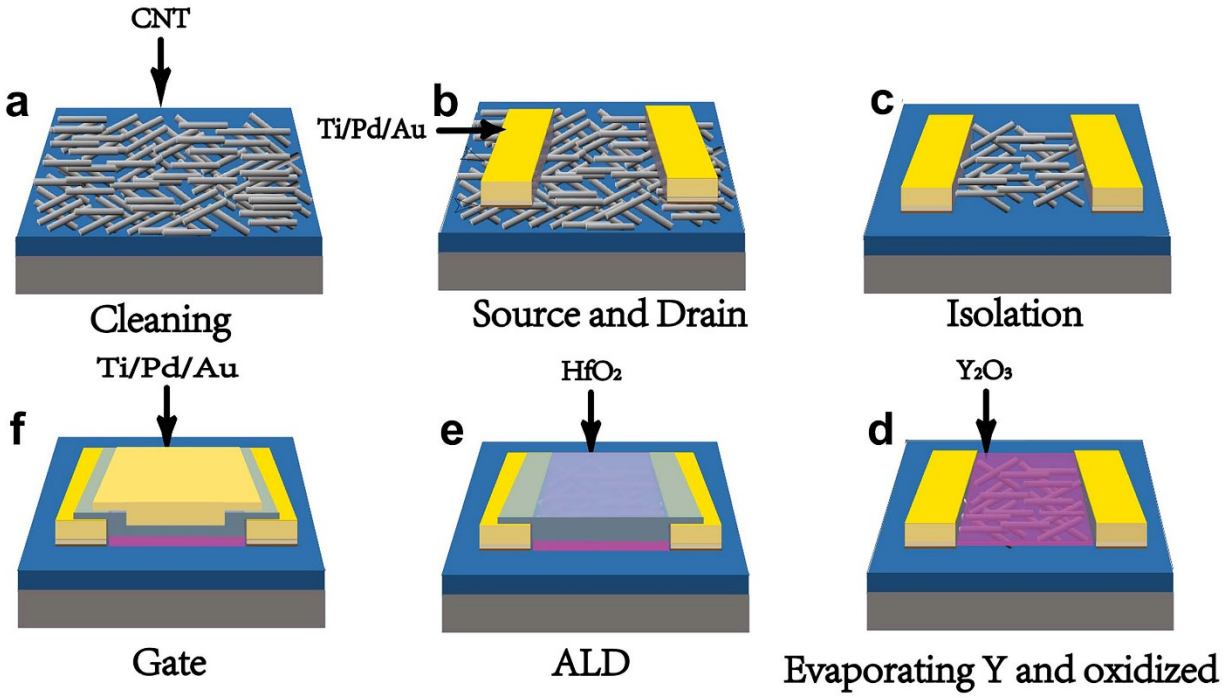

Fig. S1 Schematics showing the process for fabricating a synaptic CNT transistor. (a) A randomly distributed CNT network is deposited. (b)The source (S) and drain (D) electrodes are fabricated and interconnected in the circuit. (c) The CNT network is patterned as a transistor channel. (d) Evaporating Y on the top of the CNT channel and oxidized at 270℃. (e) HfO_2 is grown by ALD. (f) A top gate (G) metal electrode is fabricated on top of the HfO_2 dielectric.

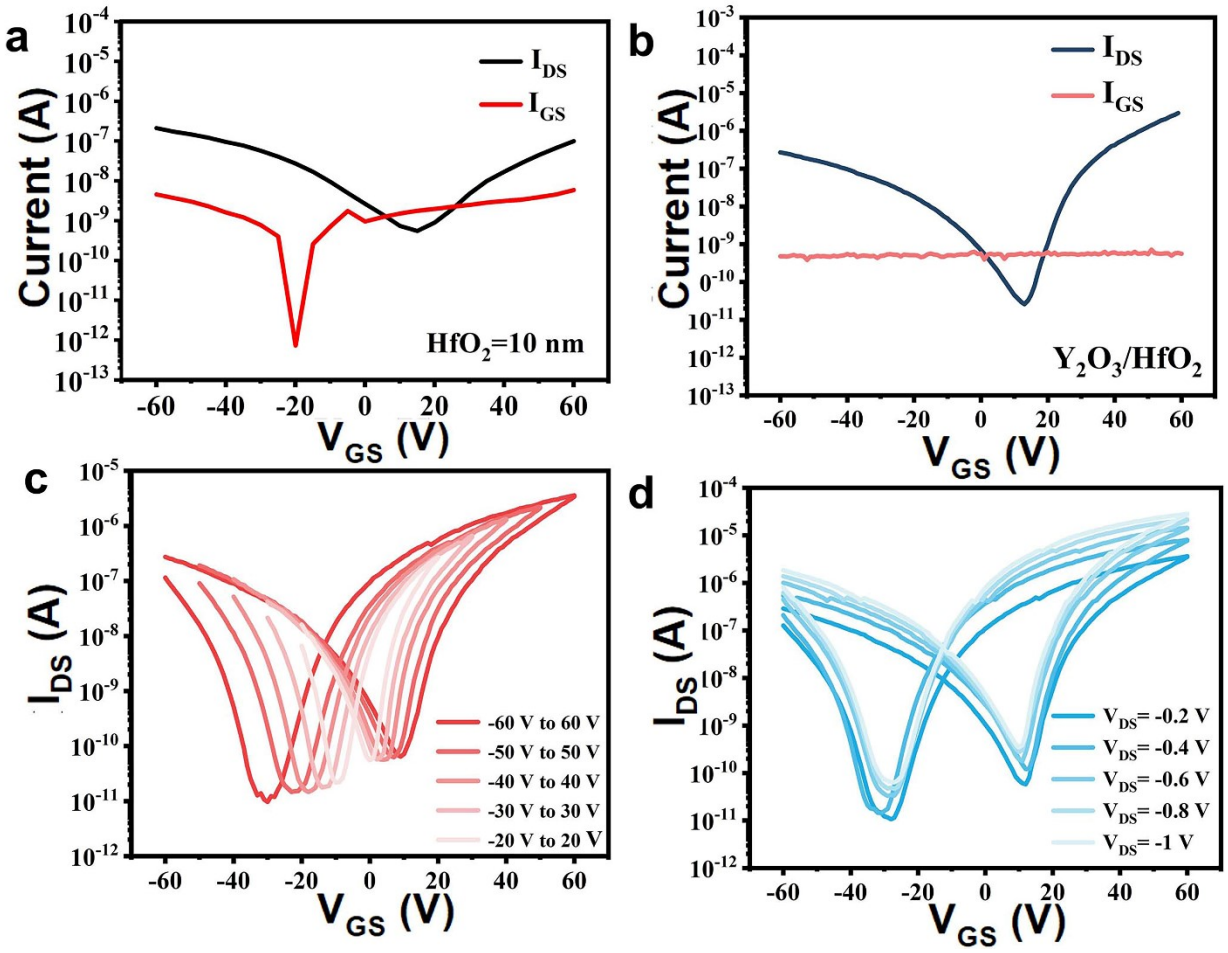

Fig. S2 (a) The transfer curves of back-gate CNTFET with 10 nm HfO_2. (b)The transfer curves of back-gate CNTFET with Y_2O_3/10 nm HfO_2. (c) The hysteresis curve of back-gate CNTFET with Y_2O_3/10 nm HfO_2. (d) The hysteresis curve of back-gate CNTFET with Y_2O_3/10 nm HfO_2.

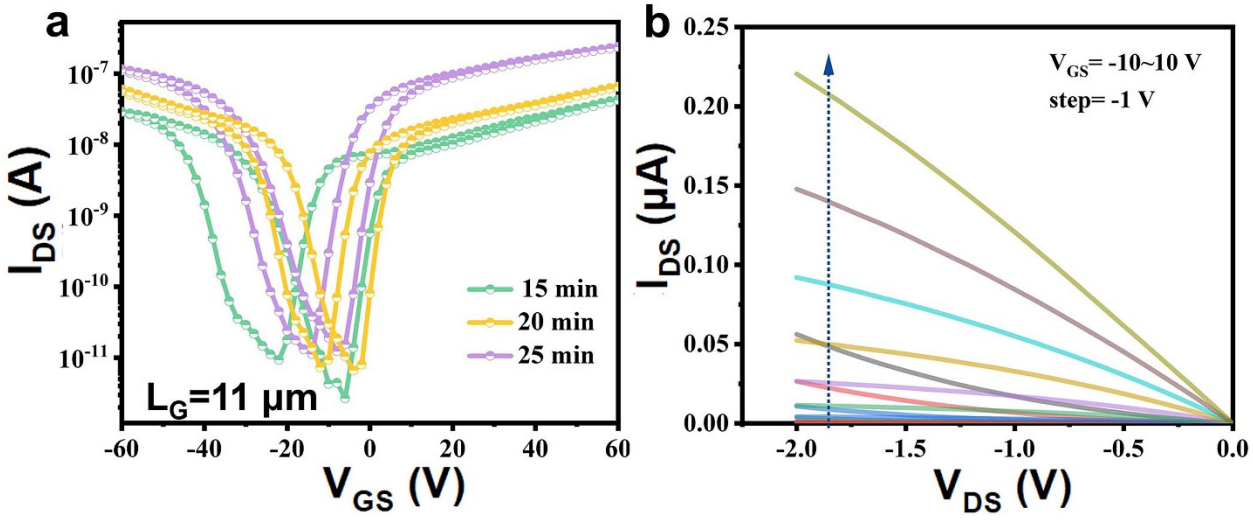

Fig. S3 (a) The transfer curves of back-gate CNTFET with different oxidation times of yttrium. (b) The output curves of back-gate CNTFET with oxidation times of yttrium was 15 min.

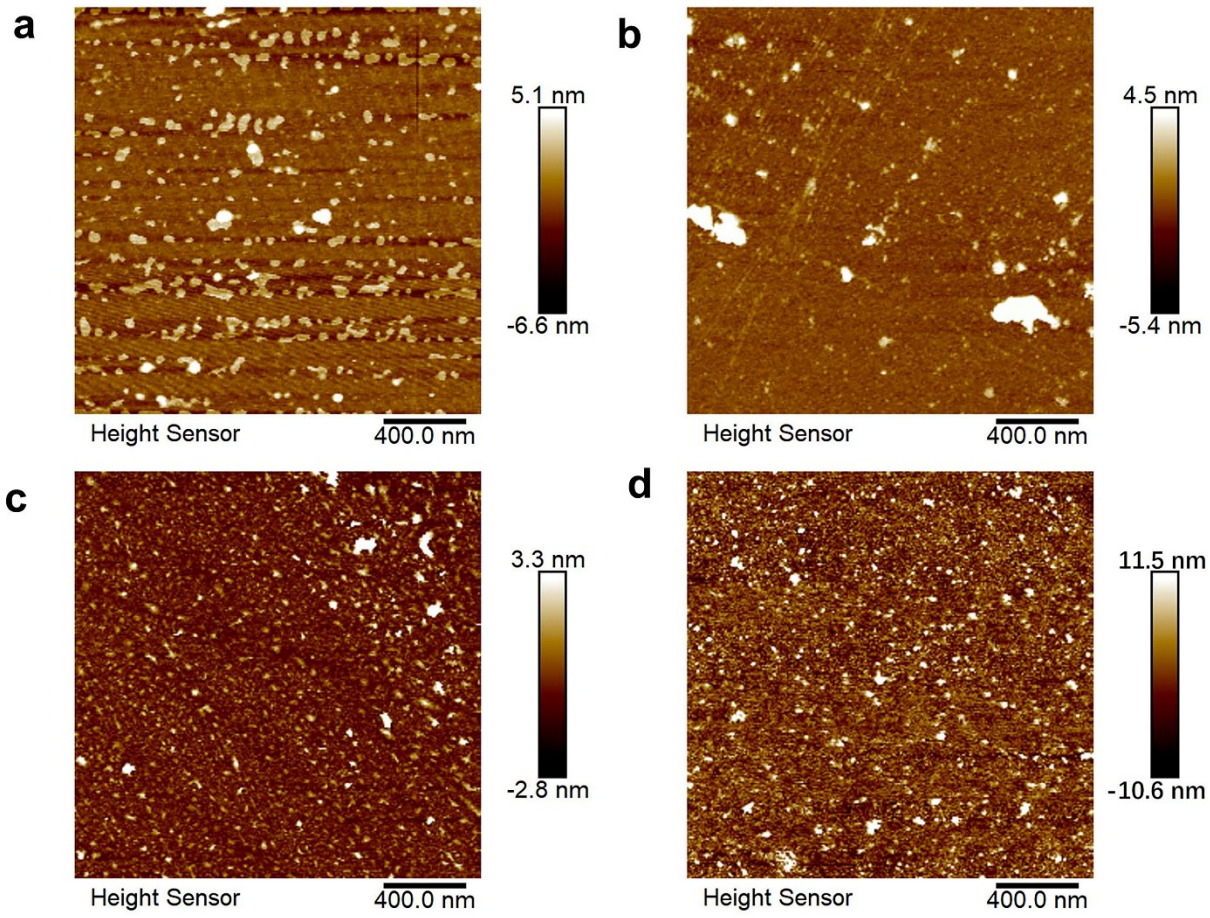

Fig. S4 AFM phase images of yttrium oxidation with (a) 15 min, (b) 20 min, (c) 25 min and (d) HfO_2, respectively.

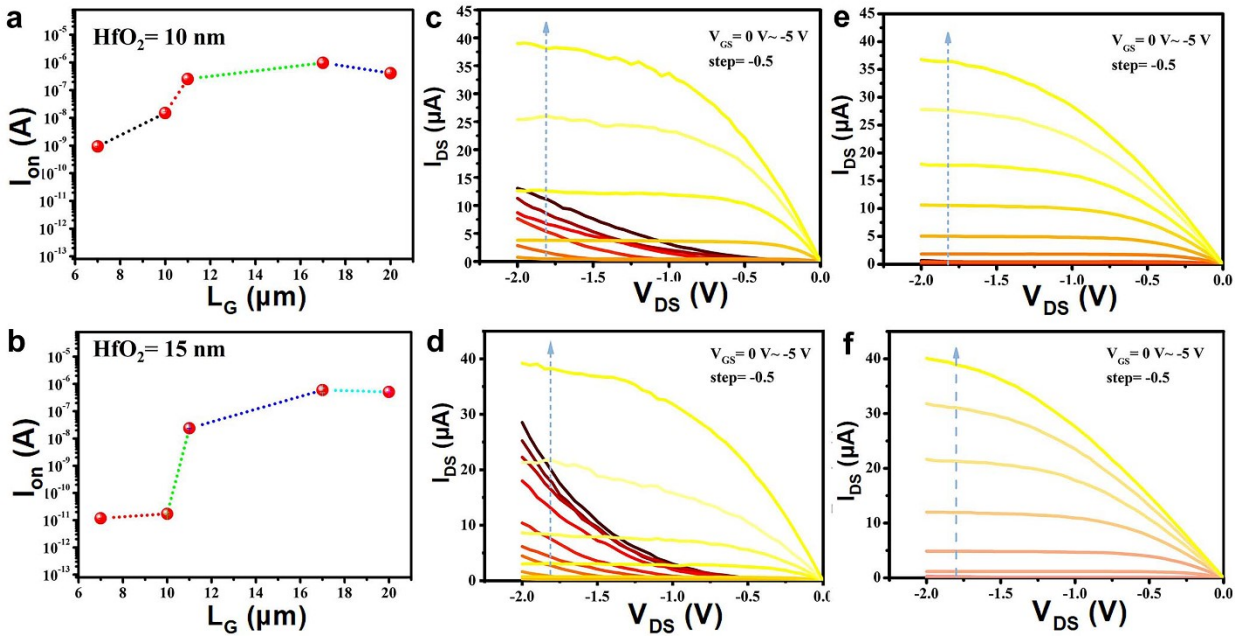

Fig. S5 (a) The on-state current as a function of gate length with CNTFET (V_{DS} = -0.2 V; HfO_2=10 nm). (b) The on-state current as a function of gate length with CNTFET (V_{DS} = -0.2 V; HfO_2=15 nm). The output curve of CNTFET (c) and annealed CNTFET (e) with 10 nm HfO_2. The output curve of CNTFET (c) and annealed CNTFET(e) with 15 nm HfO_2

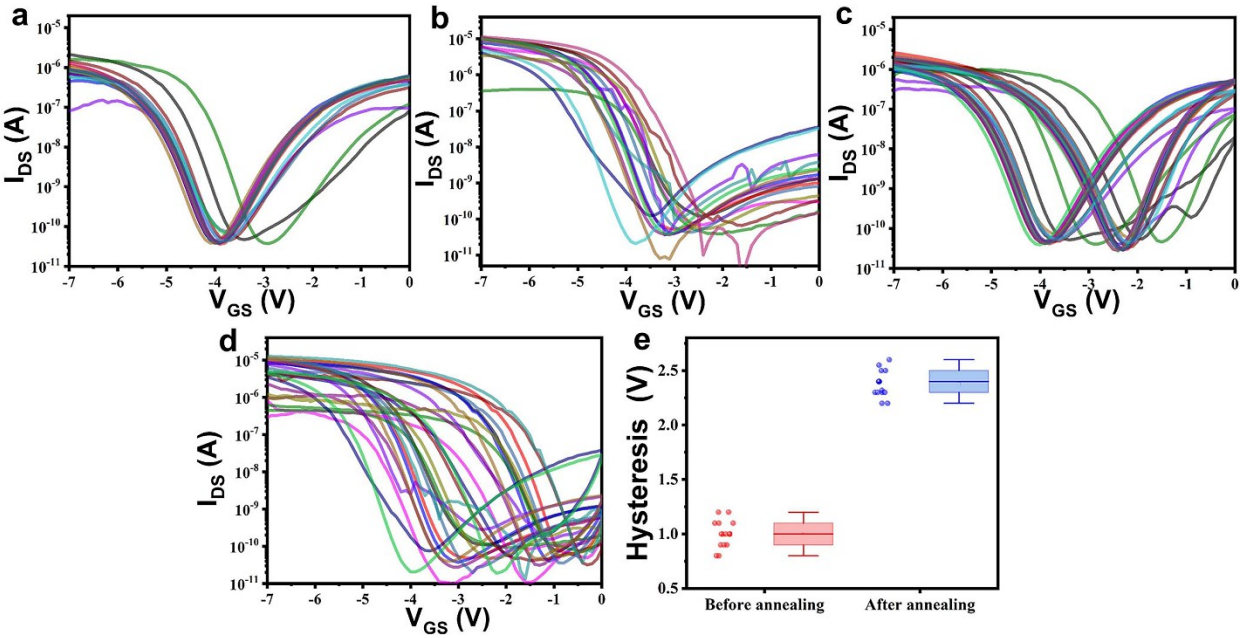

Fig. S6 Transfer curves of TGO-CNTFET (a) and annealed TGO-CNTFET (b). Hysteresis curves of TGO-CNTFET (c) and annealed TGO-CNTFET (d). (e) box plots of hysteresis windows corresponding to hysteresis curves of TGO-CNTFET and annealed TGO-CNTFET.

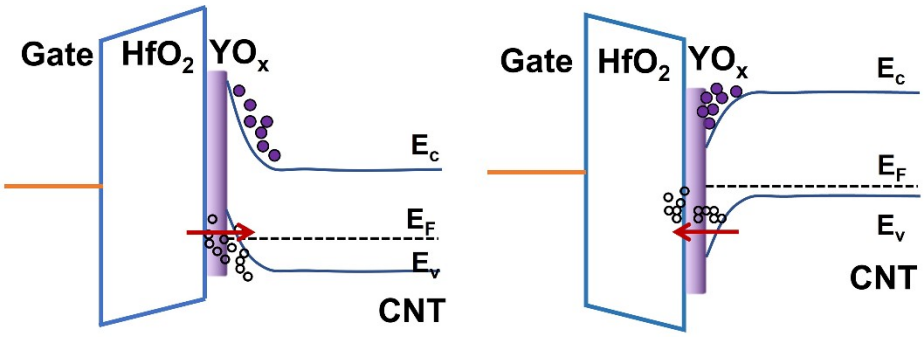

Fig. S7 Energy band diagram illustrating charge-trapping effects in TGO-CNTFET.

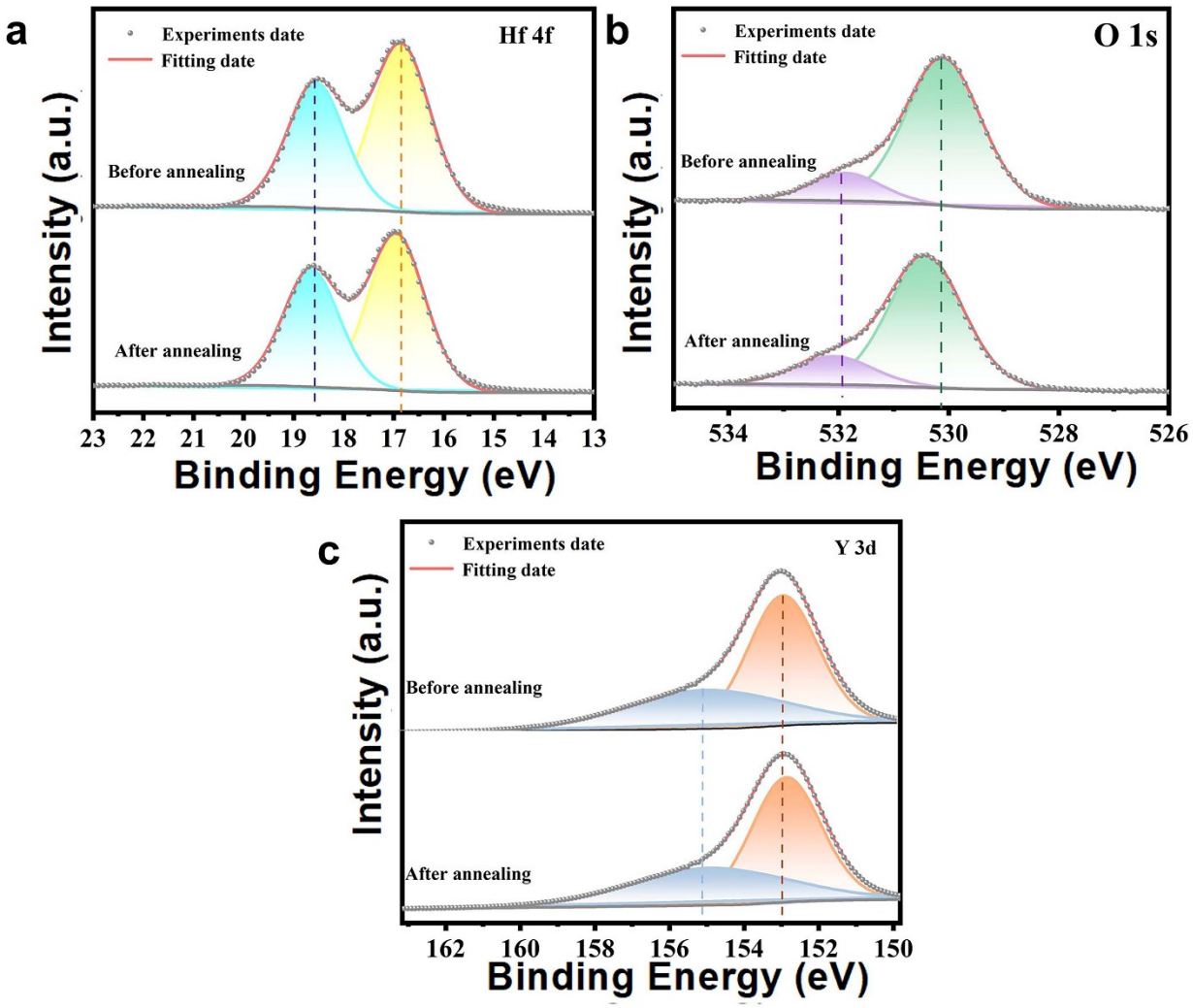

Fig. S8 (a) Compared of XPS results for CNTFET before annealing and after annealing with the Hf 4f spectra (a), O 1s spectra (b) and the Y 3d spectra (c).

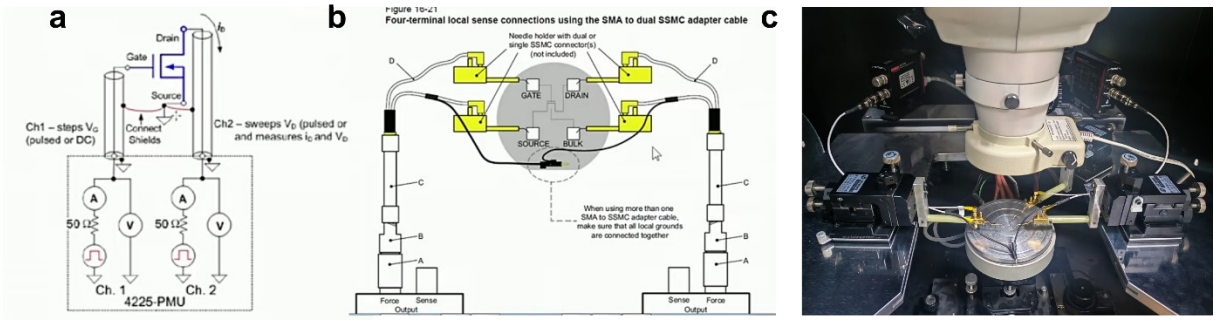

Fig. S9 (a), (b) Electronic synaptic test system and corresponding test photos (c).

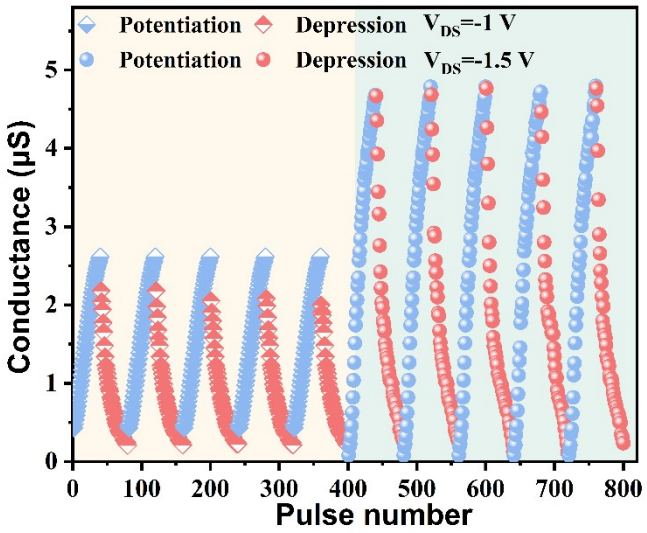

Fig. S10 Operational stability of the LTP/D characteristics of the annealed TGO CNTFET synaptic device under different V_{DS} and of various potentiation/depression pulse sets.

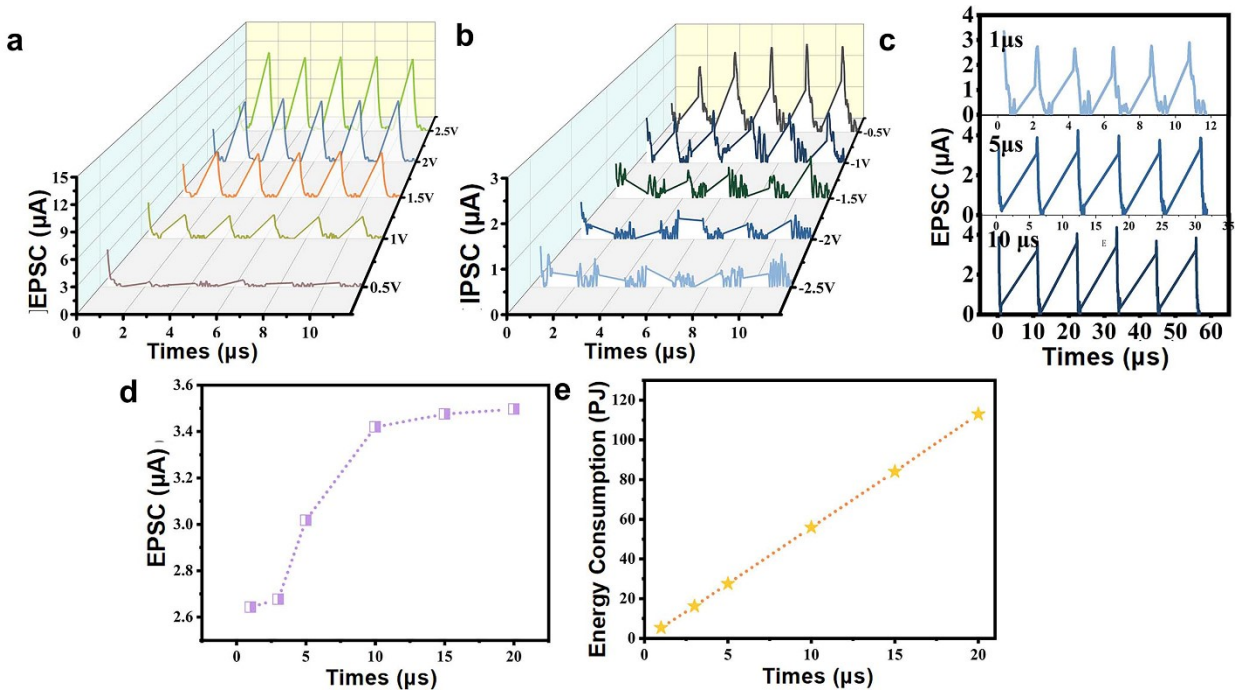

Fig. S11 (a) EPSC varies with the pre-synaptic pulse amplitude. (b) IPSC varies with the pre-synaptic pulse amplitude. (c)EPSC varies with the pre-synaptic pulse width. (d)The relationship curve between pulse width and EPSC. (e) Energy consumption of CNTFET.

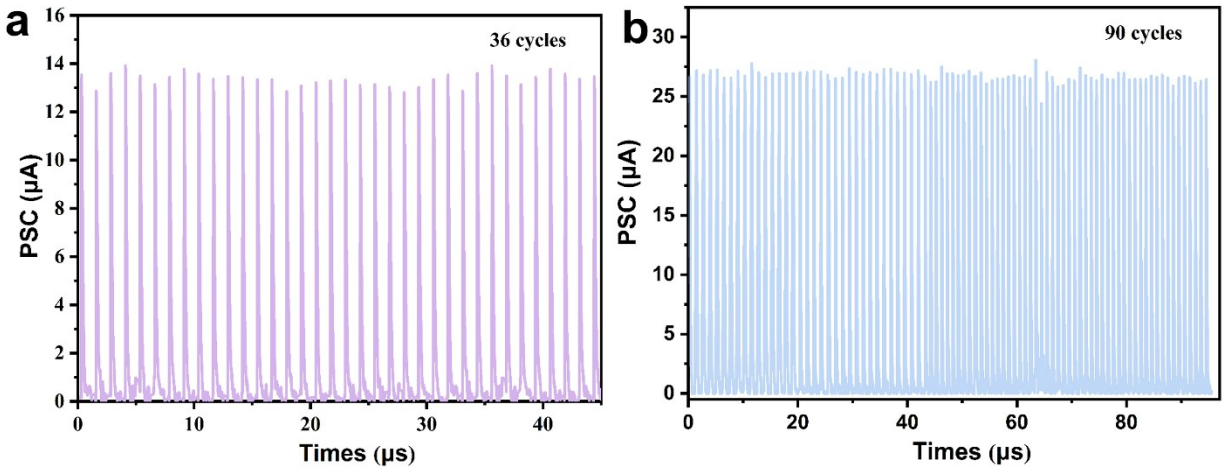

Fig. S12 Operation PSC stability of TGO CNTFET (a) and (b) annealed TGO CNTFET.

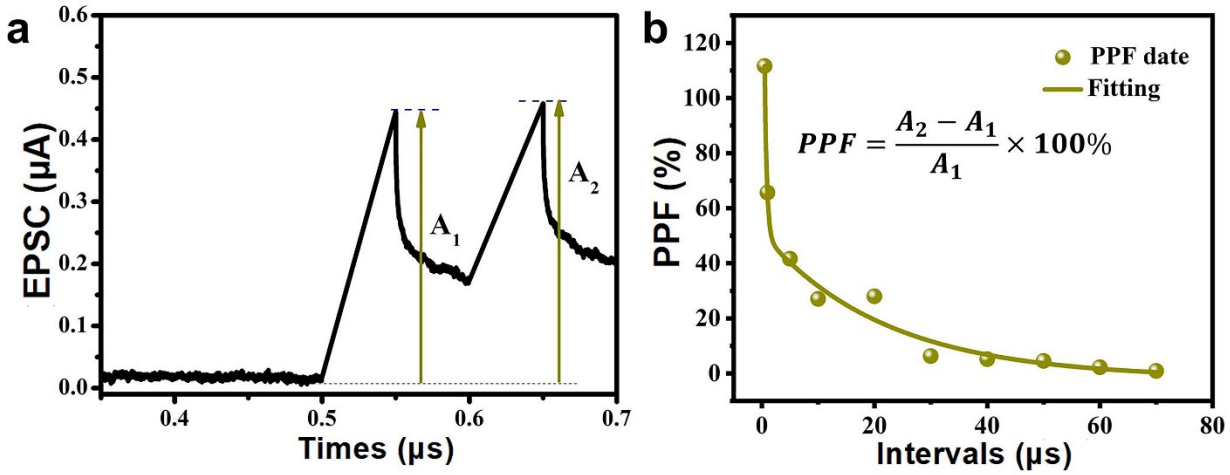

Fig. S13 (a) EPSC triggered by paired spikes (each spike: 3 V, 50 ms). A_1 and A_2 are EPSC value of the first and second spikes, respectively. (b) PPF index varies with pulse interval.

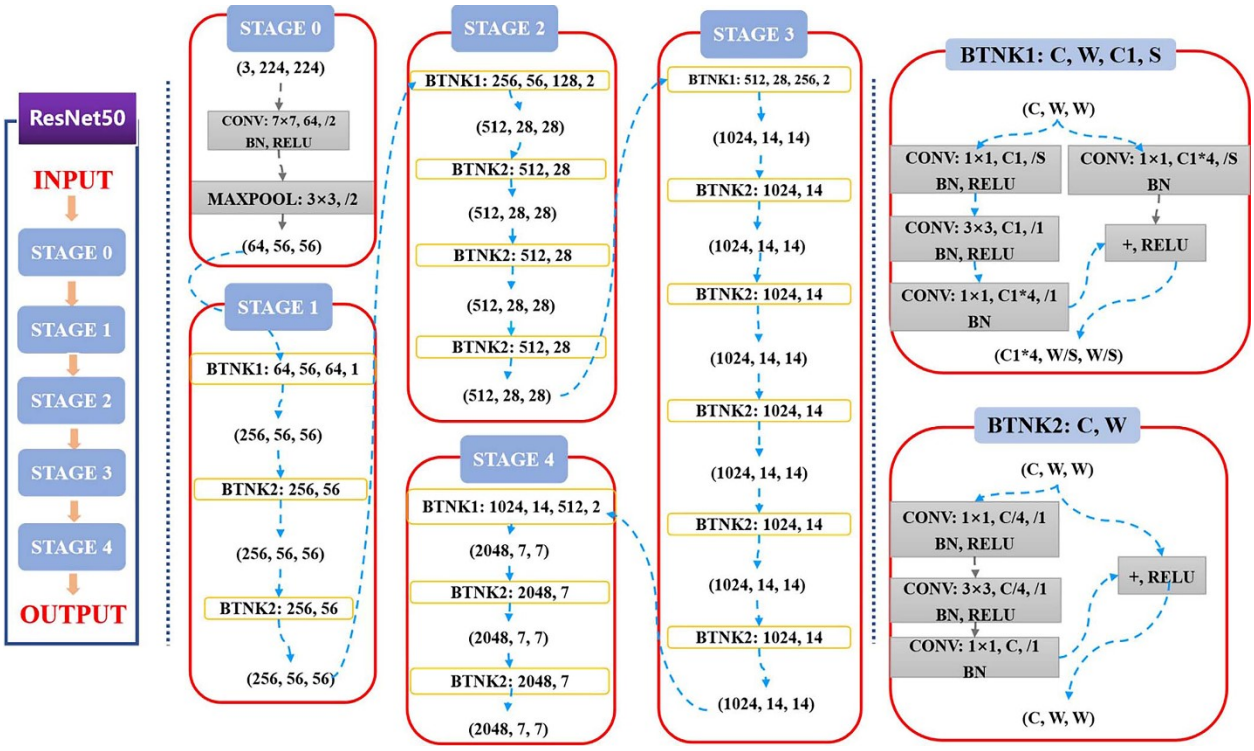

Fig. S14 The detailed flowchart and corresponding key codes of ResNet-50