# Supporting Information

# $SrTiO_3$-based memristor with metal/oxide bilayer electrode for high recognition accuracy neuromorphic computing

*Yan Wang*[1], *Hao Liu*[1], *Wenshuo Wu*[1], *Guorui Yin**[4]*Minghao Zhang*[2], *Jie Su**[1,2,3]

[1]*College of Electronic and Information Engineering, Qingdao University, Qingdao 266071, People's Republic of China*

[2] *College of Physics Science, Qingdao University, Qingdao 266071*

[3] *National Laboratory of Solid State Microstructures, Physics Department, Nanjing University, Nanjing 210093, People's Republic of China*

[4]*Qilu Hospital of Shandong University Dezhou Hospital, Dezhou 253000, People's Republic of China*

** Corresponding authors. E-mail addresses:ygr1007@163.com, jsu@qdu.edu.cn*

## Supporting figures

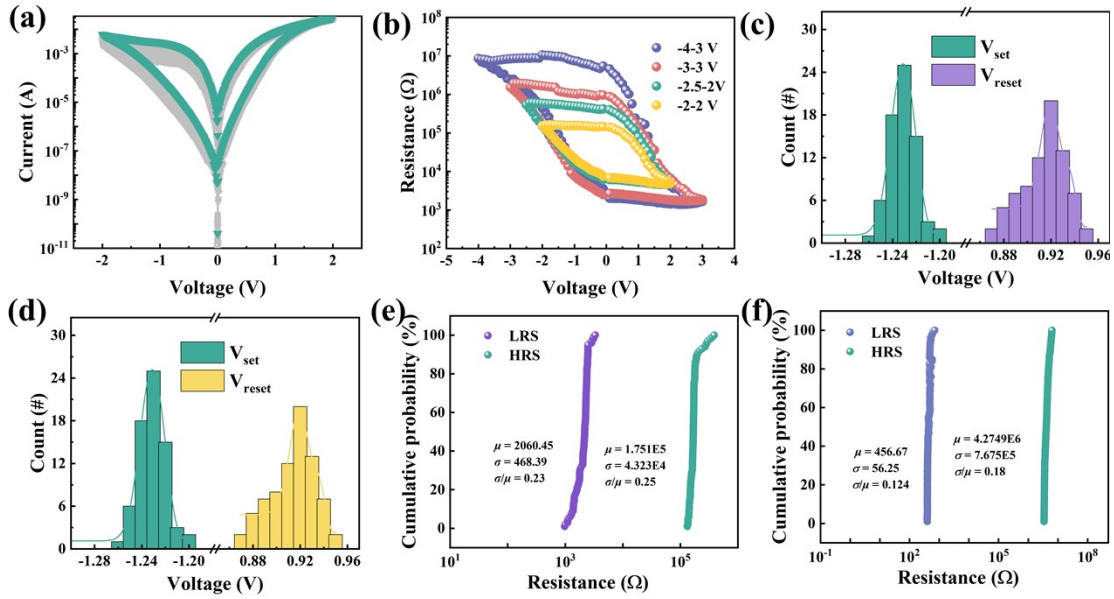


Figure S1. (a) *I-V* curve, (b) *R-V* loops, (c) $V_{set}$ and $V_{reset}$ distribution statistics and (e) Cumulative probability distributions of the *I–V* cycles of Pt/STO/NSTO memristor. (d) $V_{set}$ and $V_{reset}$ distribution statistics and (f) Cumulative probability distributions of Pt/LSMO/STO/NSTO memristor.

Figure S1a shows the 100 cycles *I-V* characteristic of the Pt/LSMO/STO/NSTO memristor. As is shown in Figure S1b, the relationship between resistance (*R*) and voltage (*V*) at different voltages was tested. The histogram of Gaussian fitting results of the threshold voltage is shown in Figure S1c.The Set voltages($V_{set}$) of the Pt/STO/NSTO memristor and Pt/LSMO/STO/NSTO memristor are respectively predominantly centered around 0.9 V and 0.58 V, while the $V_{reset}$ are respectively primarily distributed at approximately -1.24 V and -1,32 V. Figure S1e and S1f depicts the cumulative probability distributions of HRS and LRS, extracted by single electrode memristor and metal/oxide bilayer electrode memristor from the *I–V* curves ($V_{read}$ = 0.1 V), and the $\sigma/\mu$ is calculated. The $\sigma/\mu$ for HRS/LRS is 0.23/0.25 and 0.124/0.18, respectively.

The device is defined as being in HRS when its resistance exceeds $10^3$ Ω, and in LRS when below $10^3$ Ω. Based on this classification, as shown in Figure S2, we systematically determined the characteristic voltage parameters. Specifically, during the forward voltage sweep (0→$V_{max+}$), the critical voltage corresponding to the first resistance drop to $10^3$ Ω was identified as $V_{set}$. Conversely, during the reverse voltage

sweep ($V_{max-}$→0 V), the voltage at which the resistance recovers to $10^3$ Ω was defined as $V_{reset}$.

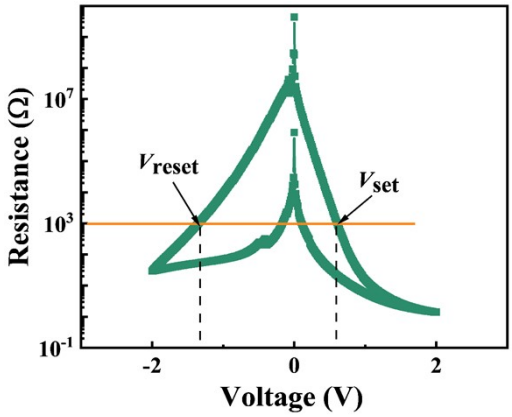


Figure S2 *R-V* curve through data processing of the original *I-V* curve.

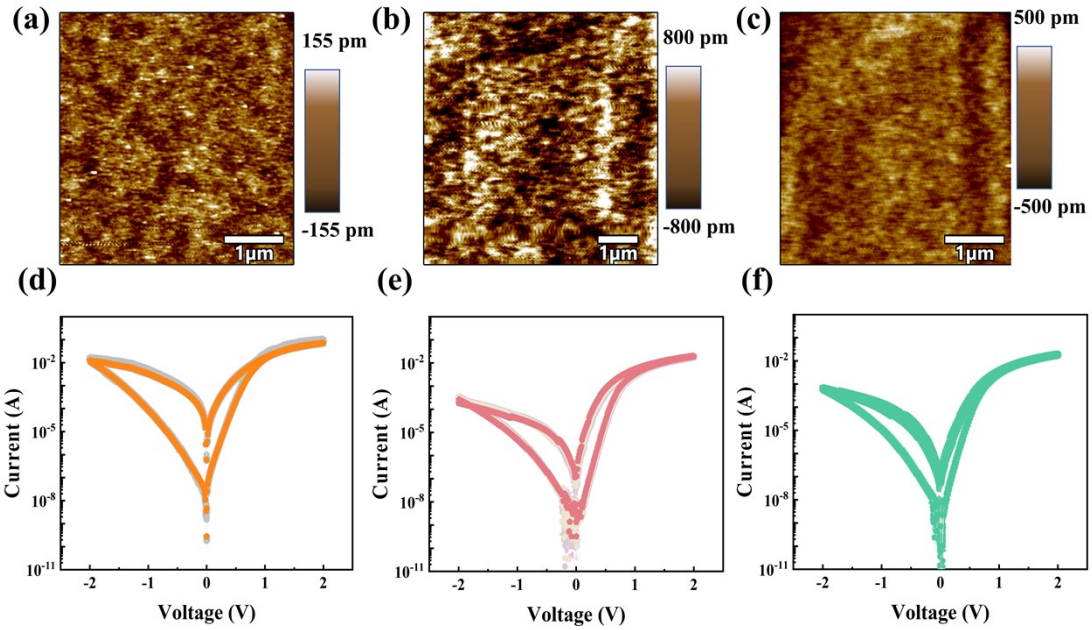


Figure S3. (a-c) AFM topography of STO thin films on different thicknesses of LSMO. (d-f) The *I-V* curves of STO thin films on different thicknesses of LSMO: (a, d) 2 nm, (b, e) 8 nm, (c, f) 10 nm.

As the thickness of LSMO layer may also an effective parameter for the resistance switch characteristics of STO devices, a series STO devices with different LSMO thickness (including 2 nm, 8 nm, 10 nm and 4 nm of LSMO depicted in Figure 1e, f) are carried out. As presented in Figure S3a-c, all the four STO thin films exhibit smooth surfaces with step-like step, confirm the high-quality growth of the thin films. The *I-V* characteristics of the prepared STO thin films are also measured, as shown in Figure S3e-f. When the LSMO thickness is 4 nm, the window of the device is

maximum, and the LSMO thickness continues to increase. At this time, hysterical current appears under the same positive voltage scan. This can be attributed to the increase of LSMO thickness and the decrease of voltage applied to the STO film.

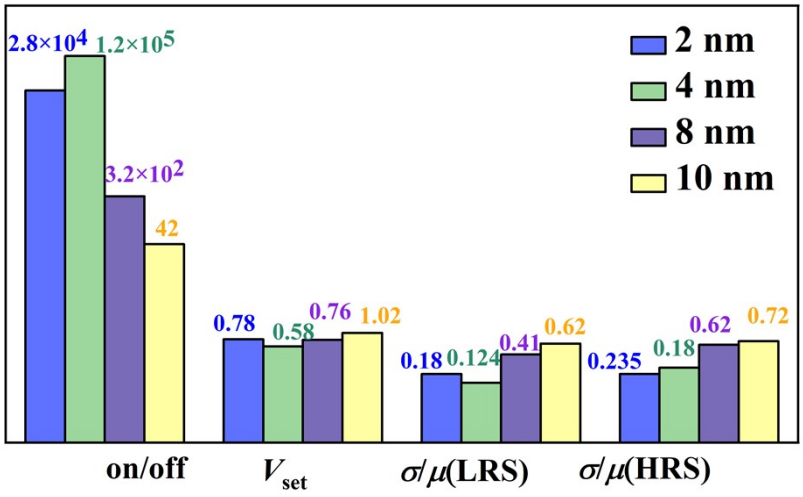


Figure S4 Pt/LSMO/STO/NSTO memristor (LSMO=2 nm) (a) $V_{set}$ and $V_{reset}$ distribution statistics and (b) *R*-*V* curves at different voltages (c) Cumulative probability distributions.

As shown in Figure S4, the 4 nm - thick LSMO memristor exhibits larger on/off ratio, smaller set voltage ($V_{set}$) and higher stability ($\sigma/\mu$) compare to other thicknesses of LSMO films. This operational mechanism stems from the dynamic regulation effect of LSMO layer thickness on $V_O$ concentration, where a 2 nm-thick LSMO layer exhibits relatively low $V_O$ density, and forward bias induces limited $V_O$ migration toward the LSMO/STO heterointerface, allowing only minimal recombination between $V_O$ in the STO layer and negative charges at the left side of the STO/NSTO interface, consequently maintaining a higher LRS during HRS-to-LRS transition. In contrast, 4 nm-thick LSMO layers demonstrate significantly enhanced $V_O$ concentration, enabling rapid ionic migration to the LSMO/STO interface under identical bias conditions, which drives substantial directional movement of $V_O$ toward the STO/NSTO interface within the STO layer, thereby achieving a lower LRS value. Notably, beyond critical LSMO thickness, $V_O$ saturation occurs where further thickness increases not only fail to enhance $V_O$ recombination in the STO layer but also elevate operational voltage requirements.

As shown in Figure S5a, b, the current waveforms of individual pulse pairs over time are presented for $\Delta t > 0$ and $\Delta t < 0$ conditions, respectively. The synaptic weight change ($\Delta\omega$) is defined as follows:

$$\Delta\omega = (\omega_2 - \omega_1)/\omega_1$$

Where $\omega_1$ and $\omega_2$ represent the synaptic weights before and after the pulse sequence.

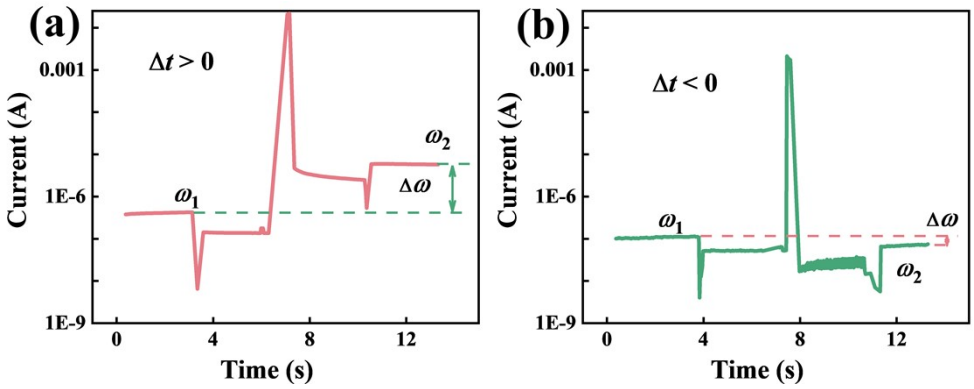


Figure S5 The current waveforms of individual pulse pairs over time are presented for (a) $\Delta t > 0$ (b) and $\Delta t < 0$ conditions.

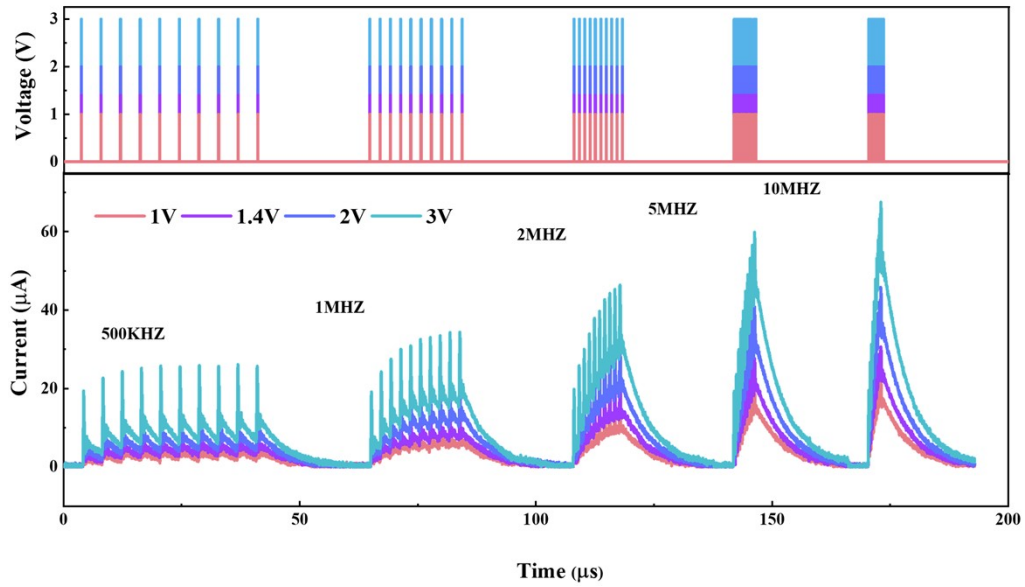


Figure S6 SRDP simulation for different frequency, voltage amplitudes.

As demonstrated in Figure S6, varying voltage amplitudes of 1 V, 1.4 V, 2 V, and 3 V combined with five distinct frequency regimes (500 kHz, 1 MHz, 2 MHz, 5 MHz, and 10 MHz) are applied to probe synaptic current responses. The results reveal a pronounced amplitude-dependent modulation of synaptic conductance. Furthermore, under fixed-amplitude pulse train conditions, the synaptic current exhibits progressive intensification with increasing stimulation frequency, thereby demonstrating successful emulation of SRDP, which establishes a solid foundation for modeling human brain behavior in learning and memory processes.

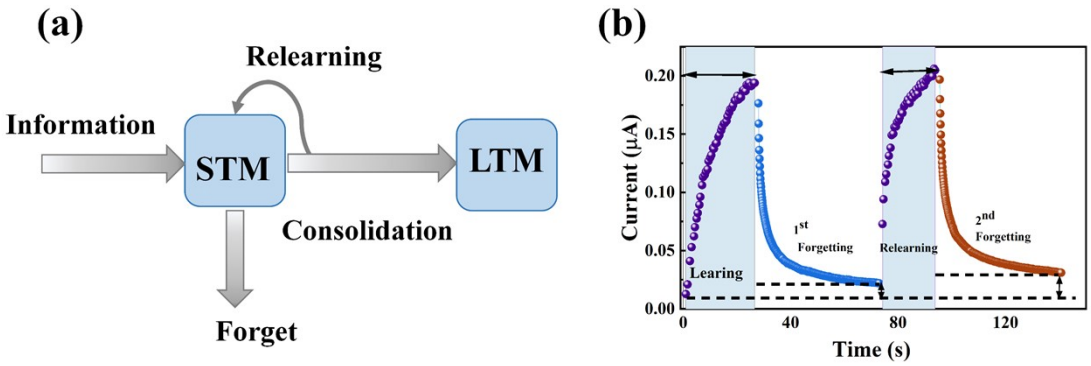


Figure S7 (a) The model of learning-forgetting-relearning. (b) The learning-forgotten relearning simulation process.

In the human brain, the synaptic weight between biological synapses can be enhanced and then consolidate their connection strength through repeated external stimulus, finally the strengthened synaptic weights lead to the transition from STM to LTM, as shown in Figure S7a, S7b shows two learning-forgetting processes by successive pulses. It is obvious that decreasing learning pulses (40, and 20) and reducing learning times (30 and 15s) can achieve the same memory effect, which above all indicates that our artificial synapses can well mimic the learning and memory functions of the human brain.

Retention and endurance are two critical performance parameters for electronic synaptic devices. As shown in Figure S8a and b, the device demonstrates stable retention in both HRS and LRS for about 4000 seconds, along with robust endurance across 200 consecutive switching cycles. These metrics meet the stringent retention and endurance requirements for neural network training, thereby establishing a reliable foundation for neuromorphic computing and simulation applications.

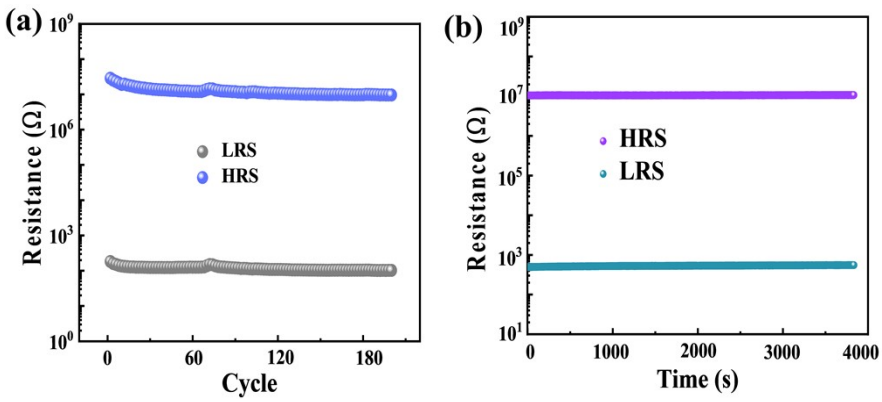


Figure S8 (a) Endurance test of the device within 200 cycles. (b) Retention characterization of the device within 4000 s.

We performed 20 consecutive D-type latch and logic computation simulations on individual devices, as illustrated in Figure S9. The resistance states after each simulated operation were statistically analyzed, yielding coefficients of variation of 0.1 (D = X, Q = 0, Q* = 0), 0.086 (D = 0, Q = 0, Q* = 0), 0.085 (D = 0, Q = 1, Q* = 0), 0.046 (D = X, Q = 0, Q* = 1), 0.661 (D = 1, Q = 0, Q* = 1), and 0.982 (D = 1, Q = 1, Q* = 1), indicating that device has a high endurance in simulating D-type latch.

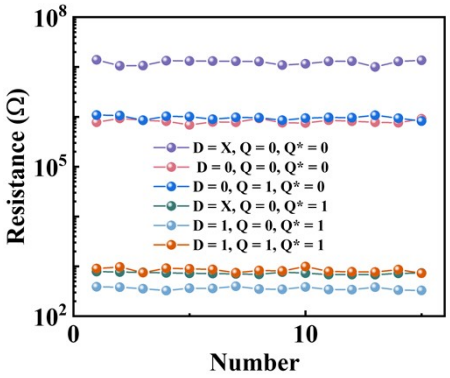


Figure S9 D-type latch's endurance test of the device within 15 times.

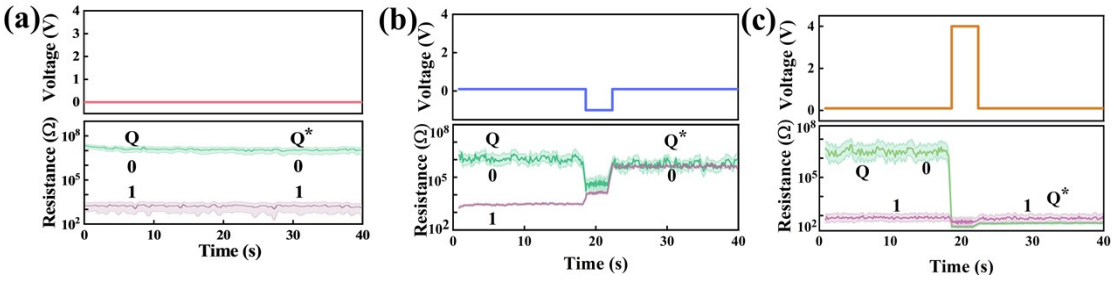


Figure S10 (a-c) The error margin for D-latch functionality achieved by twenty devices.

To quantitatively validate the accuracy of the device in implementing D-latch functionality, the resistance distribution characteristics of HRS and LRS were systematically analyzed across 20 devices during D-latch operations, as illustrated in Figure S10. The results demonstrate that the resistance variations of both HRS and LRS in all devices are consistently confined within one order of magnitude, conclusively verifying the high uniformity of the D-latch functional characteristics achieved by the fabricated devices.

As shown in Figure S11, the current-time characteristics of the device during simulated arithmetic operations were experimentally investigated. The measured data demonstrate that the current exhibited minimal amplitude variations throughout the continuous testing process. This remarkable stability directly confirms the reliable data retention characteristics of the device.

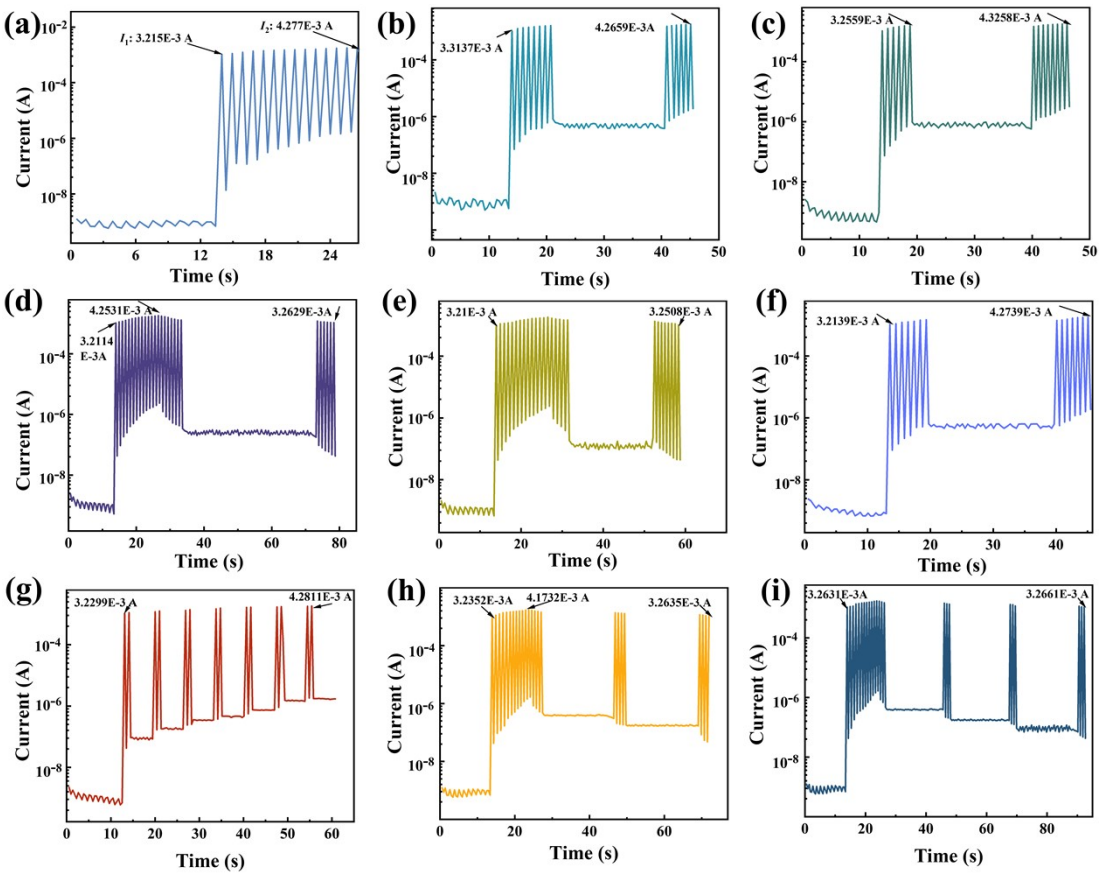


Figure S11 The current-time characteristics of the device during simulated arithmetic operations. (a) Fourteen pulses are used to calibrate the current change of the device to achieve accurate decimal calculation. (b, c) Exchange addition law. (d, e) Law of exchange for subtraction. (f, g) Exchange law of multiplication. (h, i) Subtraction-based division function.

As shown in Figure S12a, to evaluate the durability and consistency of devices in logical operations, repetitive testing comprising 15 trials of addition, subtraction, multiplication, division, and mixed operations was conducted on individual devices, with final weight values extracted post-operation, revealing error ranges of ±0.6%, ±0.8%, ±0.7%, ±0.61%, and ±1.04% respectively. Additionally, 20 independent devices were subjected to arithmetic and mixed operation tests (Figure S12b), demonstrating inter-device error ranges of ±0.9% (addition), ±0.8% (subtraction), ±0.5% (multiplication), ±0.6% (division), and ±1.12% (mixed operations). These results indicate superior operational durability and consistency across fundamental arithmetic operations (all errors below ±3%), confirming high endurance and reliability in basic logic computations.

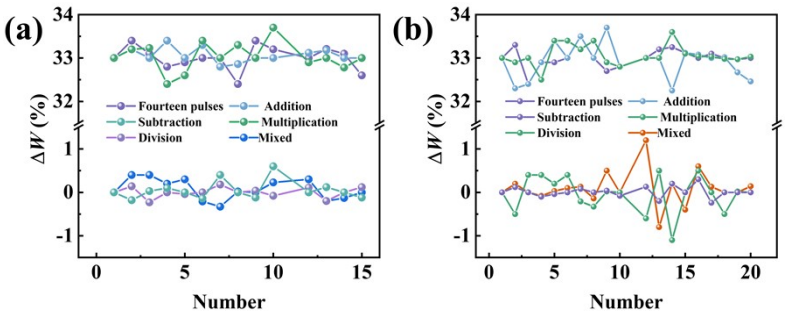


Figure S12 (a) Endurance test of the device within 15 times. (b) 20 independent devices subjected to arithmetic and mixed operation tests.