Enhanced Multifunctional Broadband Artificial Vision through Integration of ReS_2 Phototransistors with Embedded Electrodes

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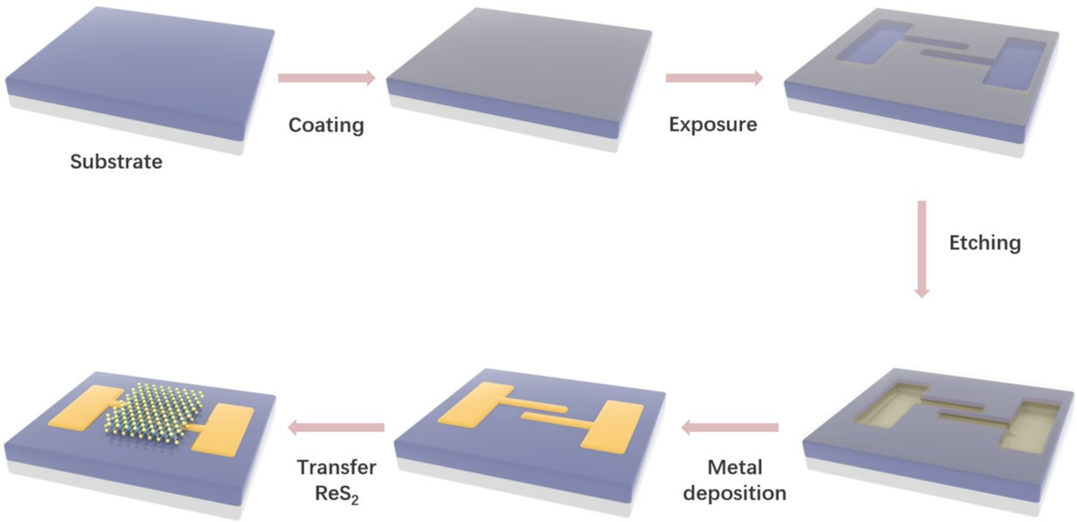

Figure S1. Schematic of the device fabrication process. First, a pattern is defined on a Si/SiO_2 substrate using photolithography. The resist is exposed to create the desired electrode shape, followed by plasma etching (SF_6 and N_2) to a depth of 50 nm. Subsequently, a 5 nm Ni layer is deposited via electron-beam evaporation, followed by thermal evaporation of a 45 nm Au layer to form the electrodes. After electrode deposition, the resist is removed. Finally, mechanically exfoliated ReS_2 flakes are transferred onto the electrodes.

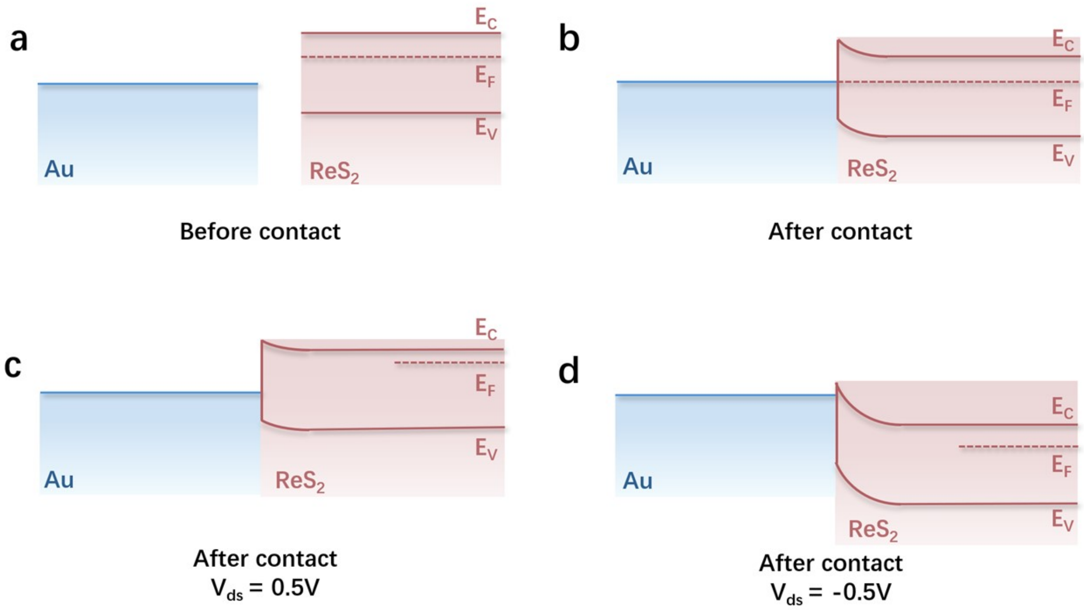

Figure S2. Energy bands of ReS_2 and Au electrodes before and after contact. (a) Energy band alignment of ReS_2 and Au electrodes before contact. (b) Energy band alignment of ReS_2 and Au electrodes after contact. (c) Energy band alignment of ReS_2 and Au electrodes under a 0.5 V forward bias after contact. (d) Energy band alignment of ReS_2 and Au electrodes under a 0.5

V reverse bias after contact.

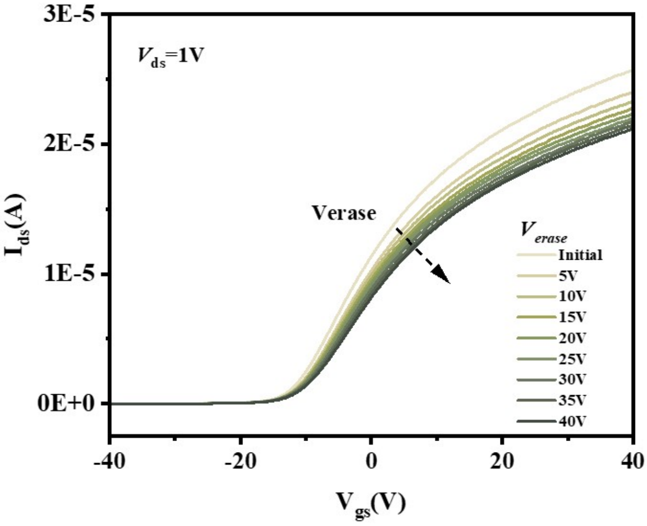

Figure S3. Transfer characteristics modulated by different erase voltages. The gate voltage V_g increases from 5 V to 40 V in steps of 5 V.

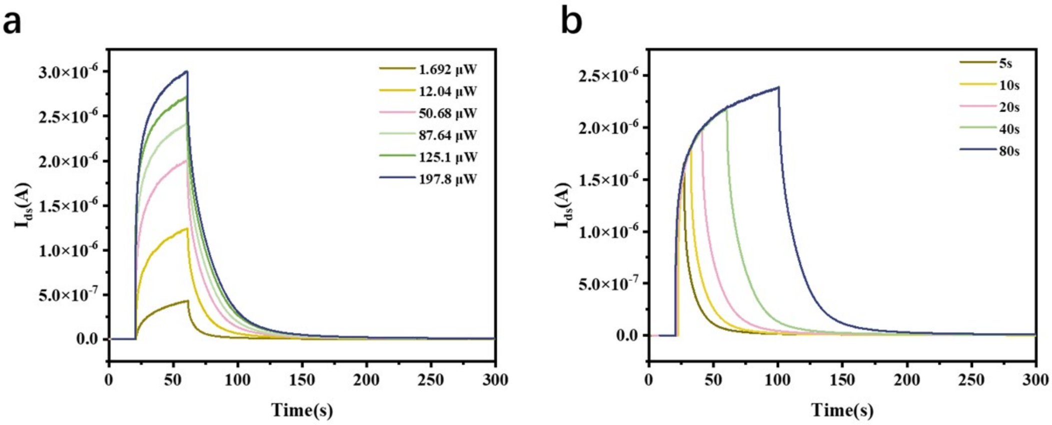

Figure S4. Photoresponse characteristics of Intrinsic ReS_2. (a) Power-dependent photoresponse characteristics of the intrinsic ReS_2 device under 637 nm wavelength laser illumination (pulse width: 40 s). (b) Pulse-width-dependent photoresponse characteristics of the intrinsic ReS_2 device under 637 nm wavelength laser illumination (pulse power: 50.68 μW).

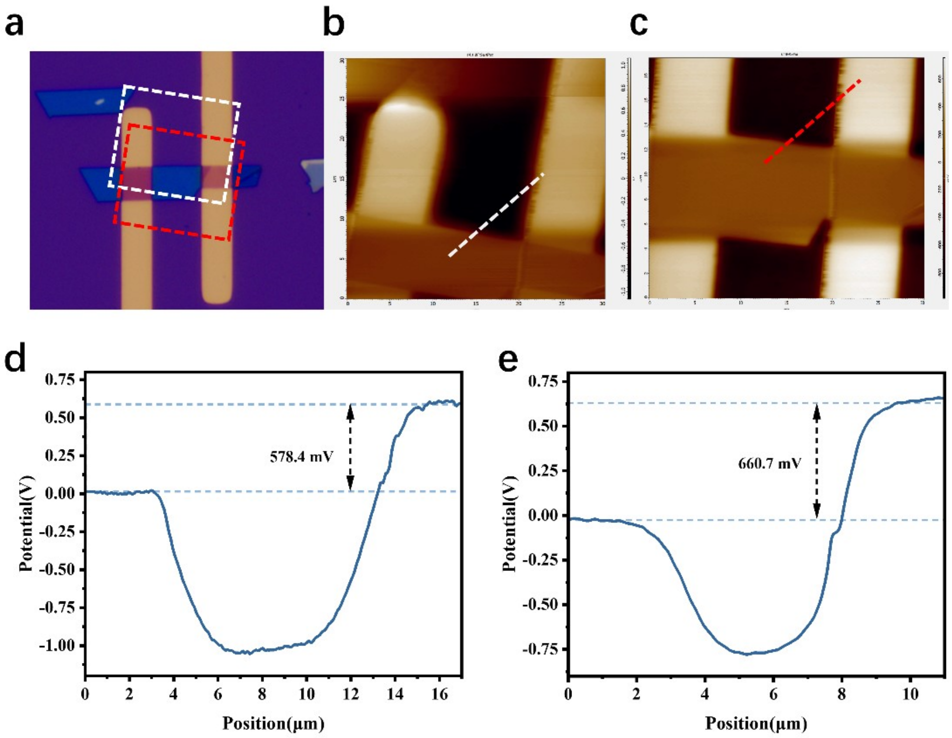

Figure S5. KPFM images before and after illumination. (a) Optical microscopy image of the bottom electrode device.(b) KPFM image of the white region in Figure (a) before illumination. (c) KPFM image of the red region in Figure (a) after illumination. (d) Potential difference between ReS_2 and Au extracted from the line profile in Figure (b) before illumination. (e) Potential difference between ReS_2 and Au extracted from the line profile in Figure (c) after illumination.

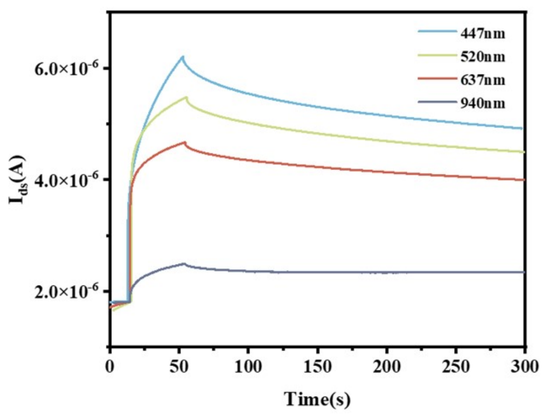

Figure S6. Photoconductive switching characteristics (PSC) of the device under laser illumination at different wavelengths (447, 520, 637, and 940 nm). The pulse width is 40 s, and the pulse intensity is 20 μW for all wavelengths.

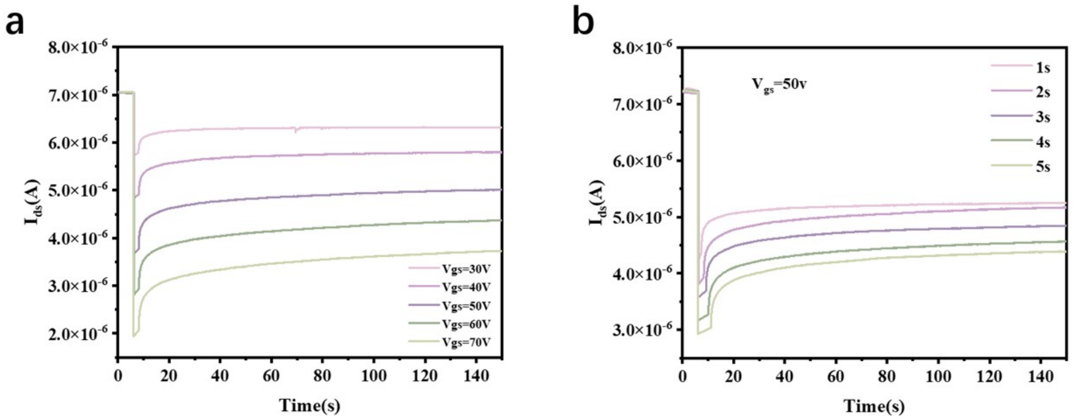

Figure S7. Erase characteristics of the device under positive gate voltage. (a) Retention characteristics of the current after applying erase pulses with a width of 2 s at different intensities. (b) Retention characteristics of the current after applying erase pulses with an intensity of 50 V at different widths.

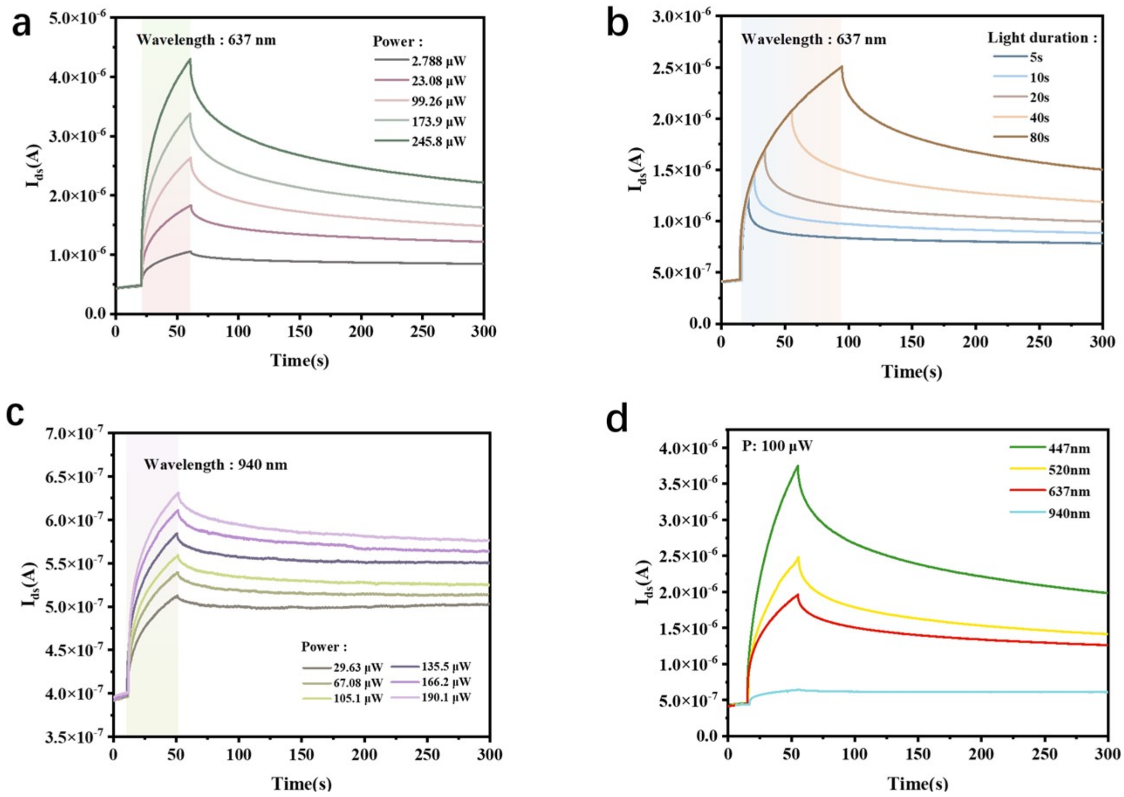

Figure S8. Photoresponse characteristics of device D2. (a) Photoconductive switching characteristics (PSC) of device D2 under 637 nm laser illumination with pulse intensities of 2.788, 23.08, 99.26, 173.9, 245.8, and 378.7 μW. (b) PSC of device D2 under 637 nm laser illumination with pulse widths of 5, 10, 20, 40, and 80 s. (c) PSC of device D2 under 940 nm laser illumination with pulse intensities of 29.63, 67.08, 105.1, 135.5, 166.2, and 190.1 μW. (d) PSC of device D2 under laser illumination at different wavelengths (447, 520, 637, and

940 nm), with a pulse width of 40 s and a pulse intensity of 20 μW.

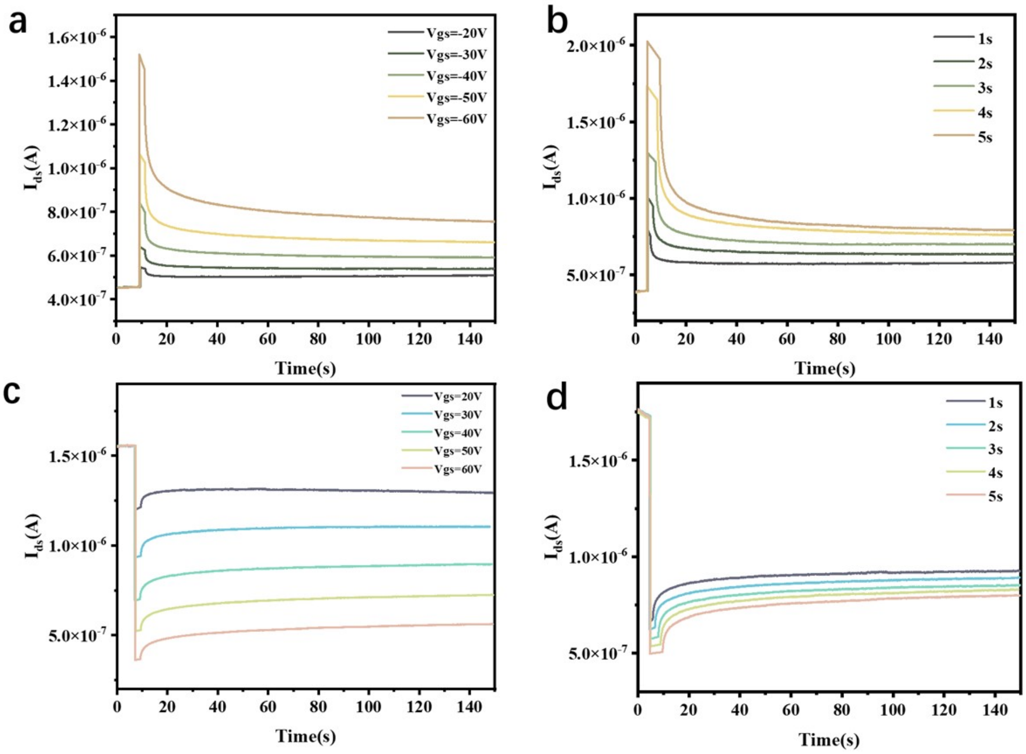

Figure S9. The electrical writing and erasing characteristics of device D2. (a) Photoconductive switching characteristics (PSC) of device D2 under gate voltage pulses with intensities of -20, -30, -40, -50, and -60 V, and a pulse width of 2 s. (b) PSC of device D2 under a -50 V gate voltage pulse with pulse widths of 1, 2, 3, 4, and 5 s. (c) PSC of device D2 under gate voltage pulses with intensities of -20, -30, -40, -50, and -60 V, and a pulse width of 2 s. (d) PSC of device D2 under a 40 V gate voltage pulse with pulse widths of 1, 2, 3, 4, and 5 s.

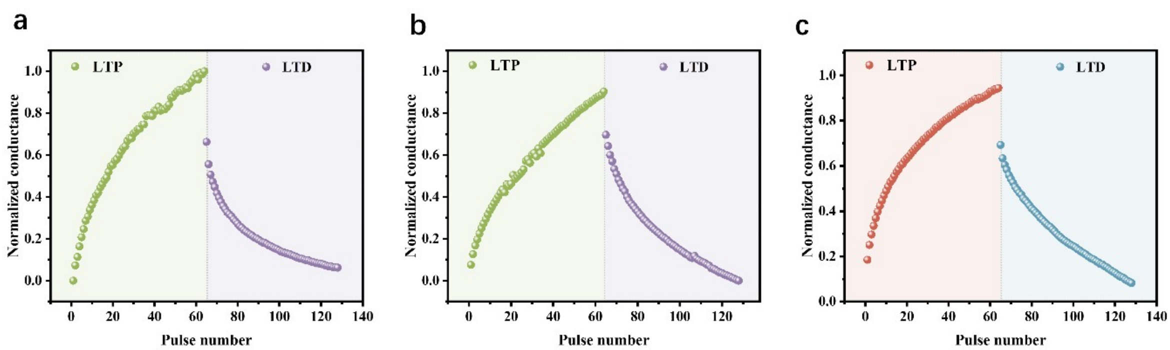

Figure S10. Changes in synaptic weights under different modulation schemes. (a) Conductance enhancement and suppression curves obtained by applying 128 gate voltage pulses, consisting of 64 negative pulses (-10 V) followed by 64 positive pulses (+15 V). The pulse width and interval are both 1 s. (b) Conductance enhancement and suppression curves obtained by applying 128 gate voltage pulses, consisting of 64 negative pulses (-10 V) followed by 64 positive pulses (increasing from +10 V to +42 V with a step of 0.5 V). The pulse width and interval are both 1 s. (c) Conductance enhancement achieved through 64 light pulses, and suppression through 64 positive pulses (increasing from +10 V to +42 V with a step of 0.5 V). Both the light pulses and voltage pulses have a width and interval of 1 s. It is evident that the highest linearity is achieved in (b).

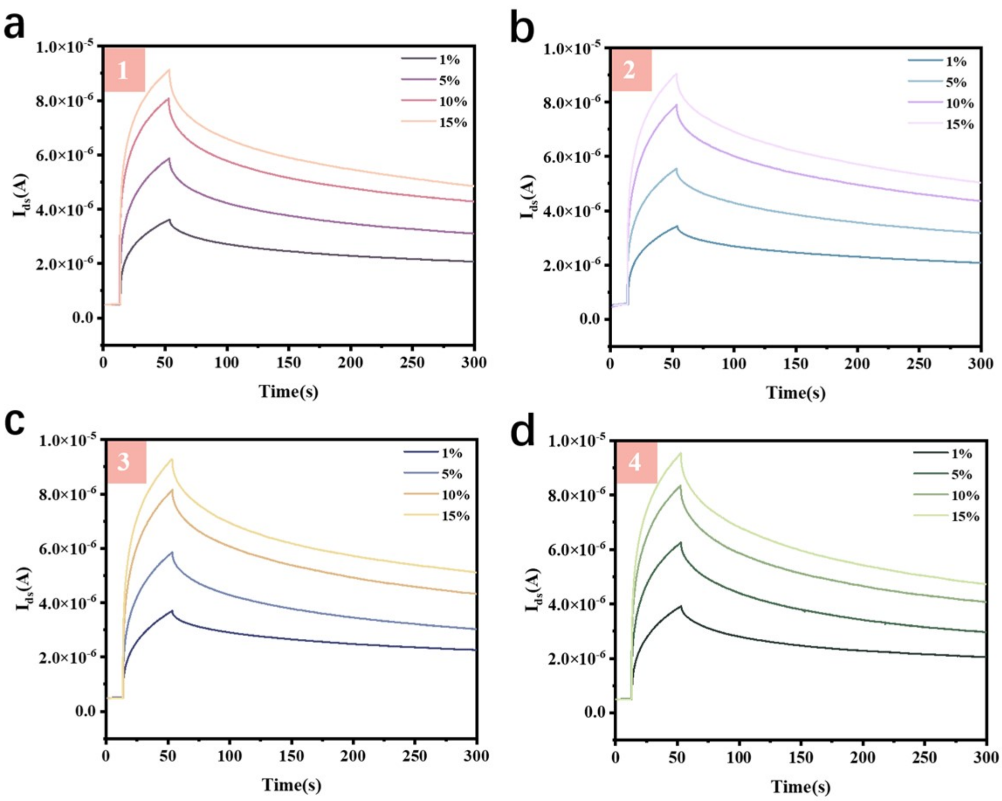

Figure S11. (a), (b), (c), and (d) show the photoresponse characteristics of the four channels of the array device at different power levels, demonstrating high similarity. This indicates that the fabricated array device exhibits stability and reproducibility.