Supporting Information

Electrically Erasable Multi-Level Charge Trapping Memory with Metal Nanoparticle Engineering for Organic Synaptic Transistors

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SUPPLEMENTARY FIGURES

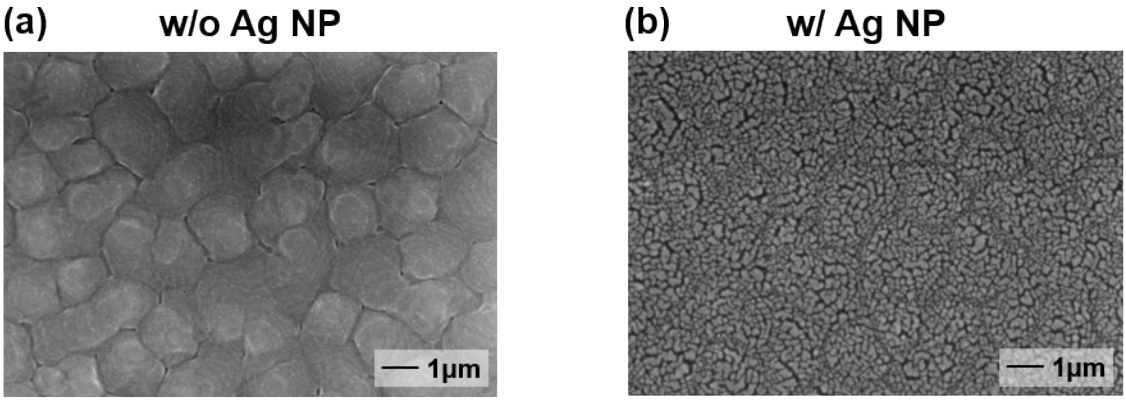

Figure S1. Scanning electron microscopy images of the surface morphology of (a) pentacene and (b) 5-nm-thick Ag NPs deposited on pentacene.

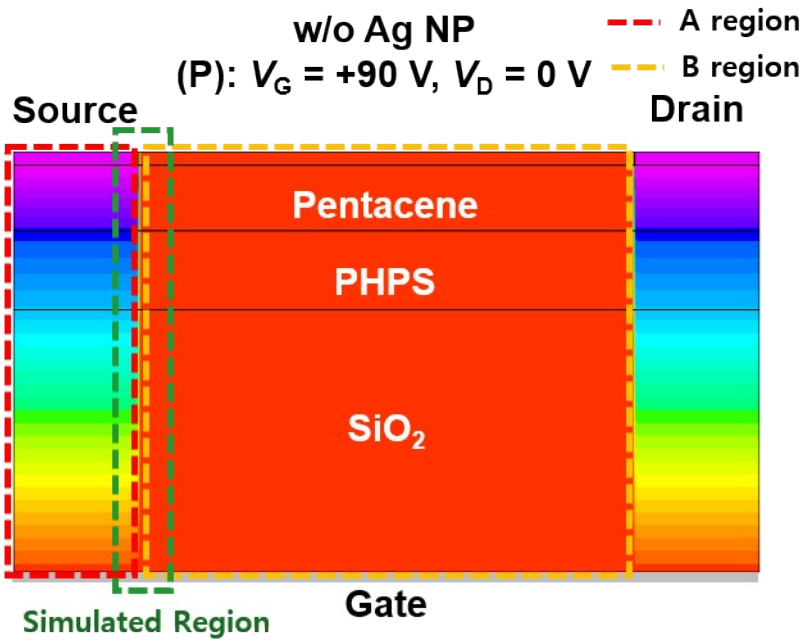

Figure S2. Numerical simulation of the electrical potential distribution of the entire device without Ag NPs under an erasing voltage ($V_{G,\,Bias}$ = +90 V). Region A indicates the region where the S/D and gate electrode overlap (red dotted line), while region B indicates the region where the gate electrode overlaps the channel without overlapping the S/D. For Fig. 2c, the simulations were performed on a portion of the source electrode and in a 200-nm-wide region near the source electrodes (green dotted box).

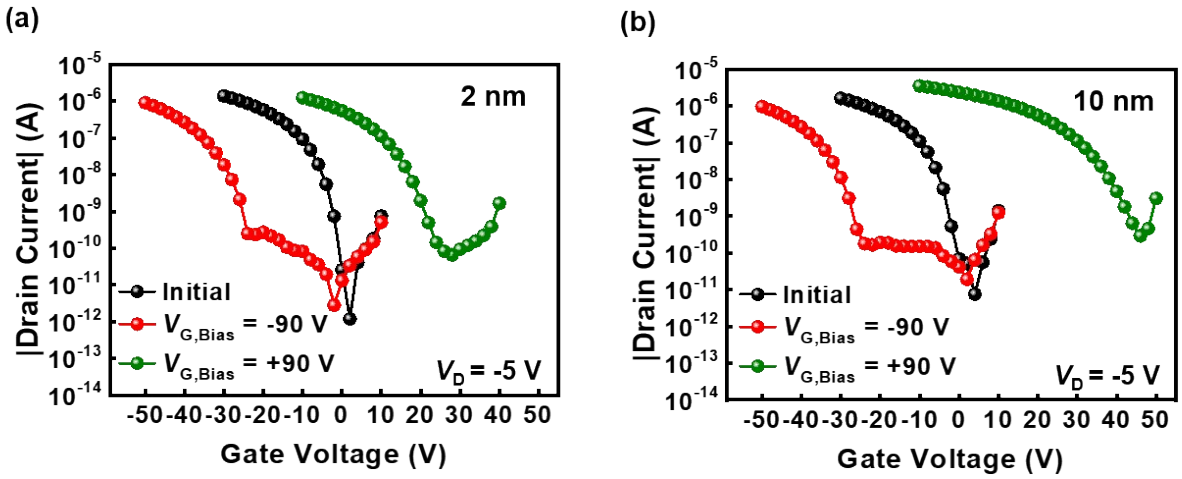

Figure S3. Transfer curves of devices incorporating (a) 2-nm- and (b) 10-nm-thick Ag NPs after the writing (red lines) and erasing (green lines) processes. The black lines represent the initial transfer curves of both devices.

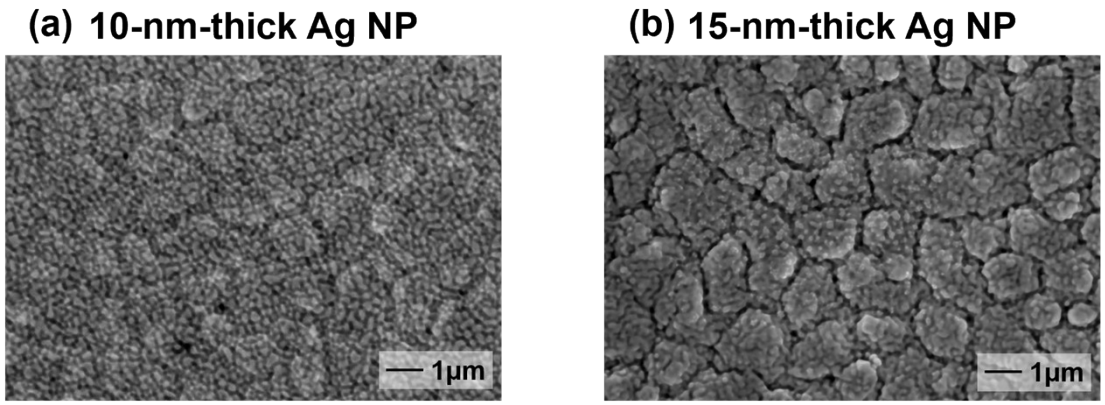

Figure S4. Scanning electron microscopy images of the surface morphology of (a) 10-nm-thick and (b) 15-nm-thick Ag NPs deposited on pentacene.

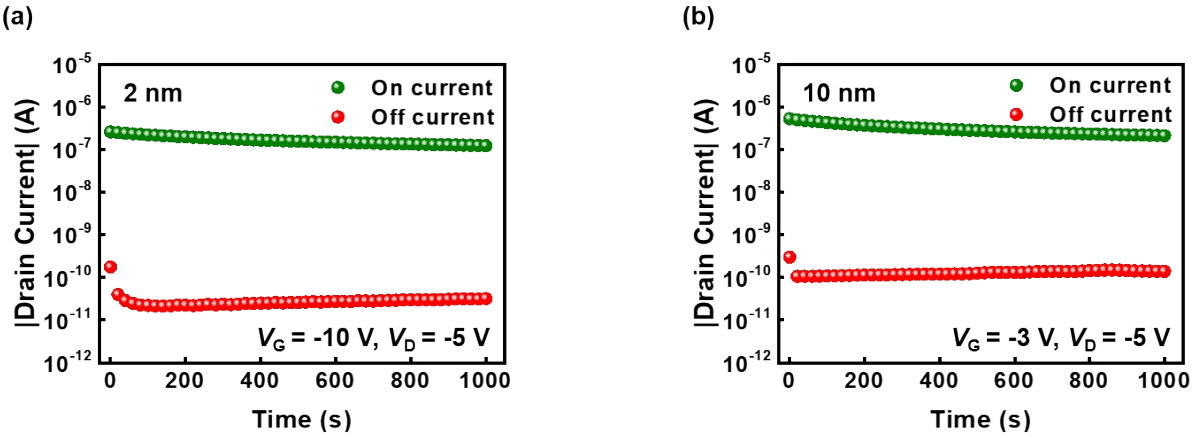

Figure S5. The retention characteristics of OSTs with (a) 2-nm and (b) 10-nm thick Ag NPs.

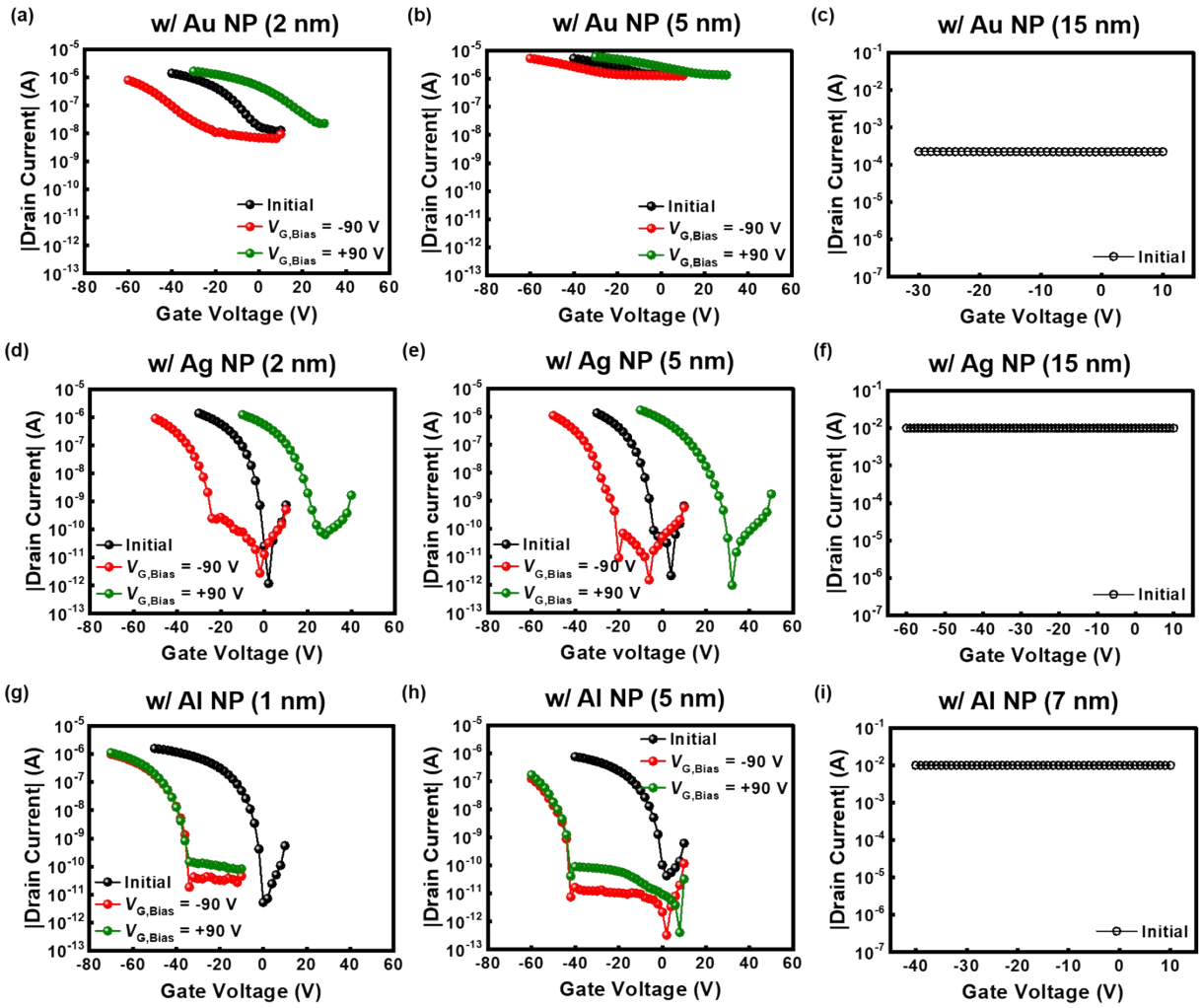

Figure S6. Electrical characteristics of NP-based OSTs with three different metal electrodes (Au, Ag, and Al) as a function of deposition thickness after the writing (depression) and erasing (potentiation) processes.

Table S1. Comparison of oligomeric synaptic transistors exhibiting potentiation/depression characteristics solely controlled by electrical pulses.

Materials (Gate/Gate insulator/ CTL[a]/ semiconductor/SD[b])	**Memory window [V]**	**Number of states (potentiation / depression)**	**Conductance ratio (G_{max}/G_{min})**	**Energy consumption [J]**	**[Ref]**
Ag/Al_2O_3/ C60/PMMA hybrid layer/ Pentacene/Au	~ 0.7	10 / 10	~ 1.2	~ 1.4×10^{-7}	[1]
Substrate/ITO/Al_2O_3/ PVPy[c]@MOF[d]/ Pentacene/Au	~ 1.5	20 / 20	~ 3	~ 0.6×10^{-7}	[2]
Si/SiO_2/ BP[e]-ZnO hybrid NP/ Pentacene/Au	~ 10	25 / 25	~ 1.4	~ 1.8×10^{-6}	[3]
Si/SiO_2/ Polyimide/ Pentacene/Au	84	-	-	-	[4][f]
Si/SiO_2/ PHPS[g]/ pentacene/Au	54 (Max 64[h])	30 /30	~ 6	~ 7.5×10^{-9}	This work

[a] CTL: charge trapping layer; [b] SD: source and drain electrodes; [c] PVPy: polyvinyl pyrrolidone; [d] MOF: metal–organic frameworks of Zn-TCPP (TCPP: tetrakis(4-carboxyphenyl)porphyrin); [e] BP: black phosphorus; [f] The demonstrated device was originally designed as a memory device rather than a synaptic transistor; therefore, data on potentiation and depression characteristics were not obtained, and energy consumption related to synaptic operation could not be evaluated; [g] PHPS: perhydropolysilazane; [h] The device with a 10-nm-thick Ag nanoparticle layer exhibited a maximum memory window of 64 V.

References

[1] Gate-Tunable Synaptic Plasticity through Controlled Polarity of Charge Trapping in Fullerene Composites, Adv. Funct. Mater. 28, 1805599 (2018)

[2] Synaptic Plasticity and Filtering Emulated in Metal–Organic Frameworks Nanosheets Based Transistors, Adv. Electron. Mater. 6, 1900978 (2020)

[3] Artificial Synapses Emulated Through a Light Mediated Organic–Inorganic Hybrid Transistor, J. Mater. Chem. C, 7, 48-59 (2019)

[4] Nonvolatile Transistor Memory Devices Using High Dielectric Constant Polyimide Electrets, J. Mater. Chem. C, 1, 3235 (2013)