Supplementary Material

Single-layer HfN_2: Symmetric Scaling Behavior in CMOS Transistors

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1. Calculation Methods

QuantumWise ATK, incorporating density-functional theory and non-equilibrium Green's function (DFT-NEGF) methods, is used to optimize the structure of SL HfN_2 and calculate the device's electron transport properties [S1, S2]. The *k*-point sampling for the HfN_2 unit cell is set to $9\times9\times1$, while that for the central scattering region and electrode regions of the HfN_2 device is set to $1\times9\times1$ and $1\times9\times160$, respectively, with a density mesh cutoff of 85 Ha. Atomic positions and energies are relaxed to less than 1×10^{-2} eV/Å and 1×10^{-5} eV, respectively. The exchange-correlation interactions are described using the Perdew-Burke-Ernzerhof (PBE) form of the generalized gradient approximation (GGA) [S3]. Transfer characteristics (I_{ds}) at various gate voltages (V_g) are calculated under a bias voltage of V_b = 0.64 V using the Landauer-Büttiker formalism [S4]:

$$I_{ds}(V_b,V_g)=\frac{2e}{h}\int_{-\infty}^{+\infty}\{T(E,V_b,V_g)\,[f_S(E-\mu_S)-f_D(E-\mu_D)]\}dE. \quad \text{(S1)}$$

where $T(E, V_b, V_g)$ is the transmission coefficient; f_S(f_D) and μ_S(μ_D) are the Fermi-Dirac distribution functions and electrochemical potentials of the source (drain) regions, respectively.

The key quality factors (KQF) for CMOS transistors include ON-state current (I_{on}), transconductance (g_m), subthreshold swing (SS), delay time (τ), power-delay product (PDP), and total capacitance (C_g). According to the 2013 ITRS criteria for sub-5-nm-L_g FETs, the required I_{on} for high-performance (HP) and low-power (LP) applications is ≥ 900 μA/μm and 295 μA/μm, respectively,

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while the OFF-state current (I_{off}) should be $\leq 0.1\ \mu A/\mu m$ for HP and $\leq 5\times10^{-5}\ \mu A/\mu m$ for LP [S5]. The g_m and SS denote the gate control capability of CMOS transistors in the superthreshold and subthreshold regions, respectively. Moreover, the τ, PDP, and C_g describe the switching time, power dissipation, and total capacitance, respectively, derived from the following equations:

$$g_m = \frac{dI_{ds}}{dV_g}. \tag{S2}$$

$$SS = \frac{\partial V_g}{\partial\, log(I_{ds})}. \tag{S3}$$

$$\tau = \frac{C_g V_{ds}}{I_{on}}. \tag{S4}$$

$$PDP = C_g V_{ds}^2 = V_{ds} I_{on} \tau. \tag{S5}$$

$$C_g = \frac{3\partial Q_{ch}}{\partial V_g}. \tag{S6}$$

In these equations, Q_{ch} denotes the total charge in the channel. The drain-source voltage is fixed at $V_{ds} = V_b = 0.64$ V.

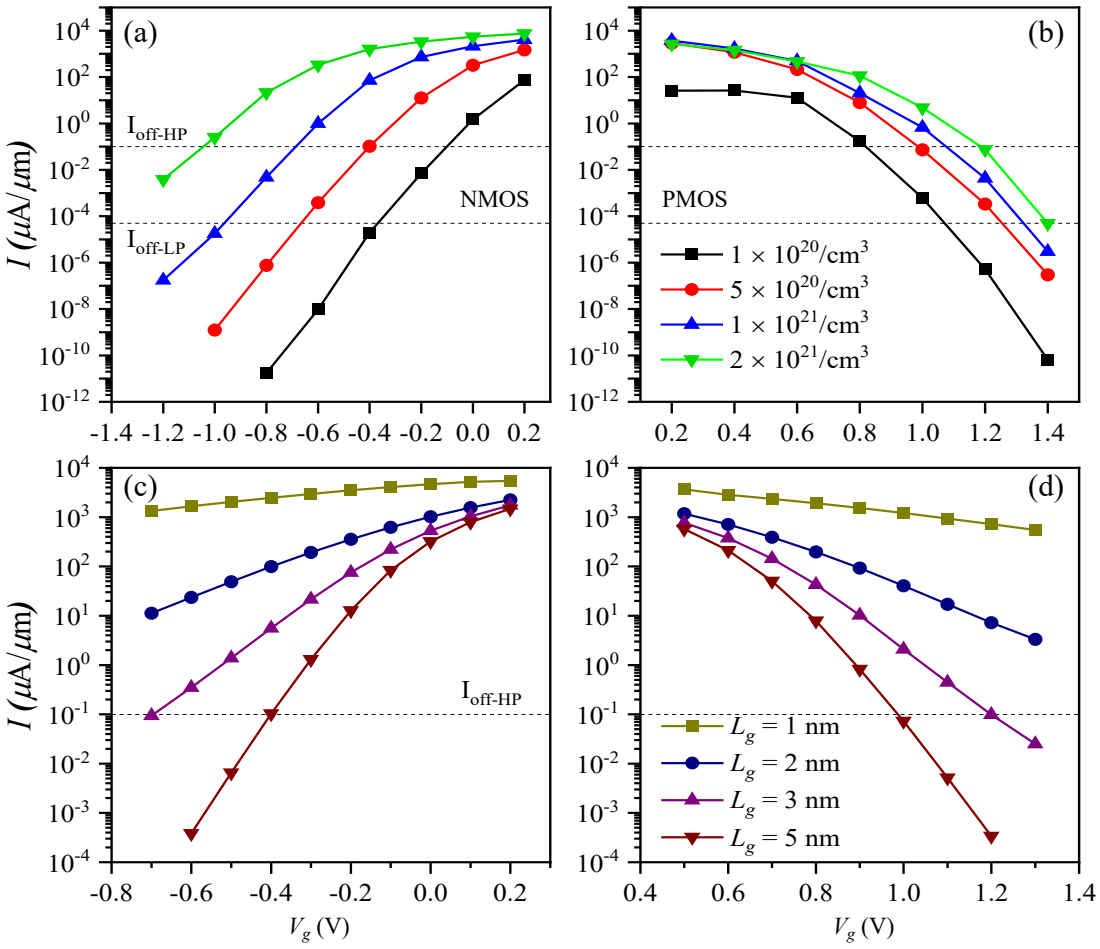

Figure S1. *I-V*$_g$ curves for L_g = 5 nm (a) NMOS and (b) PMOS without L_{UL} at four doping

concentrations. I-V_g curves for L_g = 5–1 nm (c) NMOS and (d) PMOS without L_{UL}, with $N_{e/h}$ = 5× 10^{20} cm^{-3}. $I_{off\text{-}HP}$ and $I_{off\text{-}LP}$ represent the OFF-state currents for ITRS-HP and -LP, respectively.

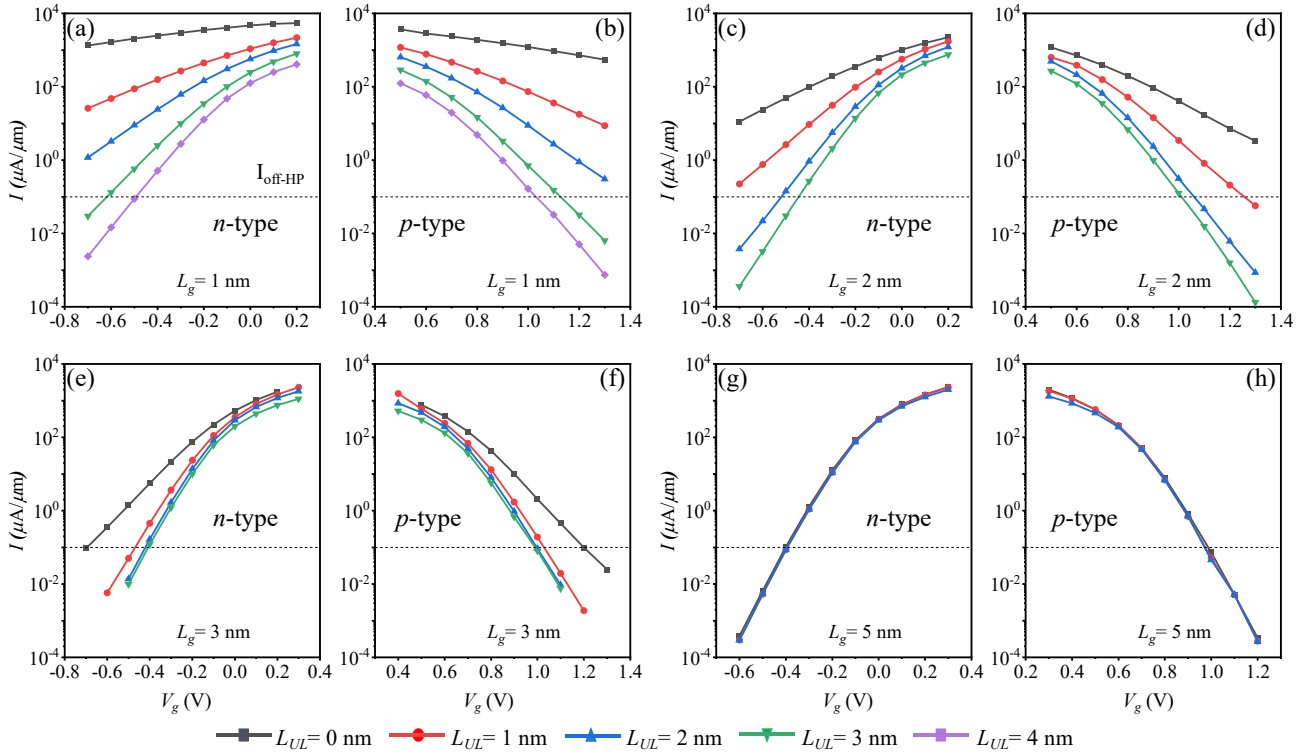

Figure S2. (a–h) $I-V_g$ characteristics of SL HfN_2 NMOS and PMOS transistors with different L_g and L_{UL} lengths.

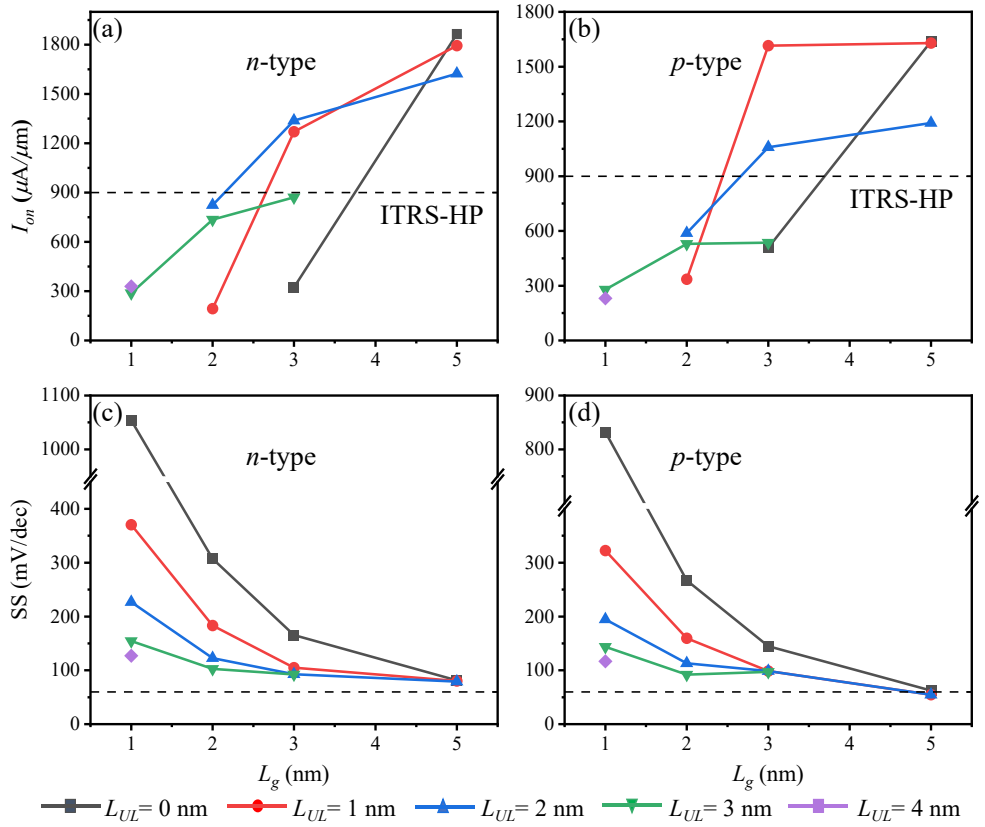

Figure S3. I_{on} as a function of L_g for SL HfN_2 NMOS (a) and PMOS (b) transistors with different L_{UL} for the HP application. Variation of SS with L_g for NMOS (c) and PMOS (d) with different L_{UL}.

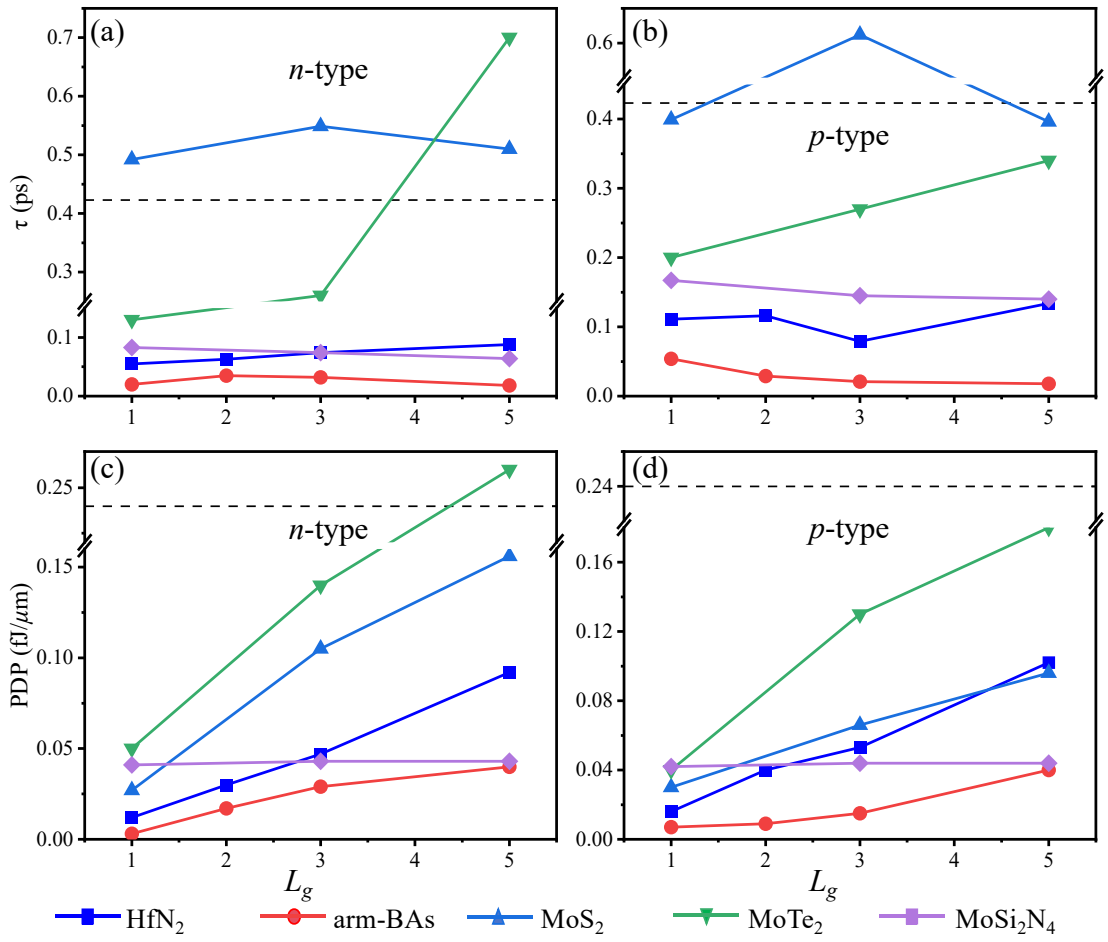

Figure S4. Comparison of optimal τ and PDP for SL HfN_2 transistors at sub-5-nm-L_g scales with reported armchair-BAs, MoS_2, $MoTe_2$, and $MoSi_2N_4$ transistors [Ref. 21-23, 40 in main text]. (a) and (c) show NMOS devices, while (b) and (d) depict PMOS devices. The dashed lines represent the ITRS-HP standard.

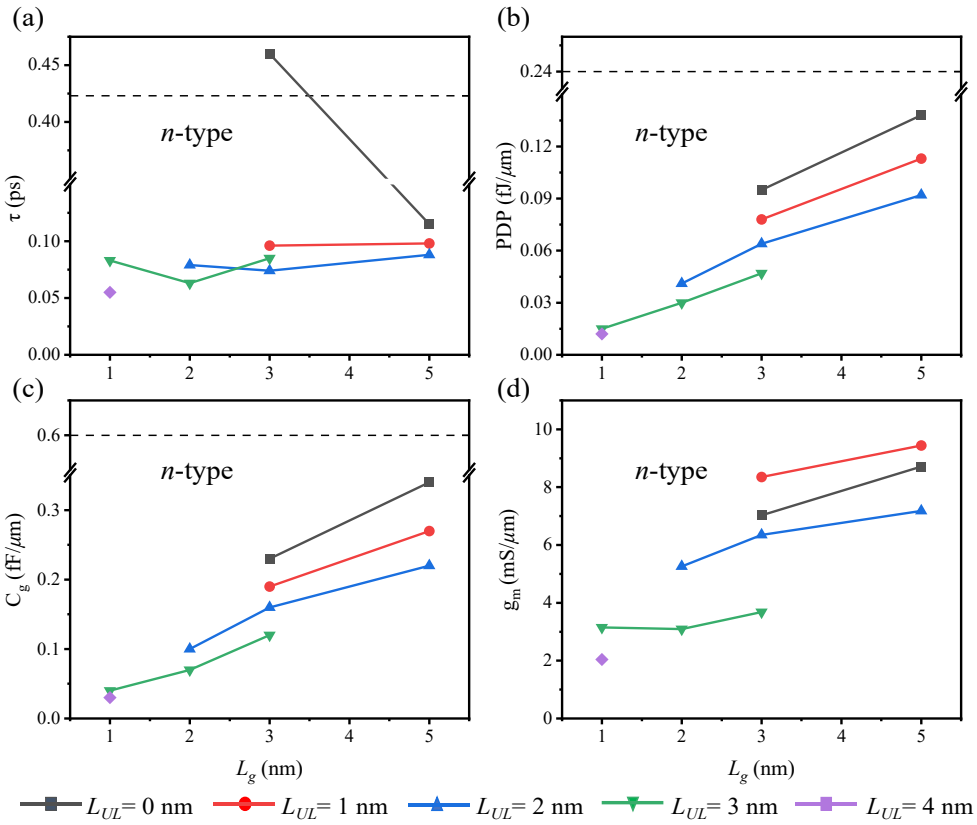

Figure S5. Variation of τ (a), PDP (b), C_g (c), and g_m (d) with L_g for SL HfN_2 NMOS devices with L_{UL} = 0–4 nm. The black dotted lines indicate the ITRS-HP application.

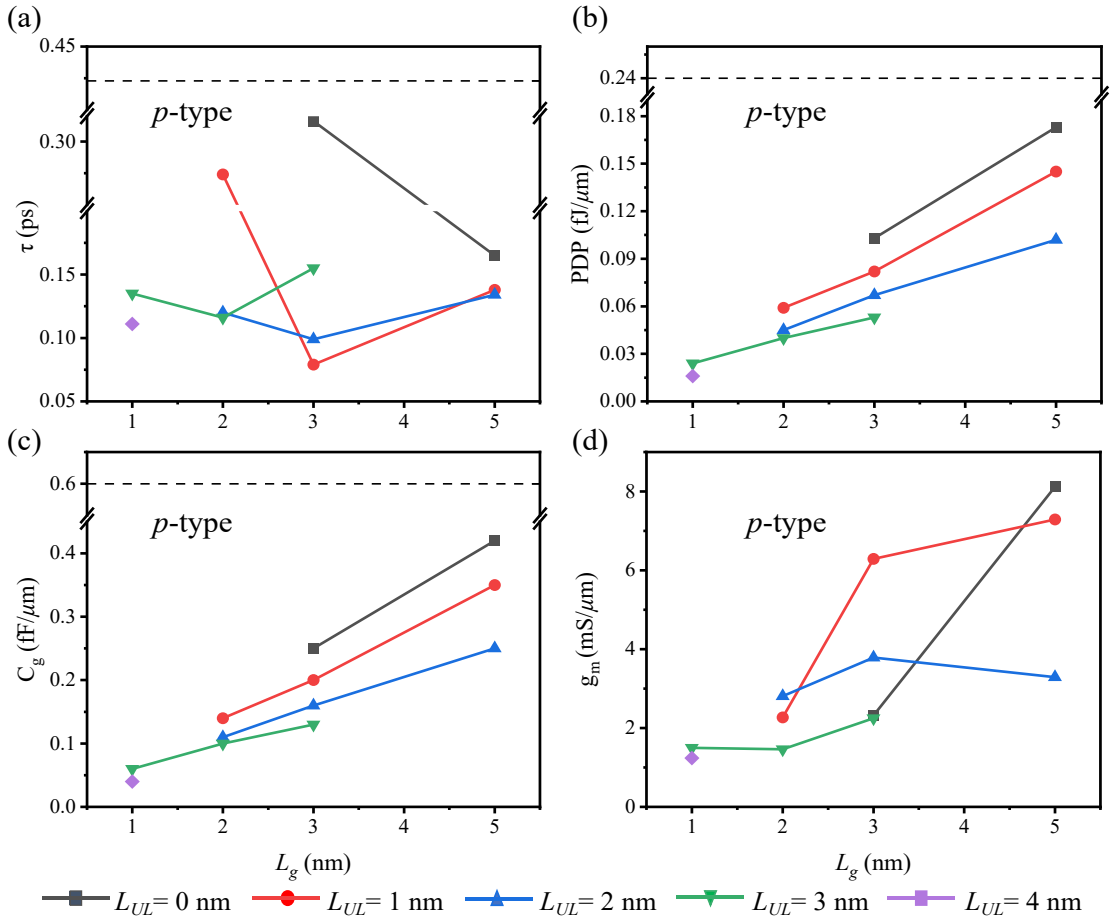

Figure S6. Variation of τ (a), PDP (b), C_g (c), and g_m (d) with L_g for SL HfN_2 PMOS devices with L_{UL} = 0–4 nm. The black dotted lines indicate the ITRS-HP application.

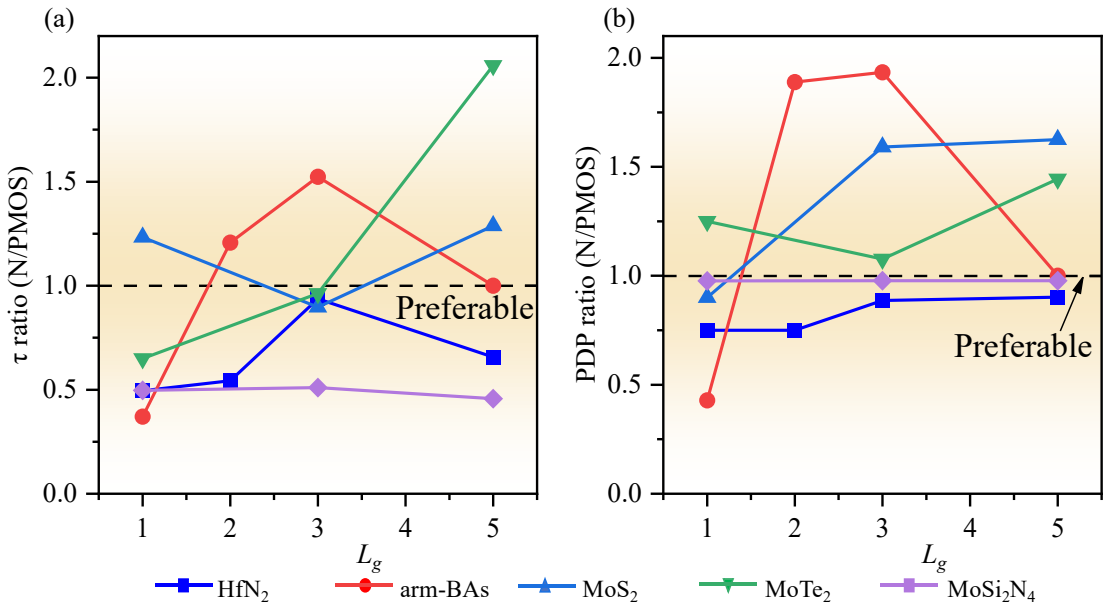

Figure S7. The ratio of τ (a) and PDP (b) between the NMOS and PMOS with the same channel material, including the SL HfN_2, armchair-BAs, MoS_2, $MoTe_2$, and $MoSi_2N_4$.

Table S1. Benchmark of the ballistic performance limits of the sub-5-nm-L_g SL HfN_2 NMOS against the ITRS requirements for HP applications in 2028 (2013 version). The doping density of the left and right electrodes is 5×10^{20} cm^{-3}.

	L_g (nm)	L_{UL} (nm)	SS (mV/dec)	I_{on} (μA/μm)	I_{on}/I_{off}	C_g (fF/μm)	τ (ps)	PDP (fJ/μm)	g_m (mS/μm)
n-type	1	0	1053.87						
		1	370.40						
		2	226.72						
		3	154.39	288.24	2.88×10^3	0.04	0.083	0.015	3.15
		4	127.10	329.41	3.29×10^3	0.03	0.055	0.012	2.04
	2	0	307.23						
		1	183.14						
		2	122.61	823.53	8.24×10^3	0.10	0.079	0.041	5.26
		3	102.60	735.29	7.35×10^3	0.07	0.063	0.030	3.09
	3	0	165.49	323.53	3.24×10^3	0.23	0.460	0.095	7.03
		1	104.93	1270.59	1.27×10^4	0.19	0.096	0.078	8.35
		2	92.75	1338.24	1.34×10^4	0.16	0.074	0.064	6.35
		3	92.27	870.59	8.71×10^3	0.12	0.085	0.047	3.68
	5	0	81.21	1864.71	1.86×10^4	0.34	0.115	0.138	8.71
		1	80.01	1794.12	1.79×10^4	0.27	0.098	0.113	9.44
		2	78.94	1623.53	1.62×10^4	0.22	0.088	0.092	7.18
ITRS-HP	5.1			900	9.00×10^3	0.60	0.423	0.240	
IRDS-HP	12		70	851	8.51×10^4	0.37	0.840	0.470	1.75

Table S2. Benchmark of the ballistic performance limits of the sub-5-nm-L_g SL HfN_2 PMOS against the ITRS requirements for HP applications in 2028 (2013 version). The doping density of the left and right electrodes is 5×10^{20} cm^{-3}.

	L_g (nm)	L_{UL} (nm)	SS (mV/dec)	I_{on} (μA/μm)	I_{on}/I_{off}	C_g (fF/μm)	τ (ps)	PDP (fJ/μm)	g_m (mS/μm)
p-type	1	0	832.15						
		1	322.46						
		2	194.53						
		3	143.60	279.12	2.79×10^3	0.06	0.135	0.024	1.50
		4	116.78	231.18	2.31×10^3	0.04	0.111	0.016	1.24
	2	0	266.91						
		1	159.53	335.29	3.35×10^3	0.14	0.274	0.059	2.27
		2	113.18	588.24	5.88×10^3	0.11	0.120	0.045	2.81
		3	92.05	529.41	5.29×10^3	0.10	0.116	0.040	1.46
	3	0	144.63	508.82	5.09×10^3	0.25	0.316	0.103	2.32
		1	98.49	1614.71	1.61×10^4	0.20	0.079	0.082	6.29
		2	98.61	1058.82	1.06×10^4	0.16	0.099	0.067	3.79
		3	97.25	535.29	5.35×10^3	0.13	0.155	0.053	2.25
	5	0	62.31	1638.24	1.64×10^4	0.42	0.165	0.173	8.12
		1	54.68	1629.41	1.63×10^4	0.35	0.138	0.145	7.29
		2	54.52	1191.18	1.19×10^4	0.25	0.134	0.102	3.29
ITRS-HP	5.1			900	9.00×10^3	0.60	0.423	0.240	
IRDS-HP	12		70	851	8.51×10^4	0.37	0.840	0.470	1.75

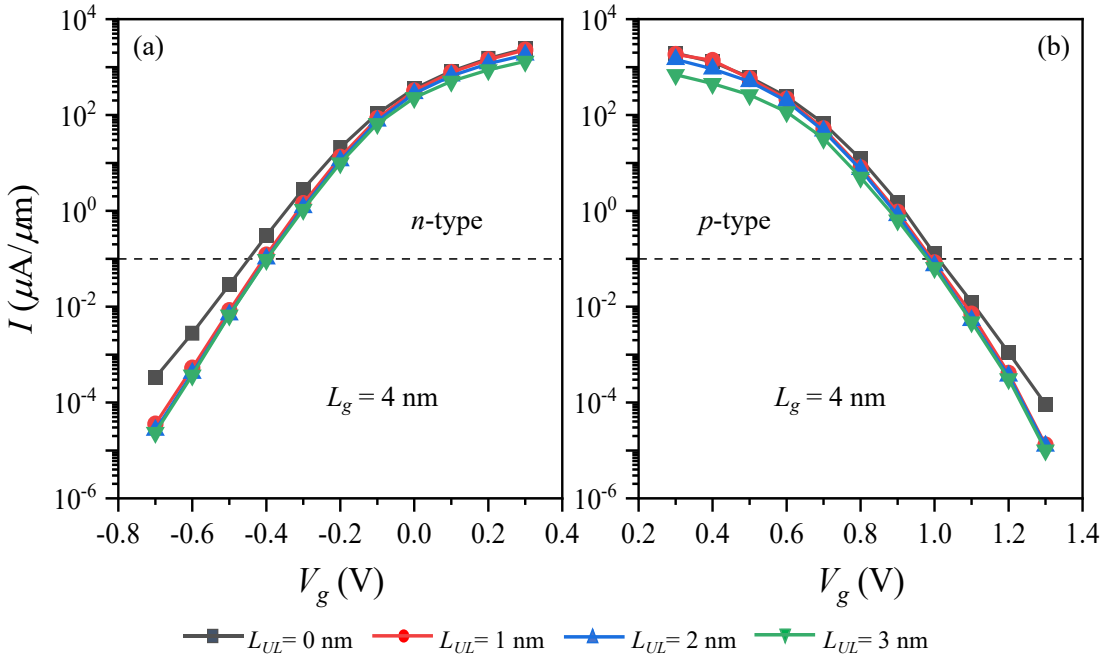

Figure S8. I-V_g curves for SL HfN_2 NMOS and PMOS devices at L_g = 4 nm and L_{UL} = 0-3 nm.

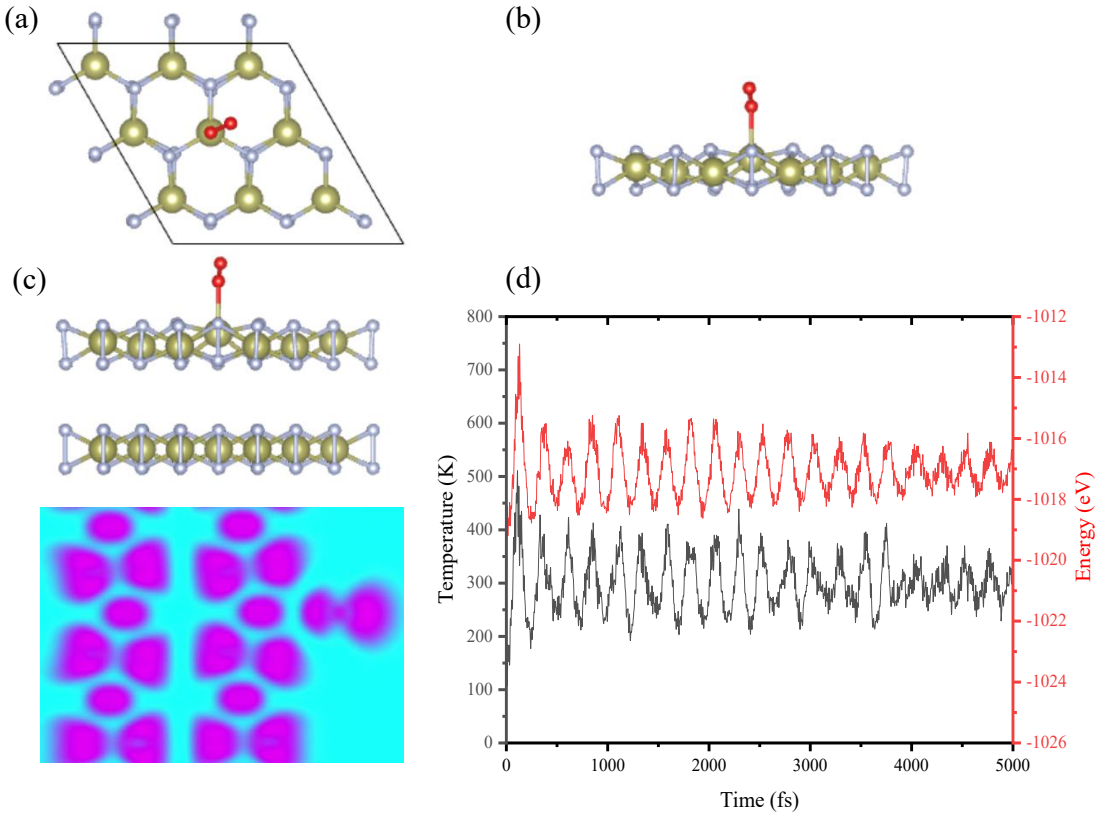

Figure S9. (a) Top view and (b) side view of a single O_2 molecule adsorbed at the top site of the HfN_2 surface. (c) Interfacial model of the HfN_2/native oxide heterostructure and corresponding electron localization function. (d) AIMD simulation of the total energy of 6 × 6 HfN_2 supercells as a function of step size at 300 K.

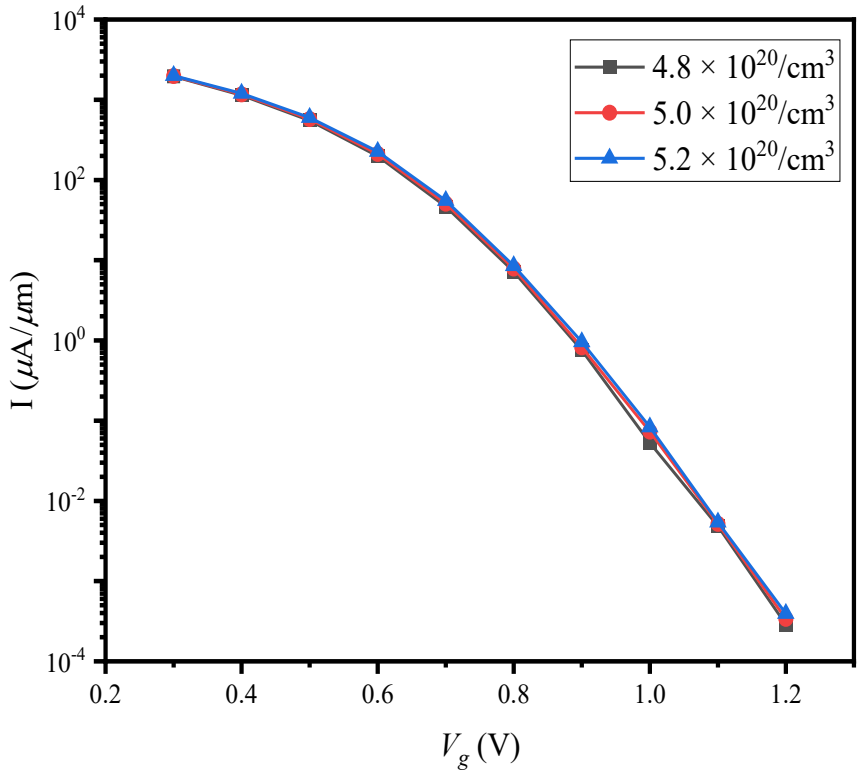

Figure S10. I–V characteristics of HfN_2 PMOS devices under three different doping concentrations: 4.8×10^{20}, 5.0×10^{20}, and 5.2×10^{20} cm^{-3}.

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