Supporting Information

Arbitrary-Ordered Pulsed Programming Achieving 11 Well-Separated Programming Levels via a Multilevel Transistor–Memristor Series Configuration

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KEYWORDS: Memristor, Multilevel resistive switching, Retention, endurance, Transistor–memristor configuration

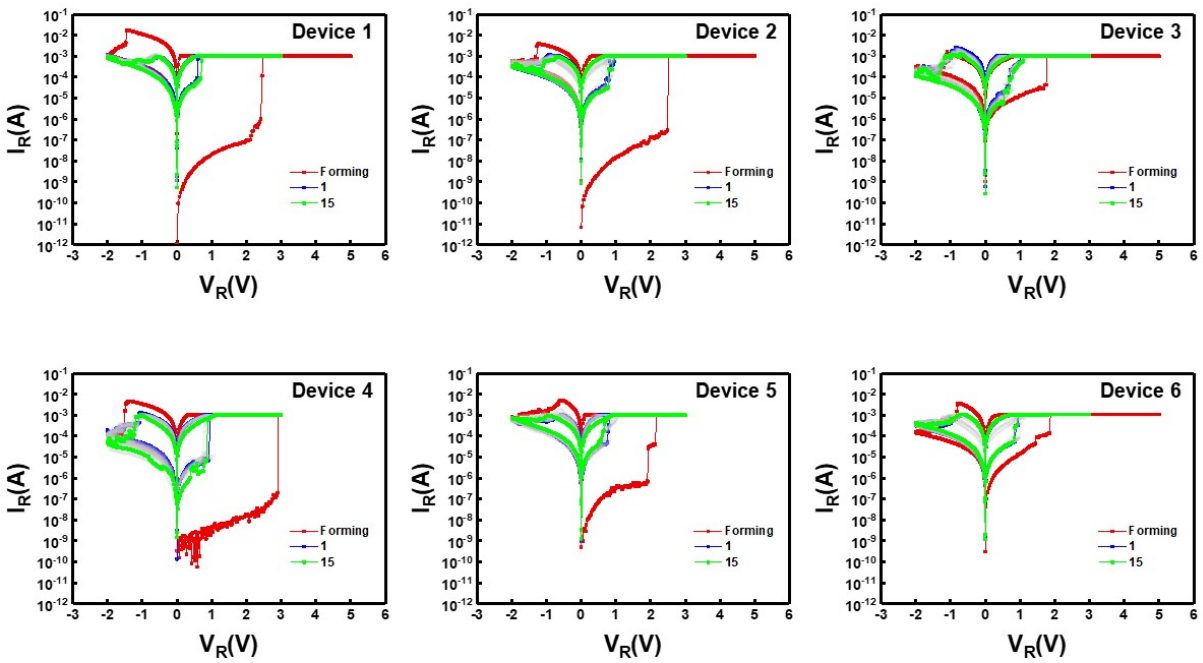

Figure S1. Device-to-device (D2D) I–V characteristics of Pt/Ta/ZrO_x/Pt memristors (Device 1 to Device 6). Each cell underwent a forming process followed by 15 consecutive switching cycles. The consistent bipolar switching behavior and stable current levels confirm good D2D uniformity and operational reliability.

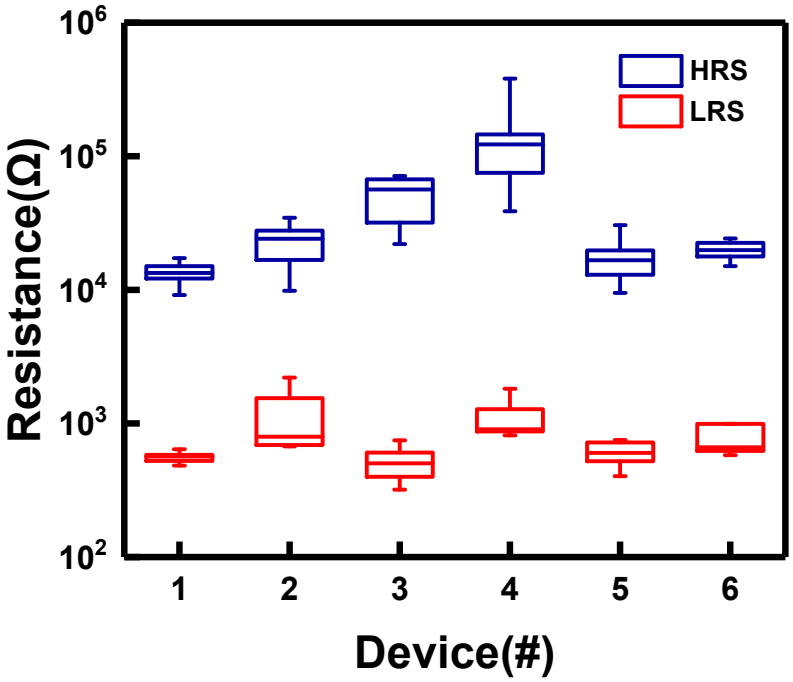

Figure S2. Box plots of HRS and LRS distributions across six devices, each measured over 15 switching cycles. The results reflect reasonable device-to-device variation and switching stability, supporting the reproducibility shown in Supplementary Figure S1.

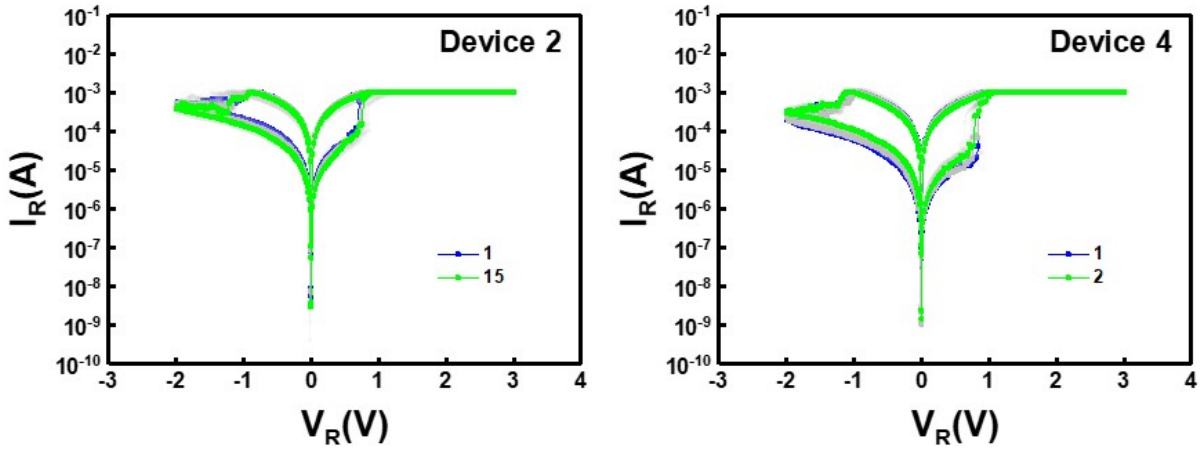

Figure S3. I–V characteristics of Device 2 and Device 4 remeasured after 50 days, showing stable resistive switching over 15 cycles. The preserved switching functionality confirms excellent environmental stability and long-term operational reliability of the devices.

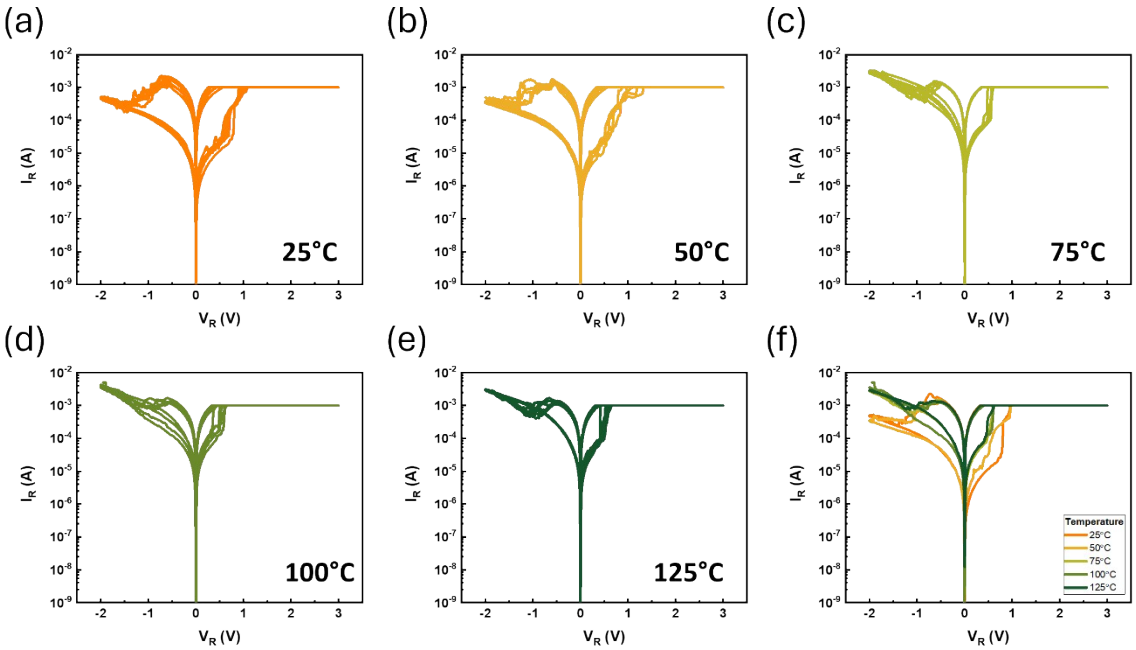

Figure S4. (a-e) Temperature-dependent I–V characteristics of the memristor measured at 25 °C, 50 °C, 75 °C, 100 °C and 125 °C under a fixed compliance current of 1 mA. (f) Overlap of representative I–V characteristics measured at 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C.

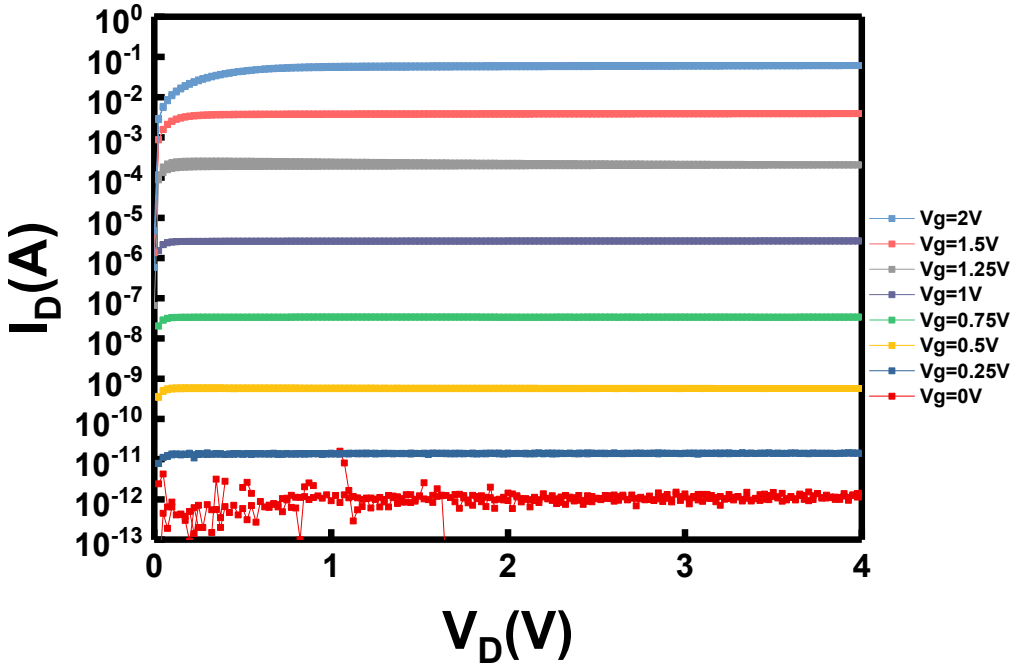

Figure S5. Transfer characteristics of the commercial NMOS transistor (2N7000). (a) Output curves under different V_g levels demonstrate well-controlled saturation current. This V_g-tunable current-limiting behavior enables the transistor to serve as an effective current compliance (CC) component during the SET process.

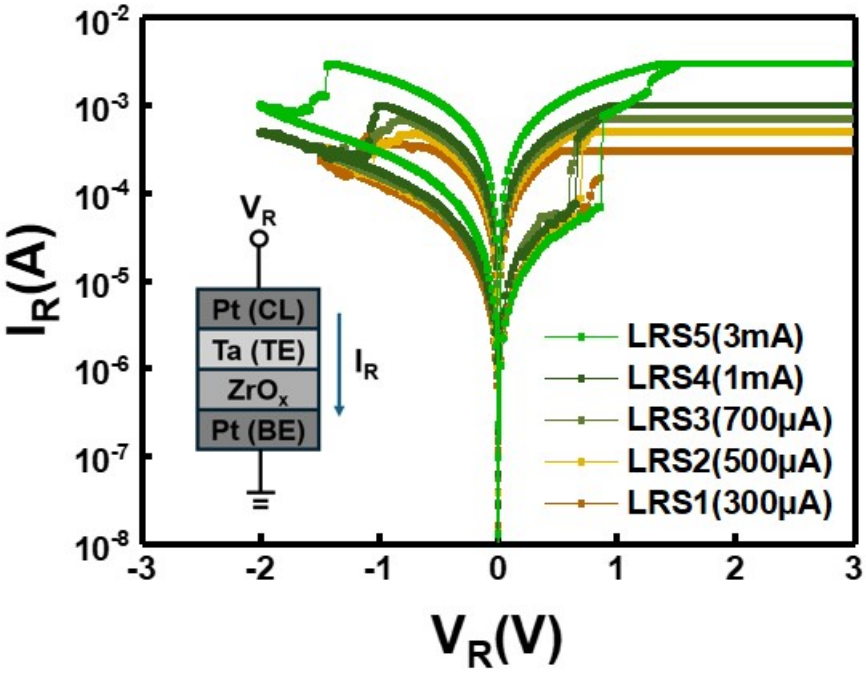

Figure S6. DC sweep curves of multilevel resistance states measured from a single memristor device under direct compliance current control. The linearity is highly consistent with that observed in the transistor–memristor series configuration, confirming that the current-limiting function does not distort intrinsic device behavior.

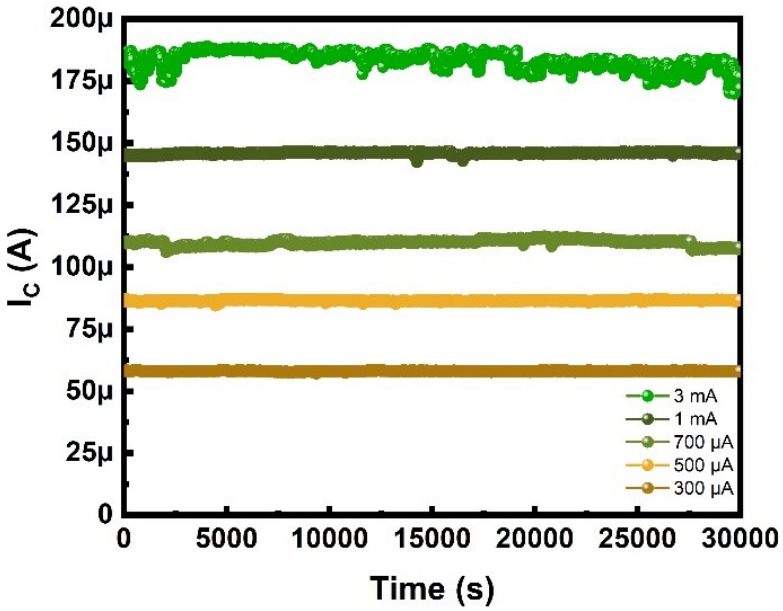

Figure S7. Retention performance of LRS1–LRS5 states measured on a single memristor at a read voltage of 0.1 V under 85 °C for 30,000 s, showing stable current without noticeable degradation, confirming excellent thermal stability and data retention capability.

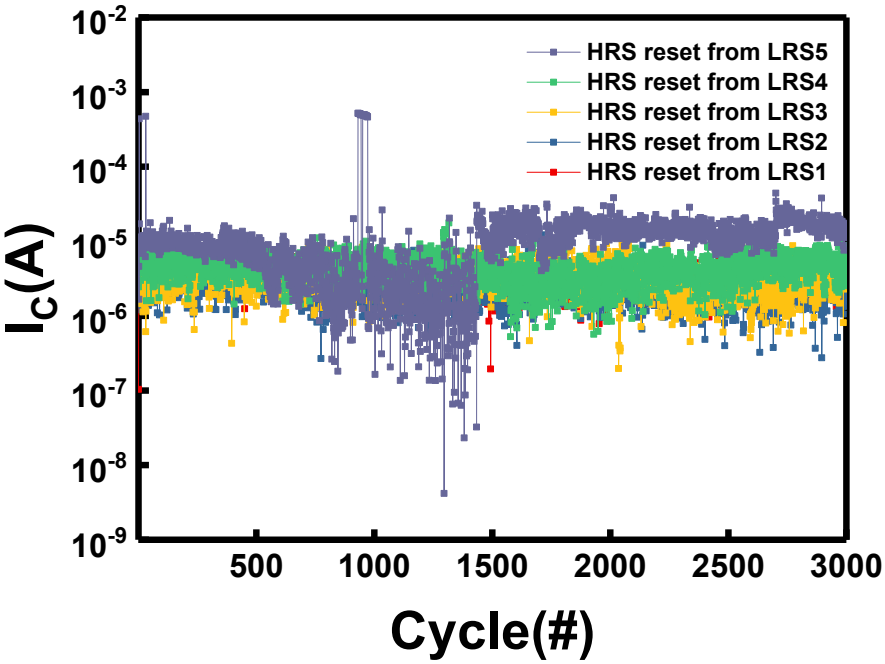

Figure S8. Endurance characteristics of HRS obtained from different initial LRS states (LRS1 to LRS5). The results demonstrate that the reset process consistently leads to a stable HRS, regardless of the preceding LRS, confirming the device's immunity to prior state history and its reliable switching repeatability.

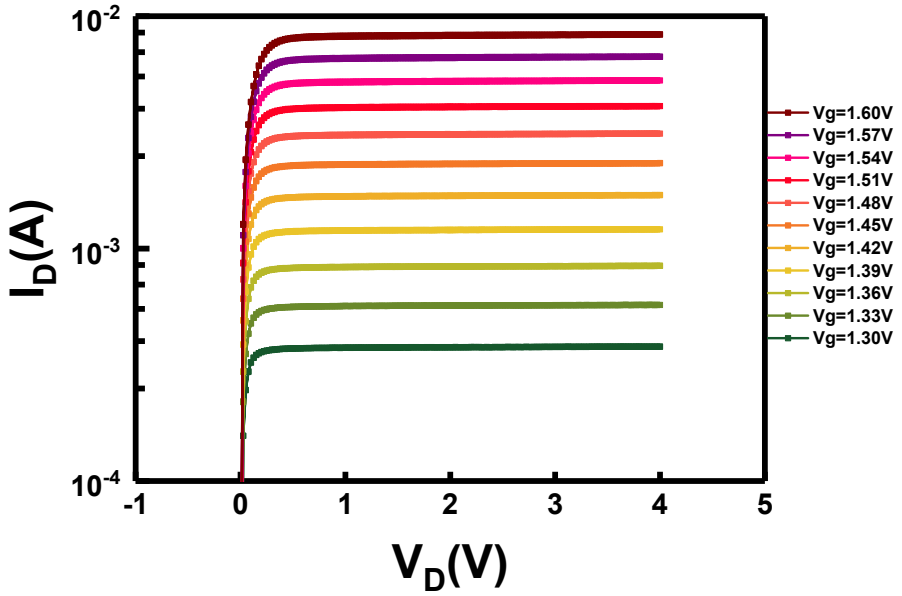

Figure S9. I_DV_D characteristics of the 2N7000 transistor measured under gradually increased gate voltages (V_g = 1.30 to 1.60 V), corresponding to programmed level 1 to 11, showing distinct and well-separated current levels.

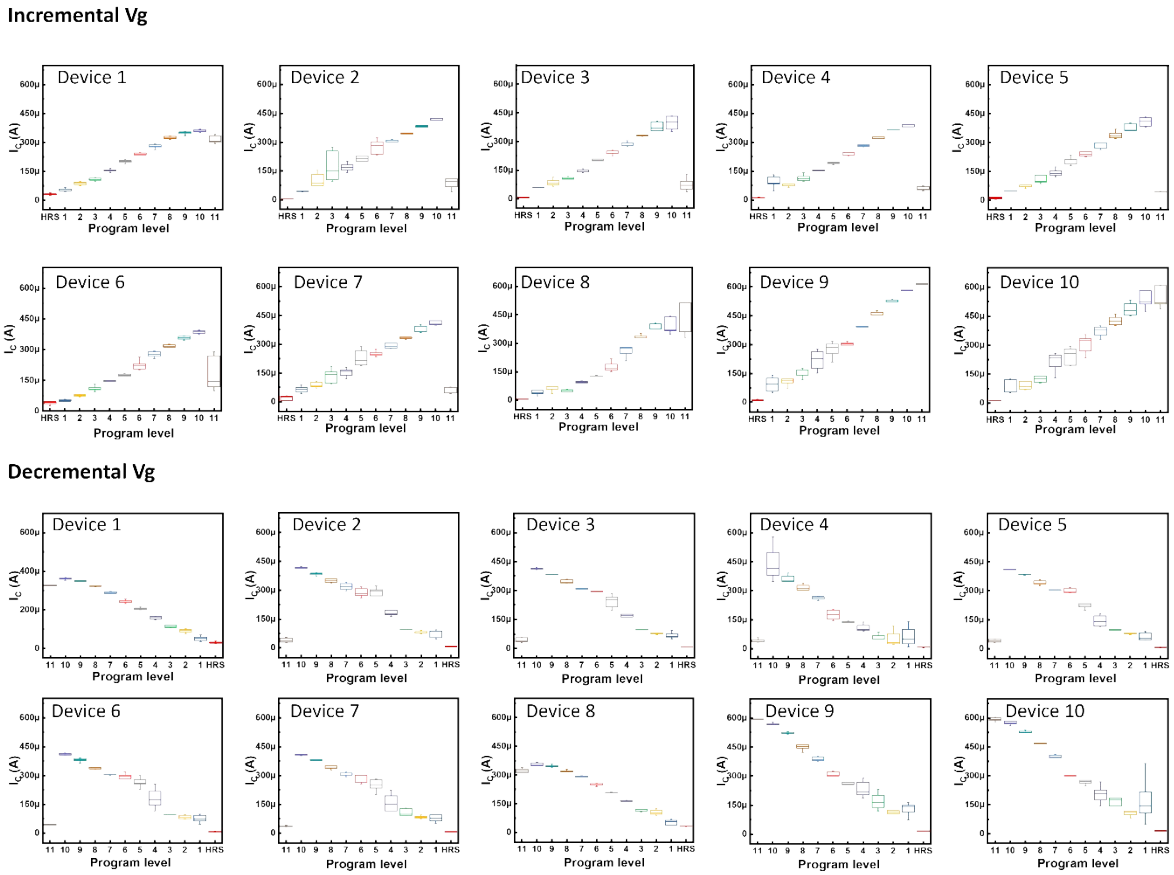

Figure S10. Statistical analysis of device-to-device (D2D) uniformity for 11 programmable levels measured from ten devices fabricated under identical conditions.

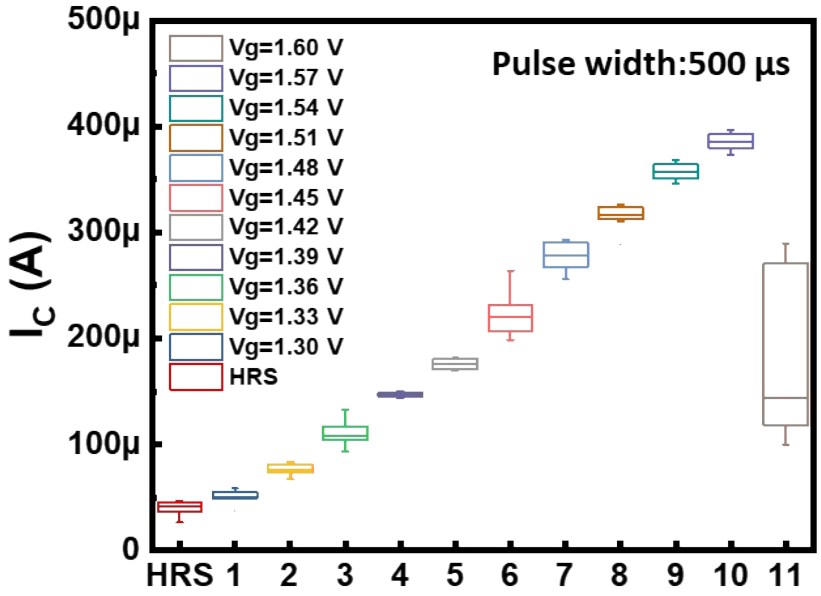

Figure S11. Box plot of read current distributions for 11 programmable levels obtained under a 500 µs pulse width. The results show ten well-defined low-resistance states and one high-resistance state (HRS).

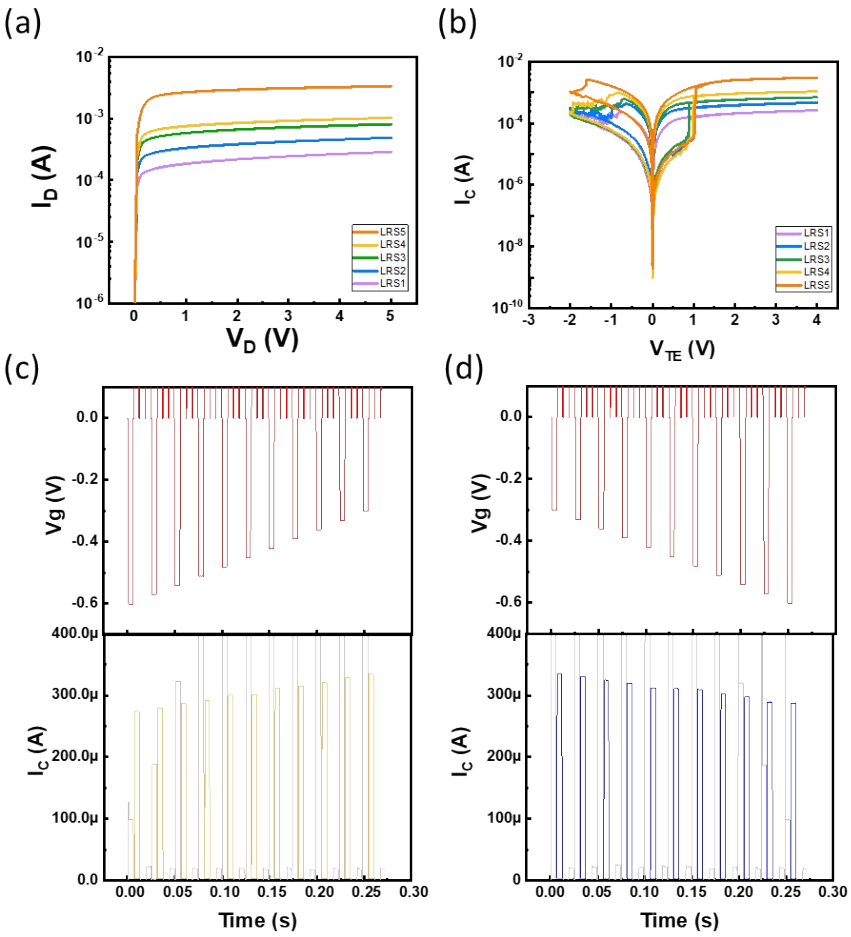

Figure S12. Validation of multilevel operation robustness using a commercial transistor (2SK170). (a) I_D-V_D characteristics of the 2SK170 transistor measured under gradually increased gate voltages (Vg = -0.3 V, -0.46 V, -0.48 V, -0.53 V and -0.55 V), corresponding to programmed LRS1 to LRS5, showing distinct and well-separated current levels. (b) Multilevel resistance states (LRS) are achieved by varying the Vg of a series-connected 2N7000 transistor. The applied Vg are -0.3 V, -0.46 V, -0.48 V, -0.53 V and -0.55 V. (c, d) Incremental (−0.6 → −0.3 V) and decremental (−0.3→−0.6 V) Vg programming schemes and their corresponding experimental results, showing the current responses I_C during programming and corresponding statistical distributions of the read currents for each level.

Table S1 HRS Current read at -0.1 V corresponding to different LRS states

State	HRS current@-0.1 V
LRS5 (3mA)	7.34E-06 A
LRS4 (1mA)	2.53E-06 A
LRS3 (700 µA)	5.28E-06 A
LRS2 (500 µA)	6.00E-06 A
LRS1 (300 µA)	3.46E-06 A

Table S2 Comparison of Transistor–Memristor Architectures for Multistate and V_g Programming

Device structure (T+R)	Number of States	Retention	Endurance	V_g pulse programing	Bidirectional Multistate	Ref.
2N(7000)+ Pt/Ta/ZrO_x/Pt	8	> 10000 s (25 °C)	>3000	✓	✓	This work
NMOS+ Ta/TaO_x/Pt	6	-	$>10^6$	✓	×	【1】
ITO/SiN/TaN (Only R)	8	> 10000 s (25 °C)	>1000	-	✓	【2】
NMOS+ Ti/HfO_2/TiN	6	> 10000 s (125 °C)	$>5x10^5$	×	×	【3】
CMOS+ TiN/Ti/HfO_2/TiN	9	-	10	×	×	【4】
NMOS+ TiN/Ti/HfO_2/TiN	9	-	-	✓	×	【5】

Reference:

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