

Supporting Information

Ultrathin Sub-5nm Gate-All-Around SiGe Nanowire Transistors with Near-Ideal Subthreshold Swing

Guowei Zhang^a, Yuang Guan^a, Yee Sin Ang^b, Shibo Fang^b, Xiaoyi Lei^a, Jinchang Liu^a, Cong Shao^a, Yang Dai^a, Wu Zhao^a, Junfeng Yan^a, Jing Lu^{c*} and Han Zhang^{a*}

^a School of Information Science and Technology, Northwest University, Xi'an 710127, P. R. China.

^b Science, Mathematics and Technology (SMT) Cluster, Singapore University of Technology and Design, 487372, Singapore.

^c State Key Laboratory for Mesoscopic Physics and Department of Physics, Peking University, Beijing 100871, P. R. China.

*Corresponding author: Han Zhang (hanzhang@nwu.edu.cn)

Jing Lu (jinglu@pku.edu.cn)

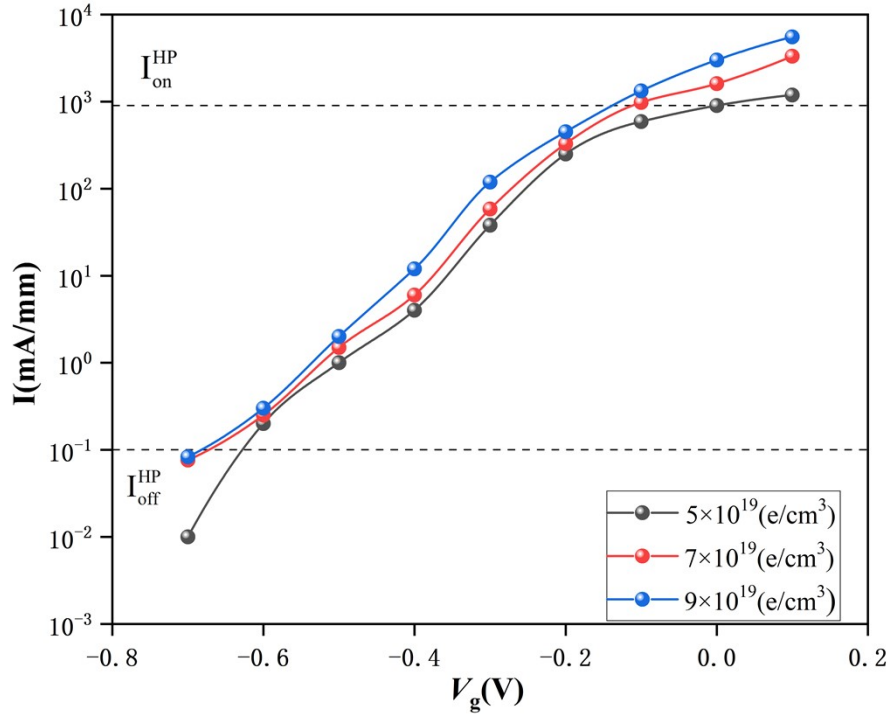


Figure S1. Transfer characteristics of the *n*-type GAA SiGe NW FETs with different electron doping concentrations (5×10^{19} , 7×10^{19} , and 9×10^{19} e/cm^3).

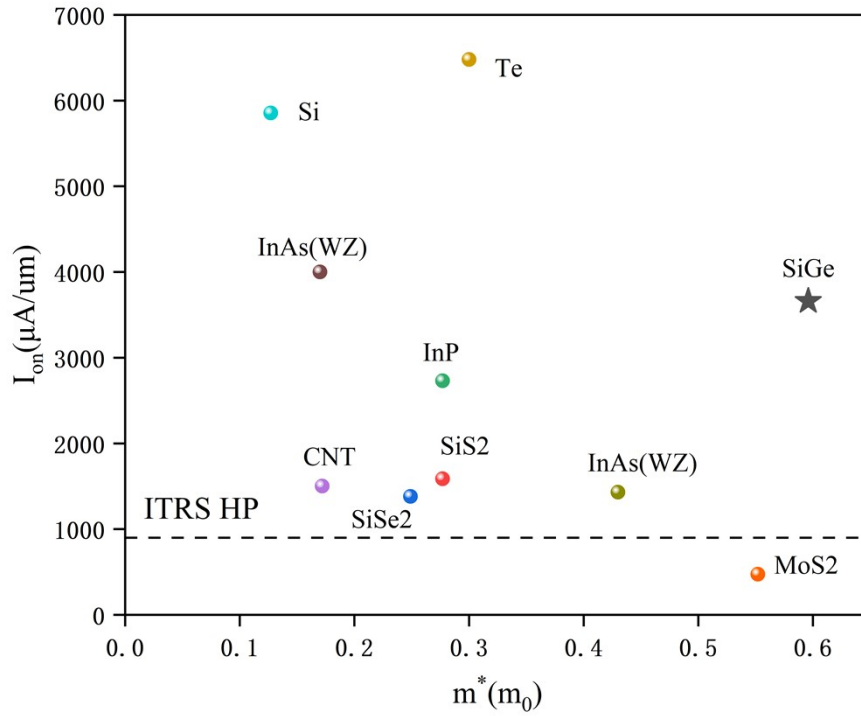


Figure S2. HP I_{on} of the low-dimensional material FETs at $L_g = 5\text{nm}$ against m^* of the low-dimensional material.

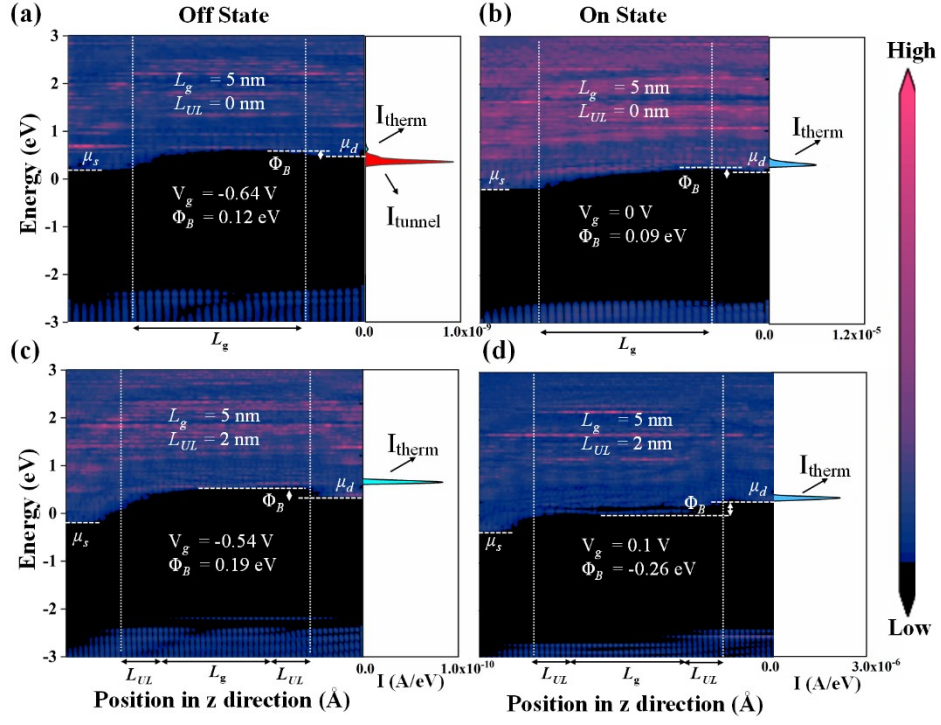


Figure S3. (a-d) Resolved LDDOS and the spectral current in the channel region of the 5 nm L_g n -type GAA SiGe NW FETs with $L_{UL} = 0$ and 2 nm at the off and on states for the HP applications. μ_s and μ_d are the chemical potential of the source and drain, respectively. The maximum hole barrier height Φ_B is labeled.

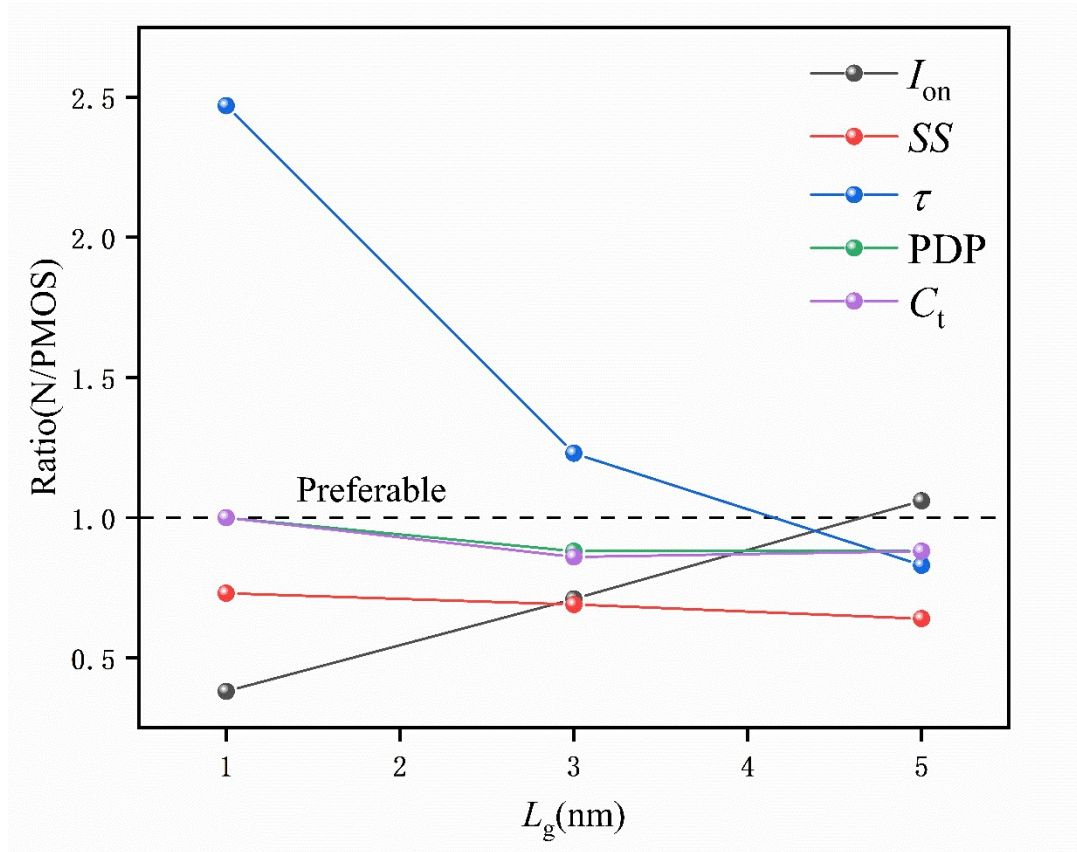


Figure S4. Ratios of I_{on} , SS , τ , PDP , and C_t for NMOS and PMOS at $L_g = 1, 3$, and 5 nm.