Supplementary Information

Charge-transfer doping in C_3N_2 vdWHs endows sub-5 nm FETs with near-Boltzmann switching and ultrahigh on-state current

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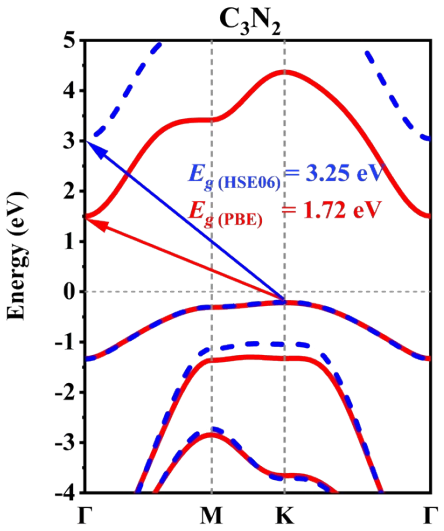

Figure S1 Calculated band structure of monolayer C_3N_2 based on PBE and HSE06 functionals. level. The red solid line represents PBE, and the blue short line represents HSE06.

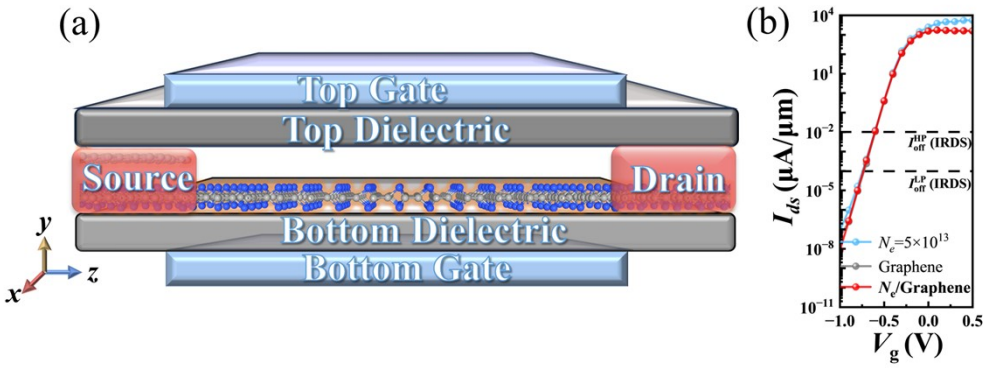

Figure S2 (a) The source is Gr/C_3N_2, and the drain is kept as *n*-type doped FET model device. (b) Transfer characteristics of FETs with different source and drain configurations.

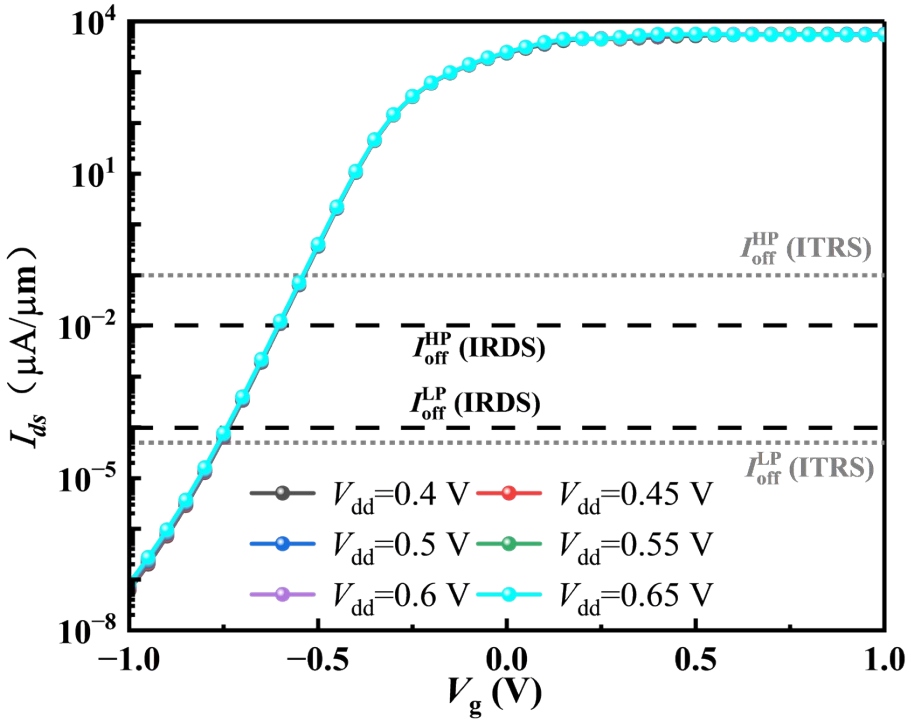

Figure S3: Transfer characteristics of C_3N_2 FETs under supply voltage fluctuations.

To quantitatively assess the stability of device parameters and the potential for further power reduction, we systematically analyze the impact of supply voltage scaling on the transfer characteristics of Sub-5nm-Lg C_3N_2-FETs. In our study, the supply voltage is maintained at 0.65 V in accordance with IRDS standards. To simulate voltage scaling, transfer characteristics are computed over a range from 0.65 V to 0.40 V, decreasing in 0.05 V steps, as depicted in Figure S3. The results indicate that device transport properties remain largely unaffected by supply voltage reductions. This demonstrates that the FET retains robust performance under minor voltage fluctuations, supporting the feasibility of further power optimization through supply voltage scaling.

Table S1 HP and LP I_{on} (μA / μm) and minimum subthreshold swing SS_{min} (mV/dec) of 4.8 nm C_3N_2 FET with different doping concentrations N_e(cm^{-2}) and 4.9 nm G-C_3N_2 FET at 0.65V supply voltage.

FET	N_e	I_{on}**(HP)**	I_{on}**(LP)**	SS_{min}
	5×10^{12}	266	266	61.0
	2×10^{13}	1444	1430	62.9
C_3N_2 (X)	**5×10^{13}**	**3035**	**1430**	**66.1**
	8×10^{13}	2862	1362	68.0
	5×10^{14}			73.2
C_3N_2 (Y)	5×10^{13}	3202	1483	65.9
G-C_3N_2		1656	1120	60.6
G-C_3N_2(S)	$5*10^{13}$(D)	1608	1077	64.5
IRDS		787	602	72

Table S2 HP and LP I_{on} (μA/μm) and SS_{min} (mV/dec) of 5 ×10^{13} N_e (cm^{-2}) C_3N_2 FET, G-C_3N_2 FET under different channel lengths L_g at 0.65 V supply voltage and optimal doping concentration

FET	L_g	I_{on}(HP)	I_{on}(LP)	SS_{min}
C_3N_2	2.3			166.4
	2.9	546		119.9
	3.5	1735	118	91.3
	4.1	2545	852	74.4
	4.8	3035	1430	66.1
G-C_3N_2	1.2			309.1
	2.5	541		113.9
	3.7	1568	782	72.96
	4.9	1669	1147	60.6
IRDS		787	602	

Table S3 calculates the I_{on} (μA/μm), SS_{min} (mV/dec), gate capacitance C_g (fF/μm), delay time τ (ps), and power consumption PDP (fJ/μm) of a 4.8 (4.9) nm channel length C_3N_2 (G-C_3N_2) FET, based on the 2023 edition of the IRDS 2025 standard.

FET	***Type***	I_{on}	SS_{min}	C_g	**τ**	**PDP**
C_3N_2		3035	66.1	0.13	0.60	0.28
G-C_3N_2	**HP**	1656	60.6	0.06	0.51	0.25
IRDS		787	72	0.39	0.96	0.49
C_3N_2		1430	66.1	0.08	0.40	0.04
G-C_3N_2	**LP**	1120	60.6	0.05	0.29	0.02
IRDS		602	67	0.39	1.26	0.49