Supporting Information

Coordinated Sub-cycle Modulation Atomic Layer Deposition of Atomic-level Homogeneous $GeTe_9$ Thin Film for High-performance OTS

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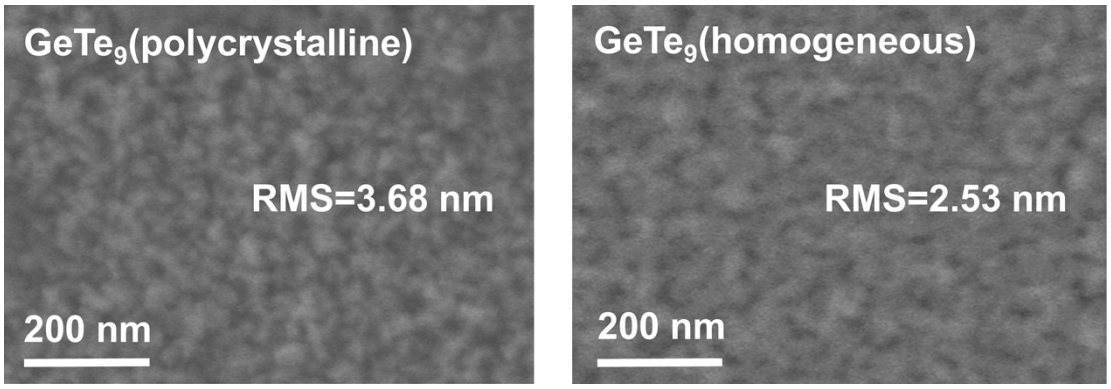

Figure S1. SEM images of $GeTe_9$ (polycrystalline) and $GeTe_9$ (homogeneous).

Figure S1 compares the surface morphology of $GeTe_9$ films synthesized under different sub-cycle conditions. The polycrystalline $GeTe_9$ film exhibits a relatively rough surface with a RMS roughness of 3.68 nm, which is attributed to the irregular grain growth and high grain-boundary density caused by insufficient precursor flux. In contrast, the homogeneous $GeTe_9$ film produced via the CSM strategy demonstrates a significantly smoother and more uniform surface with a reduced RMS roughness of 2.53 nm. This improvement confirms that the precise regulation of the super-cycle thickness to match the atomic diffusion length effectively suppresses the formation of large crystalline clusters, resulting in a more integrated and isotropic amorphous matrix.

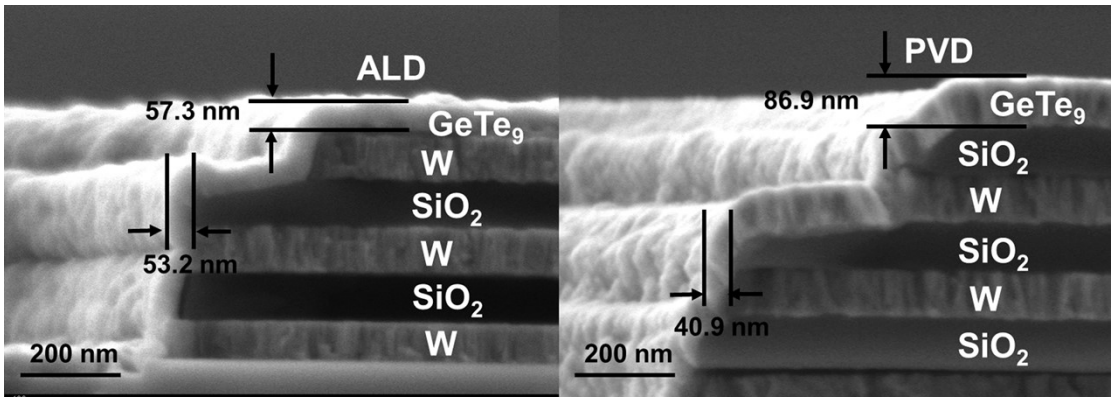

Figure S2. Comparison of step coverage between ALD and PVD deposited films.

The cross-sectional SEM images in Figure S2 illustrate the deposition of the $GeTe_9$ film onto a 3D stacked structure for vertical integration composed of W and SiO_2 layers. This comparison highlights the irreplaceable advantage of ALD over PVD for such complex high-aspect-ratio features. The ALD-deposited film exhibits excellent conformal growth across the W/SiO_2 stack, maintaining a sidewall thickness of 53.2 nm relative to a top thickness of 57.3 nm, which corresponds to a step coverage of approximately 93%. Conversely, the PVD-deposited film shows poor conformality due to the inherent shadowing effect, where the sidewall thickness is significantly reduced to 40.9 nm compared to 86.9 nm at the top surface, yielding a step coverage of only 47%. These results validate that the ALD-CSM approach provides the high-precision conformal filling required for advanced 3D memory architectures.

Table S1. Comparison of film properties deposited by ALD (CSM strategy) and PVD.

	ALD (This work, CSM)	PVD
Depositional state	Amorphous	Amorphous
Crystallization temperature	250 ℃	131 ℃[1]
RMS	2.53 nm	1.25 nm[2]
Step Coverage	93%	47%

Table S1 provides a quantitative benchmarking of $GeTe_9$ film properties synthesized by ALD and PVD. Both films remain in the amorphous state upon deposition. The amorphous structure of the ALD film is maintained up to 200 °C, providing an experimental reference for the thermal stability of Te-rich OTS selectors. While the PVD film exhibits lower surface roughness, its primary deficiency lies in the poor step coverage. In contrast, the ALD film synthesized via the CSM strategy achieves a superior step coverage of 93%, which is nearly double that of the PVD counterpart (47%), demonstrating its significant advantage for 3D vertical integration.

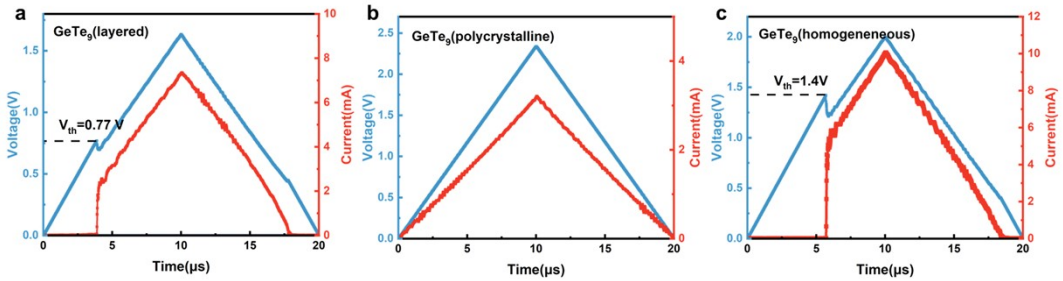

Figure S3. Triangular wave response of the three devices.

Figure S3 illustrates the transient switching characteristics of the three types of $GeTe_9$ devices under triangular voltage sweeps. The $GeTe_9$ (layered) device (a) exhibits a relatively low threshold voltage of approximately 0.77 V due to the presence of Te-rich pathways. The $GeTe_9$ (polycrystalline) device (b) fails to show any threshold switching behavior and instead presents a purely resistive response, indicating structural degradation and uncontrolled leakage. In stark contrast, the homogeneous $GeTe_9$ device (c) demonstrates an ideal OTS response with a high and stable threshold voltage of 1.4 V and excellent reversibility. This comparison corroborates that achieving atomic-level homogeneity is the fundamental prerequisite for reliable and high-performance switching operation.

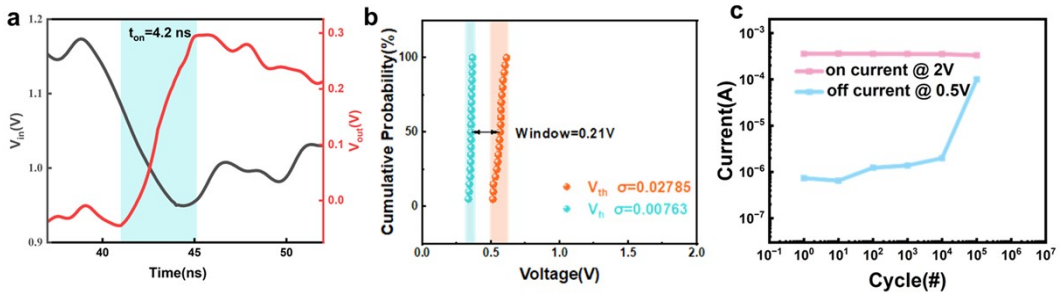

Figure S4. Electrical characteristics of $GeTe_9$ (layered). (a) Switching speed of $GeTe_9$ (layered). (b) Threshold stability of $GeTe_9$ (layered). (c) Cycle endurance of $GeTe_9$ (layered).

The electrical performance of the $GeTe_9$ (layered) device is presented in Figure S4 for comparative analysis. As shown in Figure S4(a), the device achieves a switching speed of 4.2 ns. Figure S4(b) illustrates the V_{th} characteristics, where the $GeTe_9$ (layered) device exhibits a low V_{th} and a notably narrow switching window of 0.21 V. This specific dataset was recorded for only 40 cycles because the layered device is highly prone to functional failure during testing. This inherent instability is further evidenced in Figure S4(c), where the cycle endurance is limited to only 10^4 cycles, representing a significant five-order-of-magnitude decrease compared to the 10^9 cycles achieved by the CSM-optimized $GeTe_9$ (homogeneous) device.

Reference:

[1] L. Wang, J. Wen, Z. Liu, J. Chen, H. Tong and X. Miao, Thermally stable and high-speed Ge-Te based ovonic threshold switching selector with a Ge intercalated structure, *IEEE Electron Device Lett.,* 2023, **44**, 1096−1099.

[2] A. Manivannan, S. K. Myana, K. Miriyala, S. Sahu and R. Ramadurai, Low power ovonic threshold switching characteristics of thin $GeTe_6$ films using conductive atomic force microscopy, *Appl. Phys. Lett.*, 2014, **105**, 243501.