Supplementary Information

Residual Stress Modulation as a Pathway to Reliable Multilevel 3D NAND Flash Storage

Ruifu Zhou[1], Ik-Jyae Kim[1], Sejun Park[2], Hyukchang Kwon[2], and Jang-Sik Lee[1]

[1]Pohang University of Science and Technology (POSTECH), Pohang 37673, Korea

[2]Device Solutions, Samsung Electronics Co., Hwaseong 18448, Korea

Corresponding author: Jang-Sik Lee (e-mail: jangsik@postech.ac.kr).

Table S1. Mechanical parameters used in the simulation.

Material	CTE (10^{-6}/K)	Young's modulus (GPa)	Poisson's ratio
SiO_2	1	59	0.24
SiN	3	260	0.23
Poly-Si	2.8	164	0.24
W	4.6	410	0.28
Al_2O_3	8.18	390	0.22
TiN	10.8	410	0.27

Table S2. Trap parameters of the charge-trap nitride (CTN) used in the simulation.

Trap Parameter	Used in simulation
Density of acceptor-like traps, N_{TA} (cm^{-3})	6.00×10^{19}
Peak energy level of acceptor-like traps, E_{TA} from conduction band (eV)	1.40
Capture cross section of acceptor-like traps, CCS_A (cm^2)	3.00×10^{-14}
Standard deviation of acceptor-like traps, σ_A (eV)	0.2
Density of donor-like traps, N_{TD} (cm^{-3})	6.00×10^{19}
Peak energy level of donor-like traps, E_{TD} from valence band (eV)	1.36
Capture cross section of donor-like traps, CCS_D (cm^2)	1.50×10^{-14}
Standard deviation of donor-like traps, σ_D (eV)	0.2

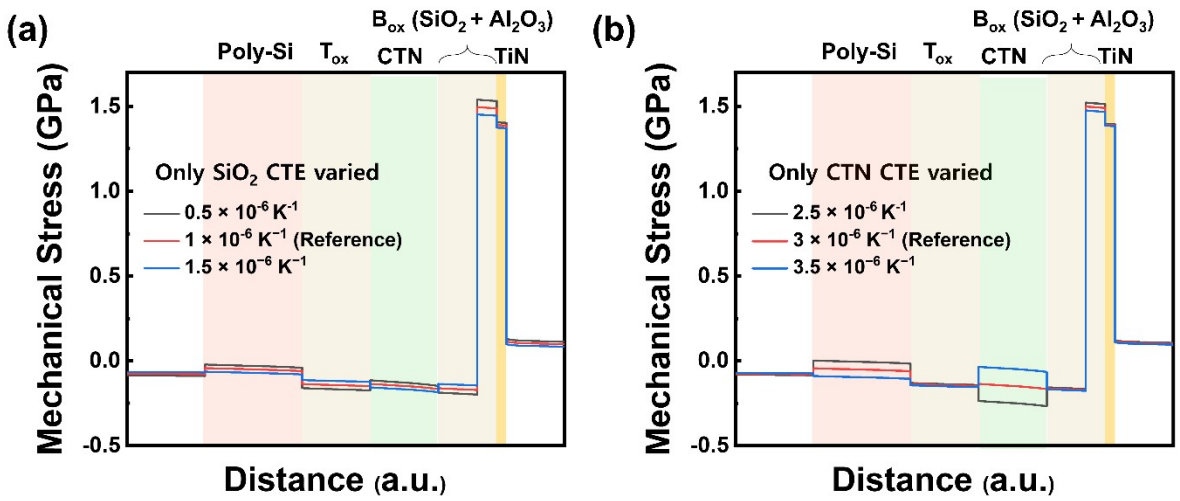

Fig. S1. Effect of the CTE of SiO_2 and CTN on the simulated residual stress distribution. (a) Residual stress distribution obtained by varying the CTE of SiO_2. (b) Residual stress distribution obtained by varying the CTE of CTN.

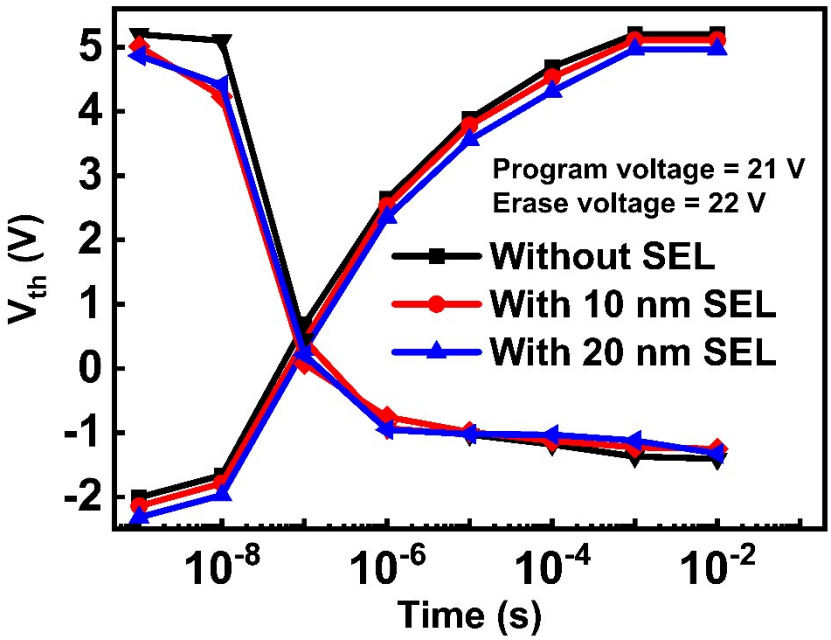

Fig. S2. Simulated V_T evolution during program and erase operations for the reference structure and structures with 10- or 20-nm SELs.

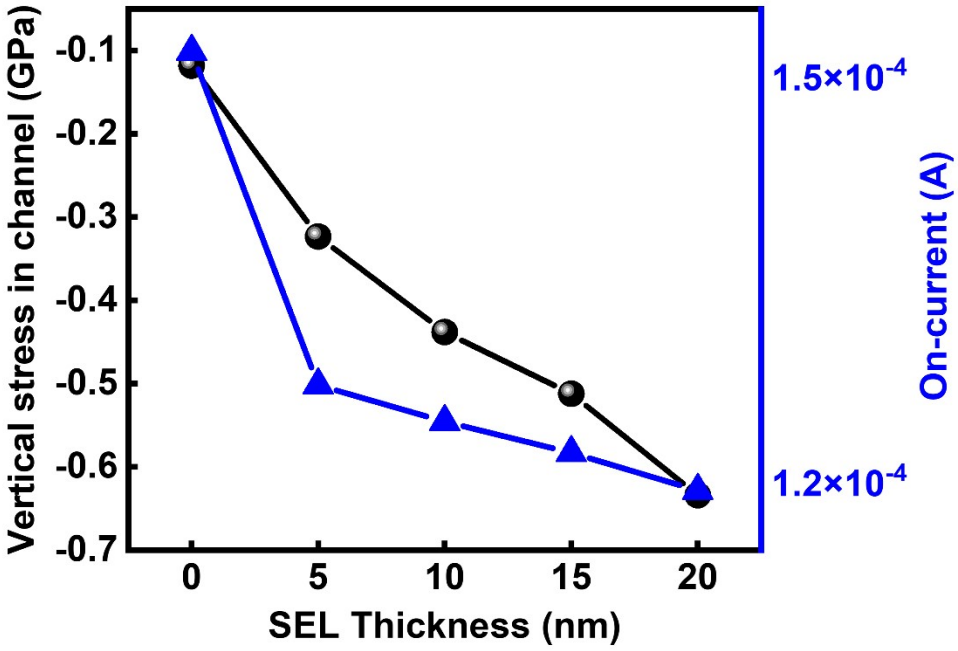

Fig. S3. SEL-thickness-dependent vertical channel stress and on-current.