Supplementary Information

High-Performance Electrode-Controlled $MoTe_2$ Memristor for Dual-Mode Synaptic Plasticity in Neuromorphic Systems

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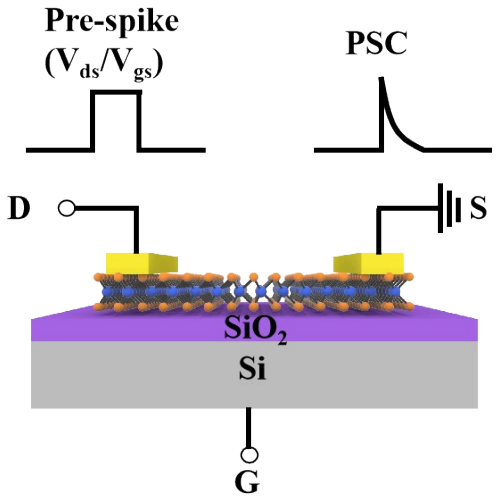

Fig. S1. Schematic diagram of a conventional thermal evaporation top-electrode device

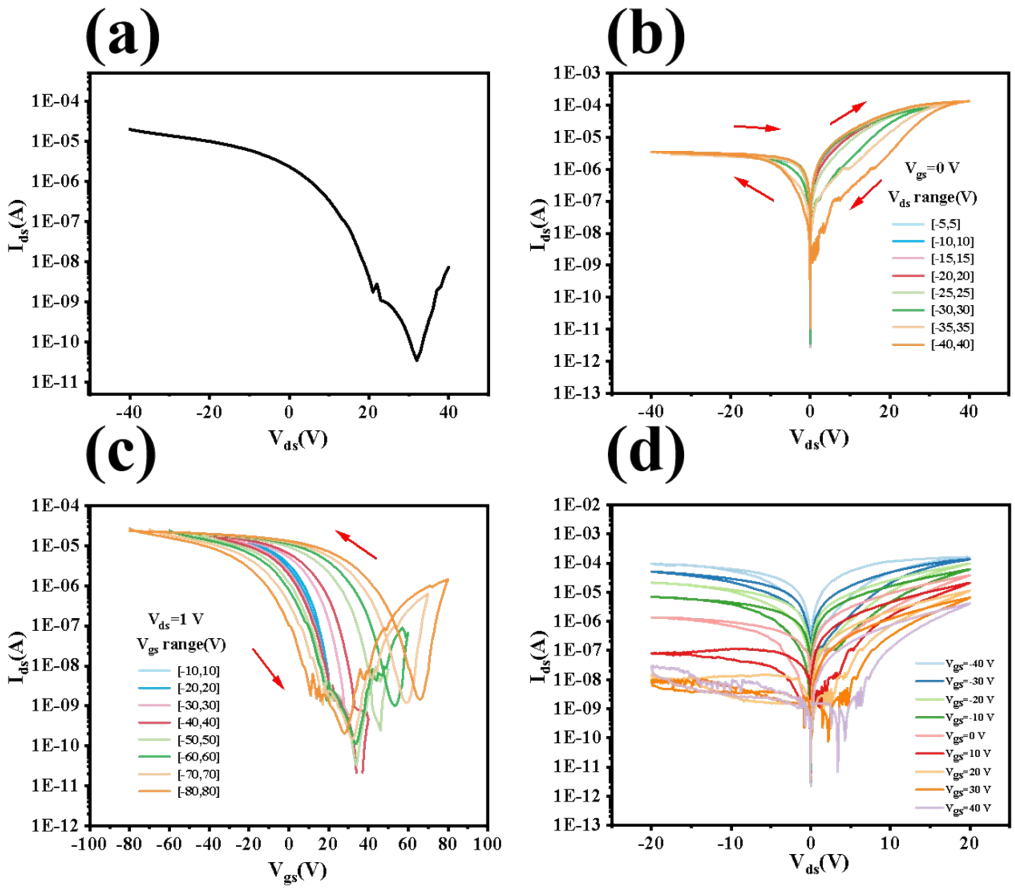

Fig. S2. Memristive property tests of the thermal evaporation top-electrode $MoTe_2$ device: (a) transfer characteristic curve; (b) output hysteresis with different bias scanning ranges; (c) transfer hysteresis with different gate voltage scanning ranges; (d) output hysteresis under different gate voltages

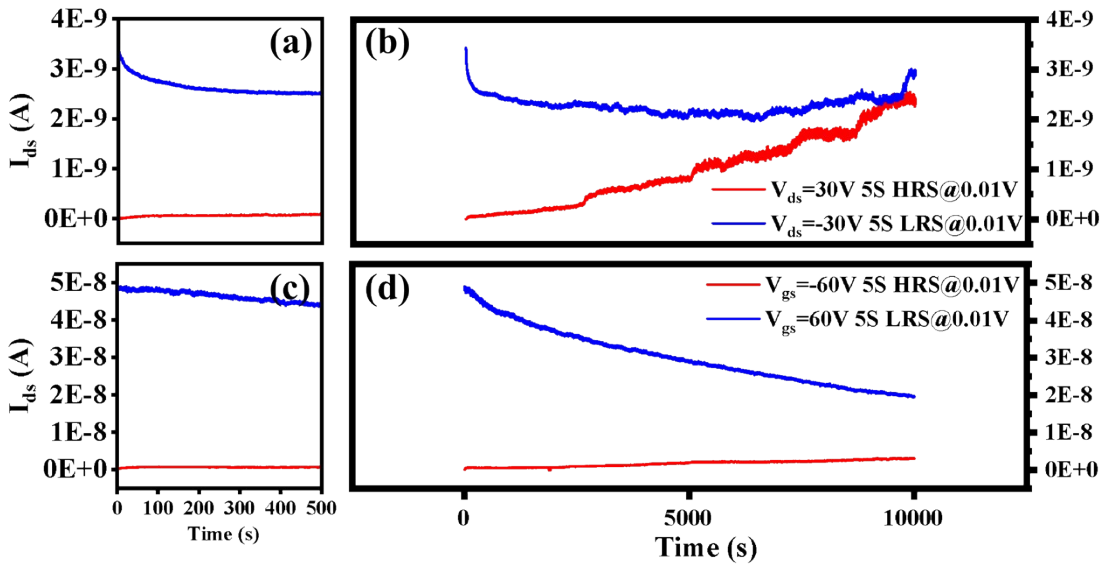

Fig. S3. (a) 500-second retention characteristics of homosynapses at a read voltage of V_{ds}=0.01V after V_{ds} pulse operation(HRS: 30V for 5s; LRS: -30V for 5s)(b) 10,000-second retention characteristics of homosynapses at a read voltage of V_{ds}=0.01V after V_{ds} pulse operation(HRS: 30V for 5s; LRS: -30V for 5s)(c) 500-second retention characteristics of heterosynapses at a read voltage of V_{ds}=0.01V after V_{gs} pulse operation(HRS: -60V for 5s; LRS: 60V for 5s)(d) 10,000-second retention characteristics of heterosynapses at a read voltage of V_{ds}=0.01V after V_{gs} pulse operation(HRS: -60V for 5s; LRS: 60V for 5s).

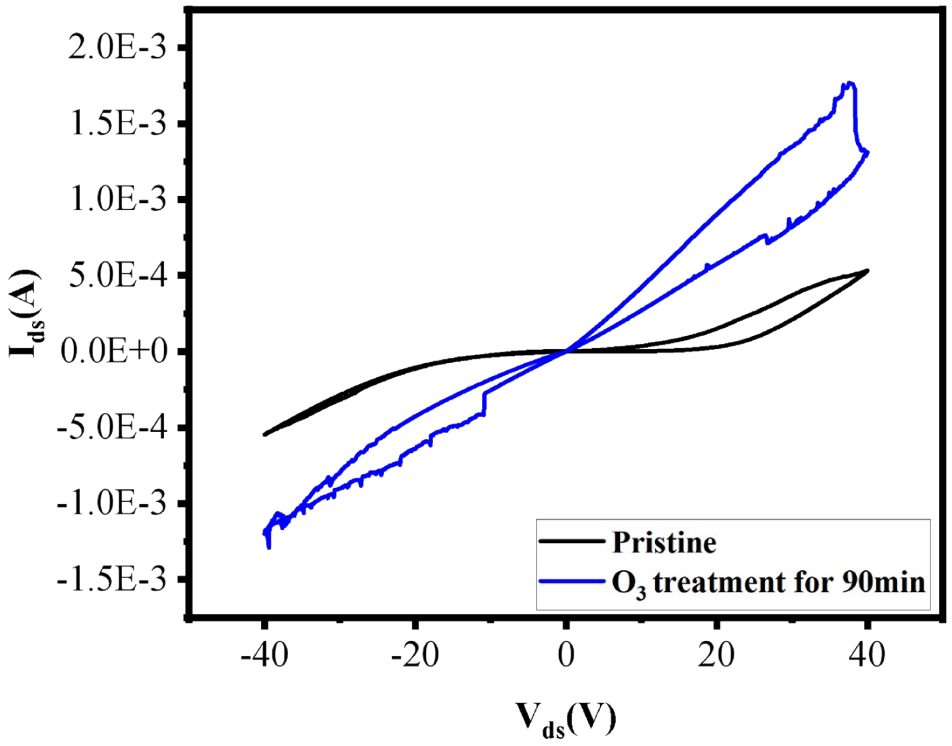

Fig. S4. Output hysteresis curves of the device under different treatments.

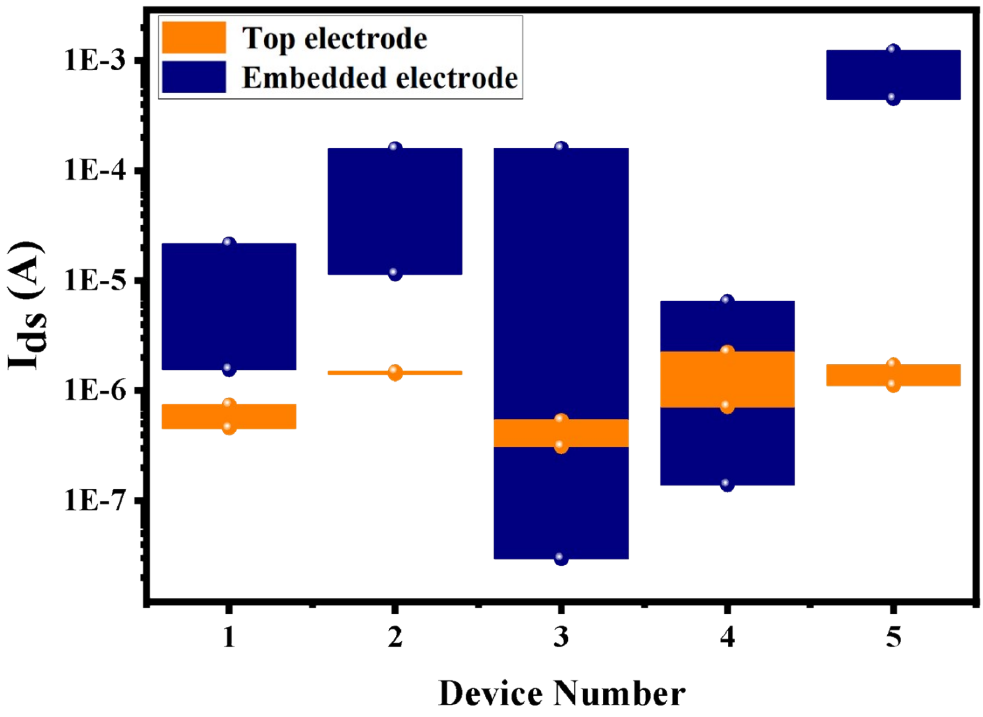

Fig. S5. Statistical distribution of I_{ds} at 20 V for embedded-electrode and top-electrode devices. The I_{ds} values were extracted from hysteresis curves measured under a voltage sweep of −40 V to 40 V.

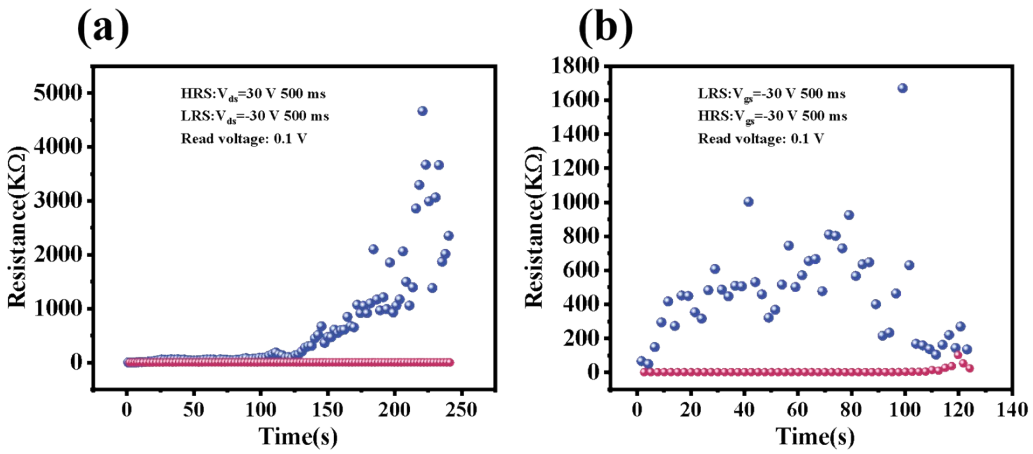

Fig. S6. Resistance switching characteristic tests of the thermal evaporation top-electrode device: (a) Homosynapse; (b) Heterosynapse.

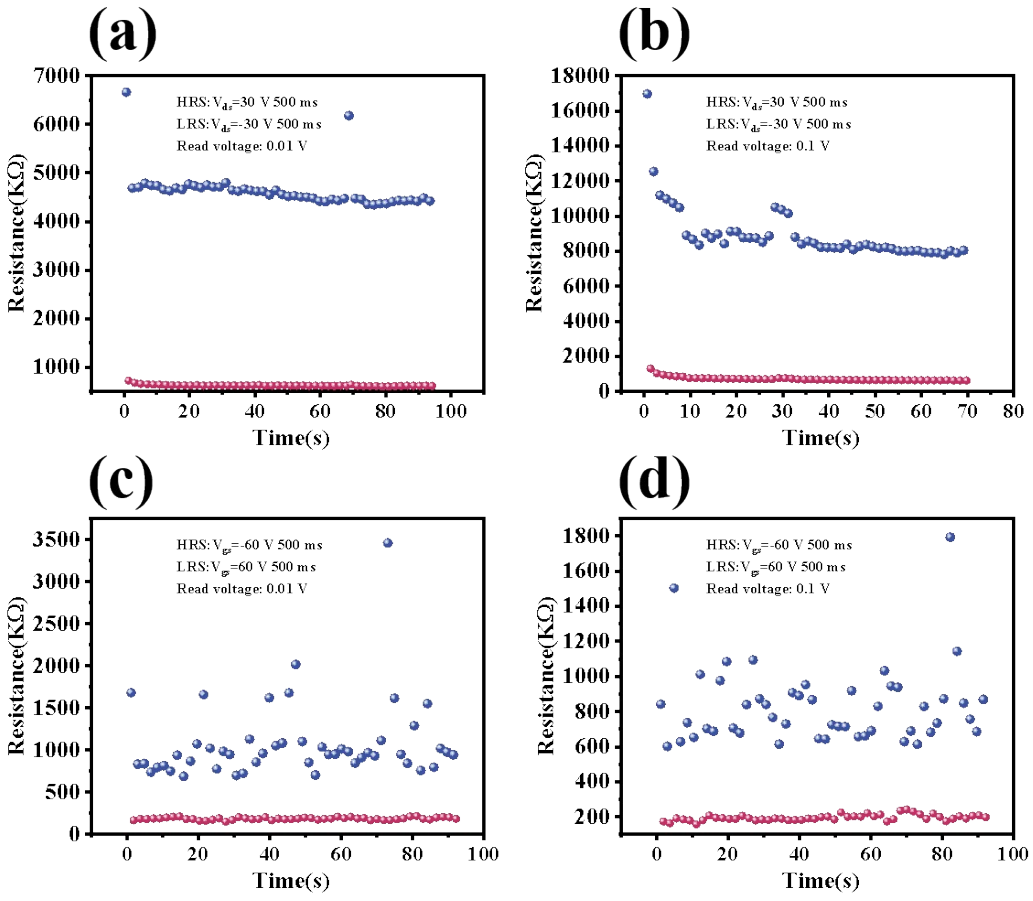

Fig. S7. Resistance switching characteristic tests of the embedded electrode device: (a-b) Homosynapse; (c-d) Heterosynapse.

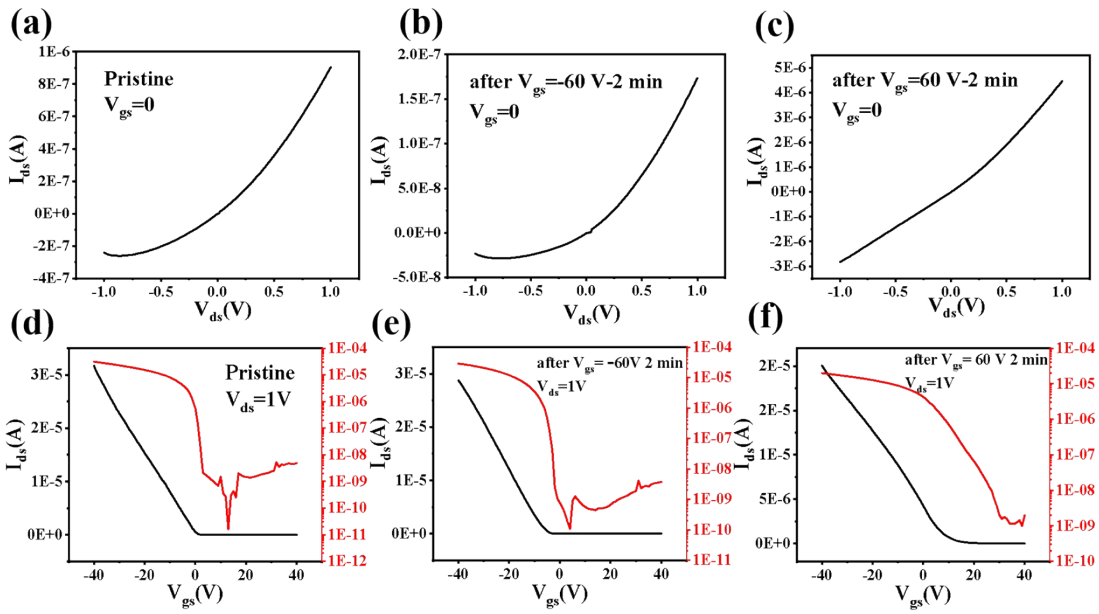

Fig. S8. Original (a) output curves and (d) transfer curves of the embedded electrode device in atmospheric environment, (b) output curves and (e) transfer curves after suppression by -60 V gate voltage, (c) output curves and (f) transfer curves after stimulation by +60 V gate voltage.

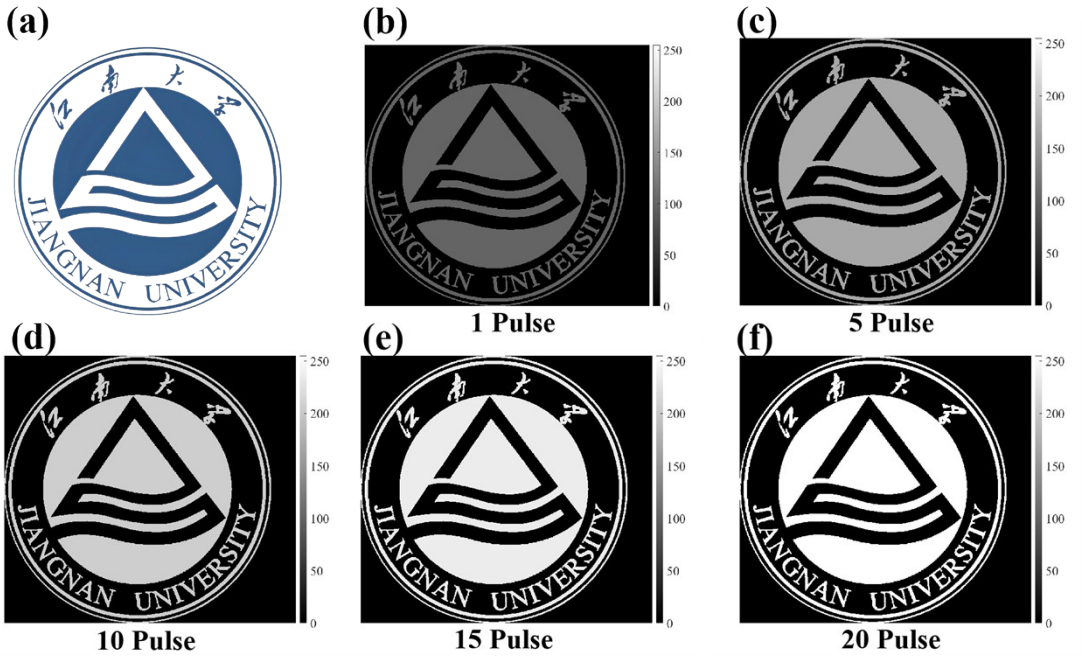

Fig. S9. Grayscale image writing after different numbers of pulses: (a) Original image; (b) 1 pulse; (c) 5 pulses; (d) 10 pulses; (e) 15 pulses; (f) 20 pulses.

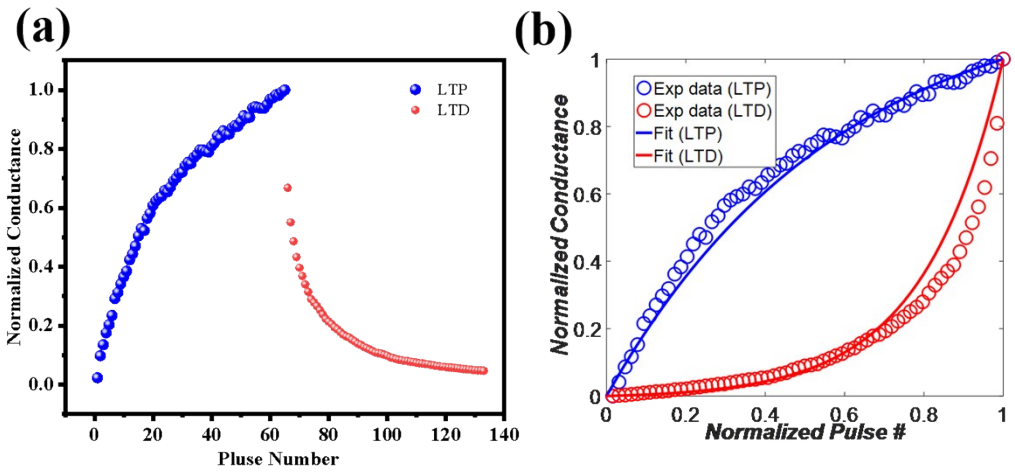

Fig. S10. (a) Long-term potentiation (LTP) and depression (LTD) curves measured by applying 128 gate voltage pulses (including 64 positive pulses (10 V) followed by 64 negative pulses (-10 V)). The width and interval of the voltage pulses are 1 s. (b) Nonlinearity fitted from the LTP and LTD curves.