Supplementary Information

Contact Engineering of MoS_2 Synaptic Transistors via Reactive Ion Etching

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Supplementary Information:

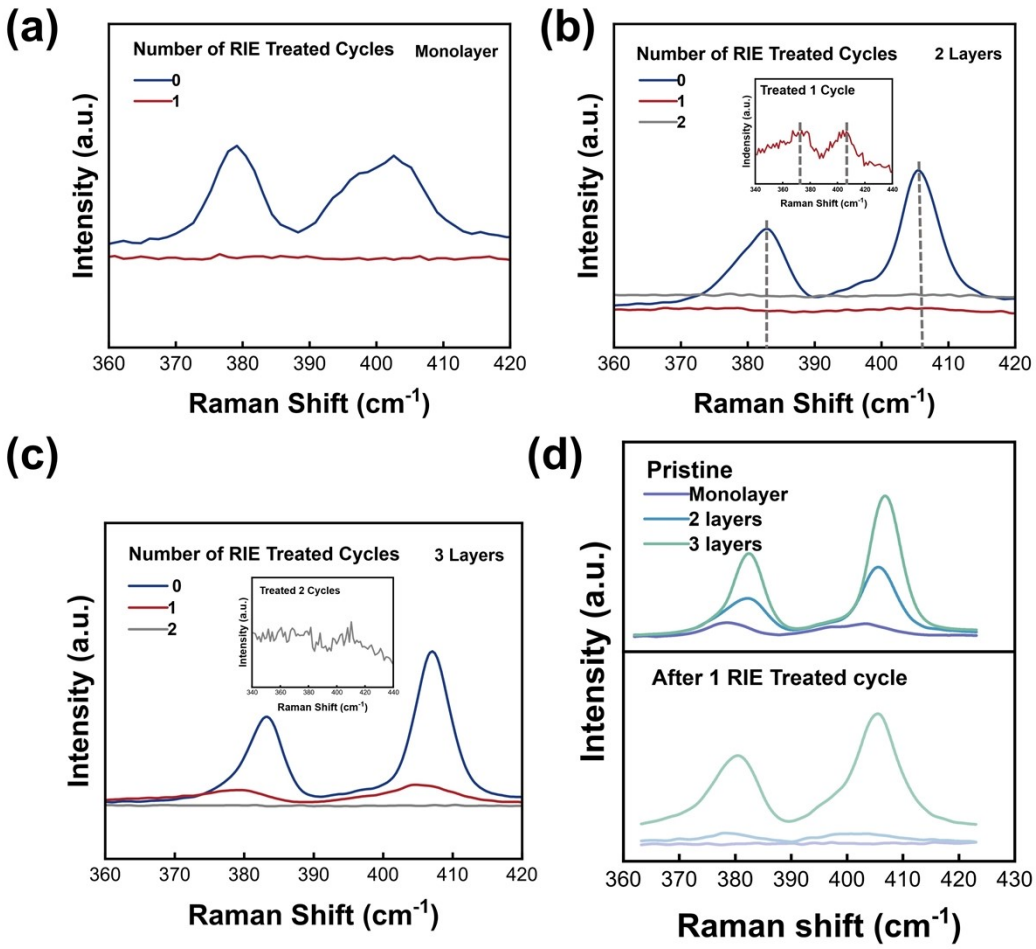

Figure S1. Raman evolution of mono-, bi-, and trilayer MoS_2 flakes on Au after successive RIE cycles. (a) Raman spectra of monolayer MoS_2 on Au before and after one etching cycle. (b) Raman spectra of bilayer MoS_2 on Au before treatment and after one and two etching cycles; inset: enlarged view of the weak Raman signal after one etching cycle. (c) Raman spectra of trilayer MoS_2 on Au before treatment and after one and two etching cycles; inset: enlarged view of the weak Raman signal after two etching cycles. (d) Comparison of the Raman spectra of pristine mono-, bi-, and trilayer MoS_2 flakes on Au and their evolution after one etching cycle. The progressive weakening of the Raman response with decreasing thickness supports the stepwise thinning behavior induced by RIE.

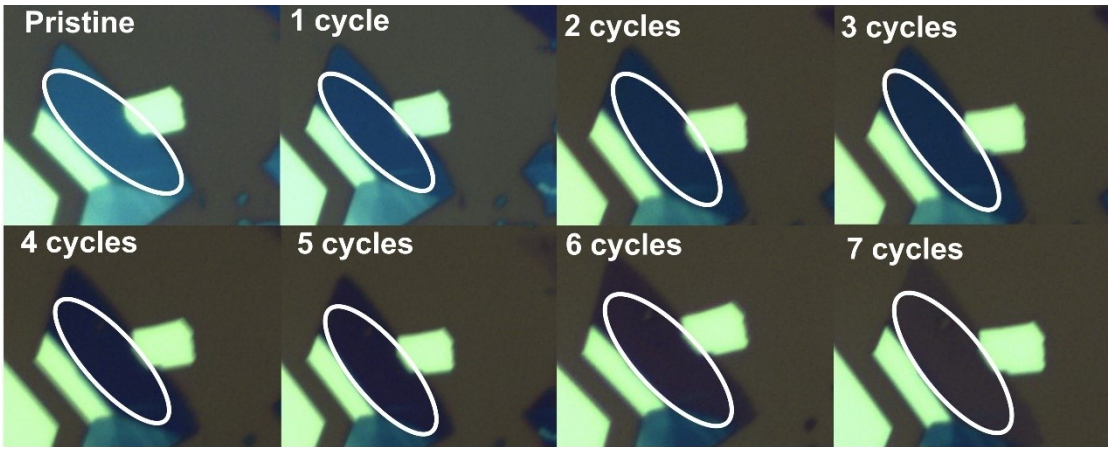

Figure S2. Optical micrographs of the same MoS_2 flake on SiO_2/Si from the pristine state to after seven successive RIE cycles. The circled area marks the tracked region.

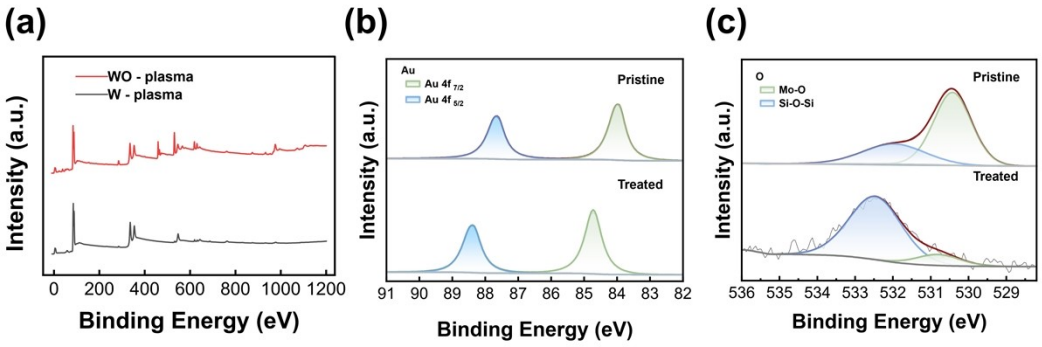

Figure S3. Additional XPS analysis of pristine and contact-etched MoS_2 on Au. (a) XPS survey spectra of samples without and with plasma treatment. (b) High-resolution Au 4f spectra of pristine and contact-etched samples. (c) High-resolution O 1s spectra, showing that the reduced Mo–O-related contribution and the enhanced Si–O–Si signal after etching are consistent with thinning of the MoS_2 layer and the increased contribution of the underlying SiO_2/Si substrate to the XPS signal.

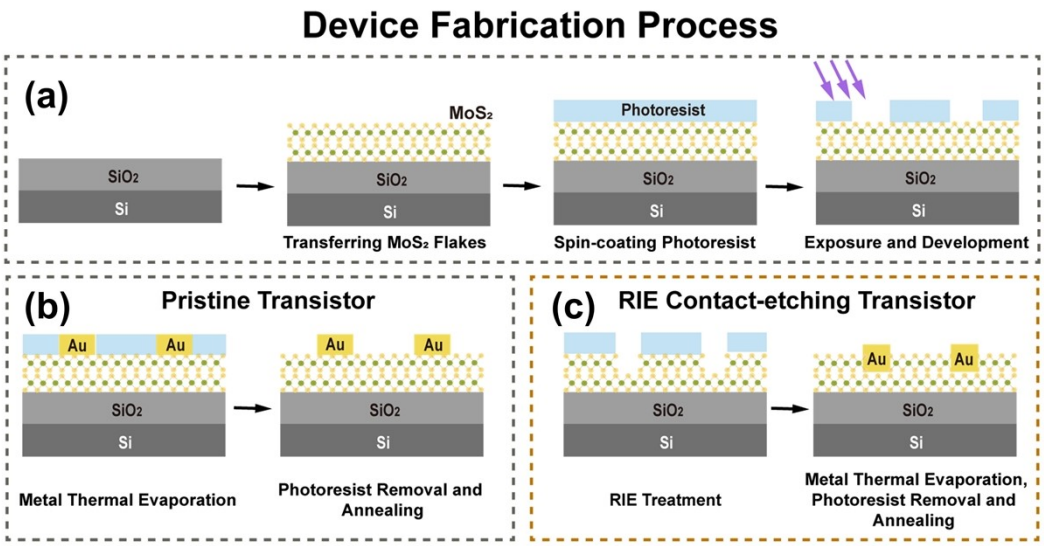

Figure S4. Comparison of the fabrication processes for pristine and contact-etched MoS_2 FETs. (a) Shared fabrication steps for both device types, including mechanical exfoliation of MoS_2 flakes onto SiO_2/Si substrates, followed by photoresist coating, soft baking, UV exposure, and development to define the electrode pattern. (b) Subsequent process for the pristine devices: direct deposition of Cr/Au electrodes after development, followed by lift-off, forming conventional top contacts. (c) Subsequent process for the contact-etched devices: an additional RIE step is introduced after development and before Cr/Au deposition, followed by lift-off, producing top electrodes with edge-contact characteristics. Both device types were finally annealed at 200 °C for 2 h.

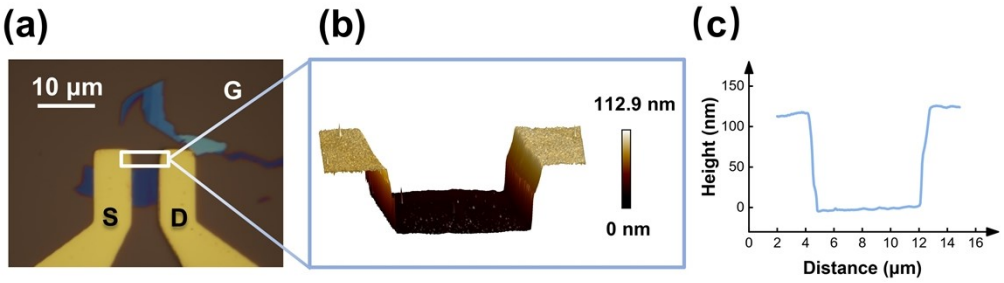

Figure S5. AFM characterization of the contact-etched electrode edge. (a) Optical image of a contact-etched device. (b) AFM 3D topographic image acquired from the boxed region in (a). (c) Corresponding height profile. A slight non-vertical feature is visible at the electrode edge, which is likely related to the resolution limits of the photolithography and development processes. No obvious additional residual layer attributable to the CF_4/Ar etching step is observed on the substrate near the electrode edge, although a trace amount of fabrication-related resist residue cannot be completely excluded.

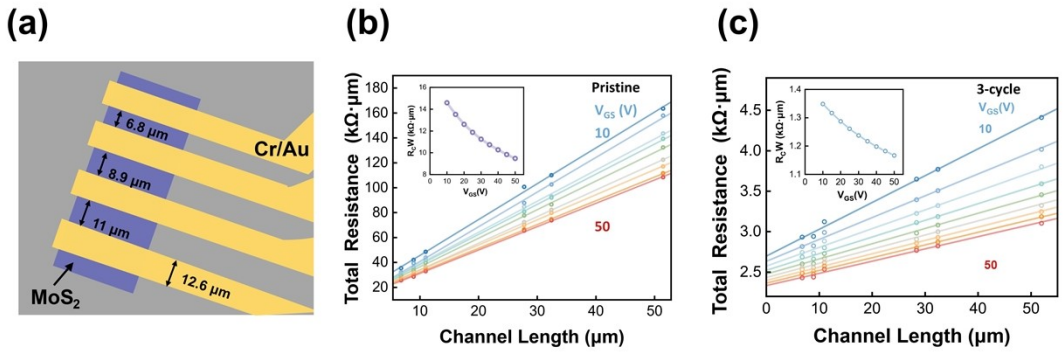

Figure S6. Transmission line method (TLM) analysis of the pristine and contact-etched MoS_2 FETs. (a) Schematic illustration of the corresponding TLM test structure. (b, c) Total resistance as a function of channel length measured at different V_{GS} , together with the extracted channel-width-normalized contact resistance R_c (inset), for (b) pristine and (c) three-cycle contact-etched MoS_2 FETs.

Total resistance normalized by channel width (R_{total}·W) as a function of channel length (L) measured at different gate voltages (V_{GS}). The total resistance was extracted from the low-bias linear regime using $R_{total} = V_{DS} / I_{DS}$. According to the TLM relationship,

$$R_{total}{\cdot}W = 2R_c{\cdot}W + R_{sh}{\cdot}L \#(S3)$$

where R_c is the contact resistance of a single contact, W is the channel width, and R_{sh} is the sheet resistance of the MoS_2 channel. Therefore, linear fitting of the R_{total}·W–L plots at each V_{GS} gives the sheet resistance from the slope and the contact resistance from half of the y-intercept. The inset shows the extracted R_c·W as a function of V_{GS}, indicating that the contact resistance decreases with increasing gate bias. The minimum R_c·W of the pristine device is about 9.48 kΩ·μm at V_{GS} = 50 V, whereas that of the three-cycle contact-etched device is about 1.15 kΩ·μm.

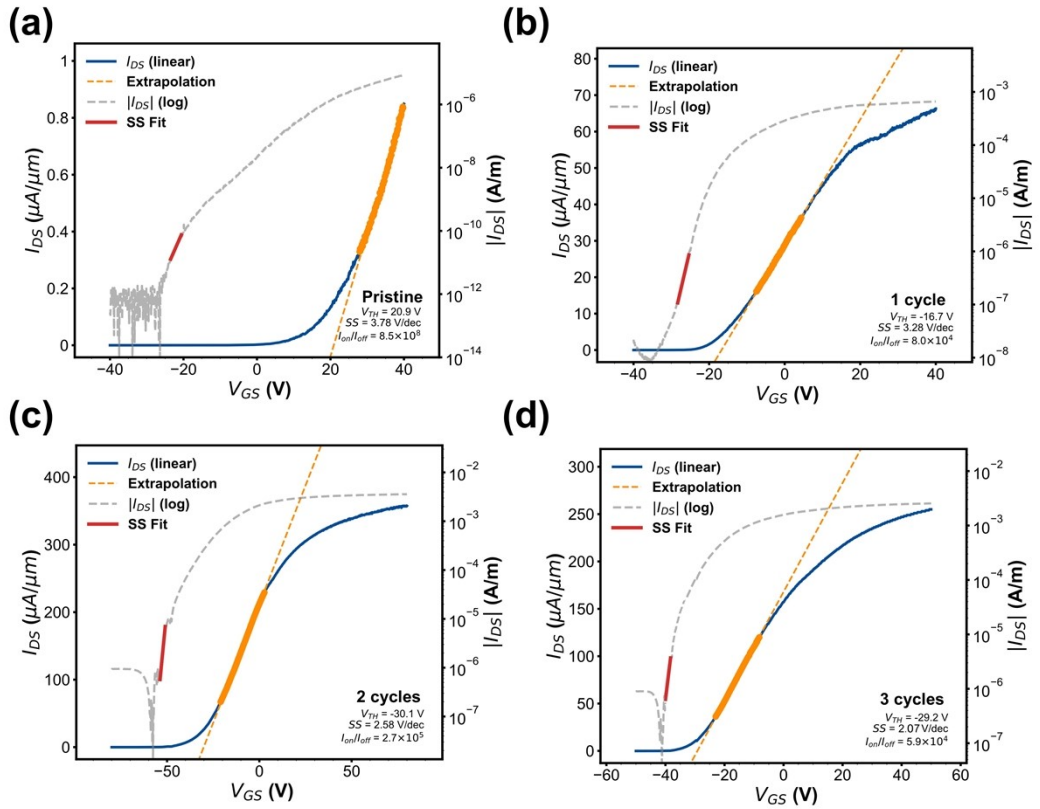

Figure S7. Extraction of threshold voltage (V_{TH}), subthreshold swing (SS), on/off current ratio, and field-effect mobility (μ_{FE}) from the transfer curves. The curves are from (a) pristine, (b) one-cycle, (c) two-cycle, and (d) three-cycle contact-etched MoS_2 FETs. In each panel, the blue curve shows the linear-scale transfer characteristic used for V_{TH} extraction, and the gray curve shows the semi-logarithmic transfer characteristic used for SS and on/off ratio extraction. V_{TH} was determined from the linear extrapolation of the I_{DS}–V_{GS} curve in the linear-current regime. SS was obtained from the fitted subthreshold region according to:

$$SS = \frac{dV_{GS}}{d(log_{10}|I_{DS}|)} \#(S1)$$

The on/off ratio was calculated as $|I_{ON}|/|I_{OFF}|$, where I_{ON} and I_{OFF} are the maximum and minimum drain currents extracted from the same transfer curve, respectively. The field-effect mobility (μ_{FE}) was calculated according to:

$$\mu_{FE} = \frac{L}{W \cdot Cox \times V_{DS}} g_m \#(S2)$$

where $g_m = dI_{DS} / dV_{GS}$ in the linear regime.

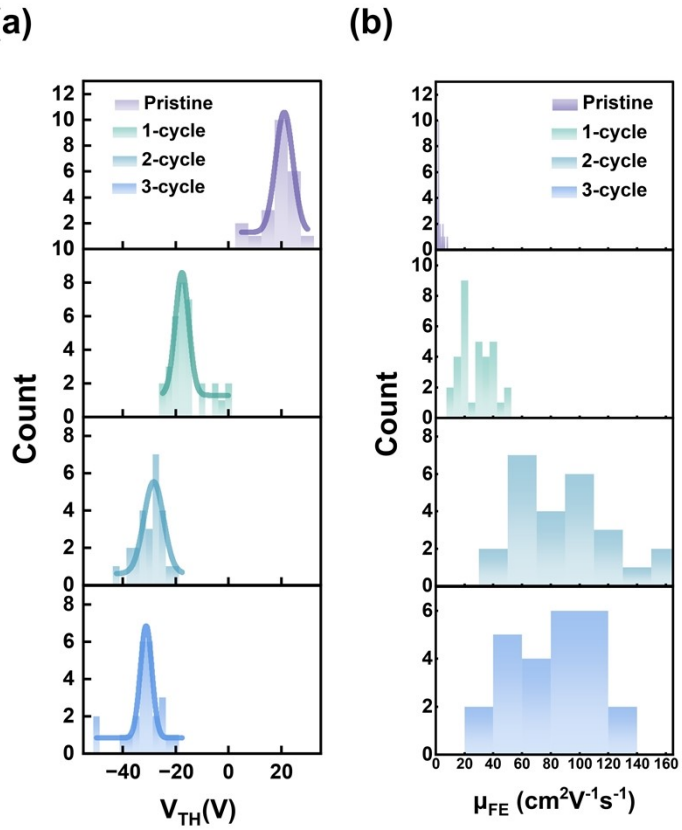

Figure S8. Statistical distributions of threshold voltage and field-effect mobility for multiple fabricated devices. Distributions of the extracted (a) threshold voltage (V_{TH}) and (b) field-effect mobility (μ_{FE}) for pristine, one-cycle, two-cycle, and three-cycle contact-etched MoS_2 devices. The numbers of analyzed devices are 23, 33, 25, and 25 for the pristine, one-cycle, two-cycle, and three-cycle devices, respectively. The fitted curves are included as guides to the distribution trend. Compared with the pristine devices, the contact-etched devices exhibit an overall negative shift in V_{TH} and generally higher μ_{FE}. The devices presented in the main text were selected by jointly considering V_{TH}, μ_{FE}, hysteresis-window width, current level, and overall electrical behavior.

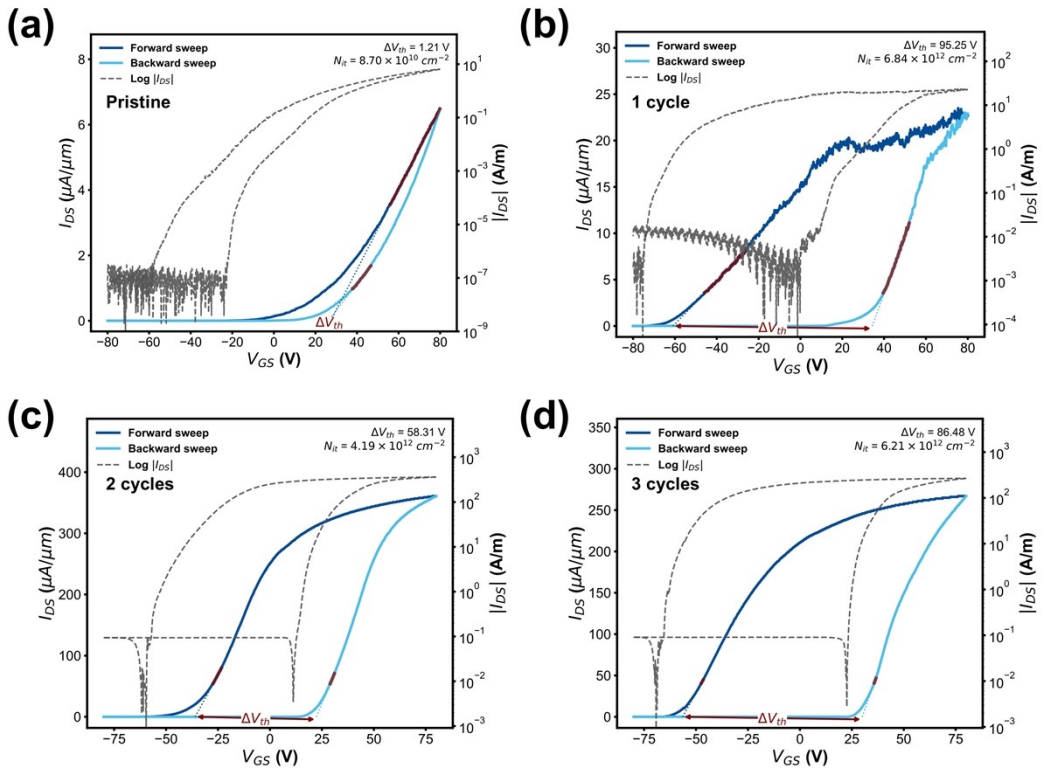

Figure S9. Extraction of memory window (ΔV_{TH}) and effective trap density (N_{it}) from hysteresis curves for devices with different etching cycles. The curves are obtained from (a) pristine, (b) one-cycle, (c) two-cycle, and (d) three-cycle contact-etched MoS_2 FETs. For each panel, the threshold voltages of the forward and backward sweeps were extracted independently by linear extrapolation of the I_{DS}–V_{GS} curves. The memory window was determined as $\Delta V_{TH} = |V_{TH,forward} - V_{TH,backward}|$. The effective trap density was estimated using $N_{it} = \frac{C_i \Delta V_{TH}}{q}$.

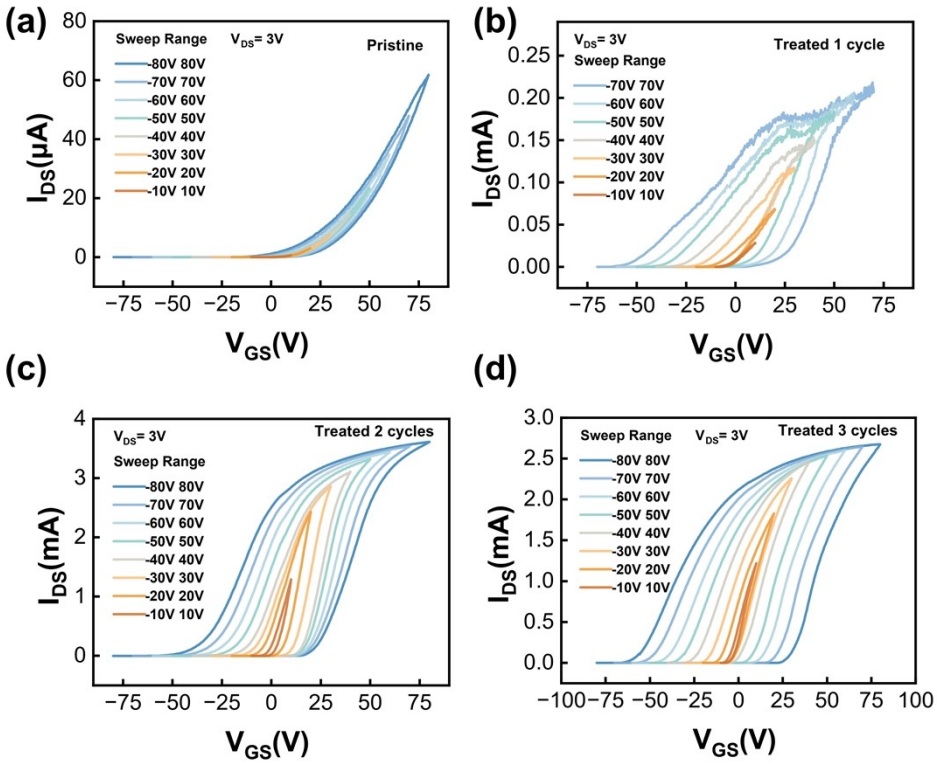

Figure S10. Hysteresis curves with various sweep ranges for devices with different etching cycles. The curves are obtained from (a) pristine, (b) one-cycle, (c) two-cycle, and (d) three-cycle contact-etched MoS_2 FETs. The electrical characteristics were measured at V_{DS} = 3 V while the gate-voltage sweep range was decreased.

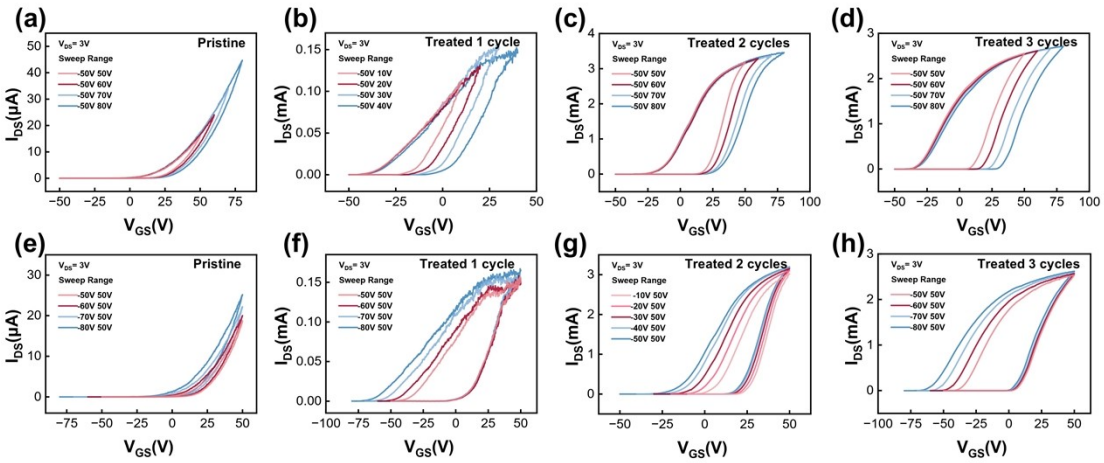

Figure S11. Hysteresis curves measured under asymmetric gate-voltage sweep ranges for devices with different etching cycles. The curves are obtained from pristine (a, e), one-cycle (b, f), two-cycle (c, g), and three-cycle contact-etched (d, h) MoS_2 FETs. In (a–d), the negative sweep limit was fixed at −50 V while the positive sweep limit was increased stepwise. In (e–h), the positive sweep limit was fixed at +50 V while the negative sweep limit was extended stepwise. The measurements were performed at V_{DS} = 3 V. The asymmetric sweep ranges mainly affect the corresponding branches of the hysteresis curves, resulting in different extracted memory windows.

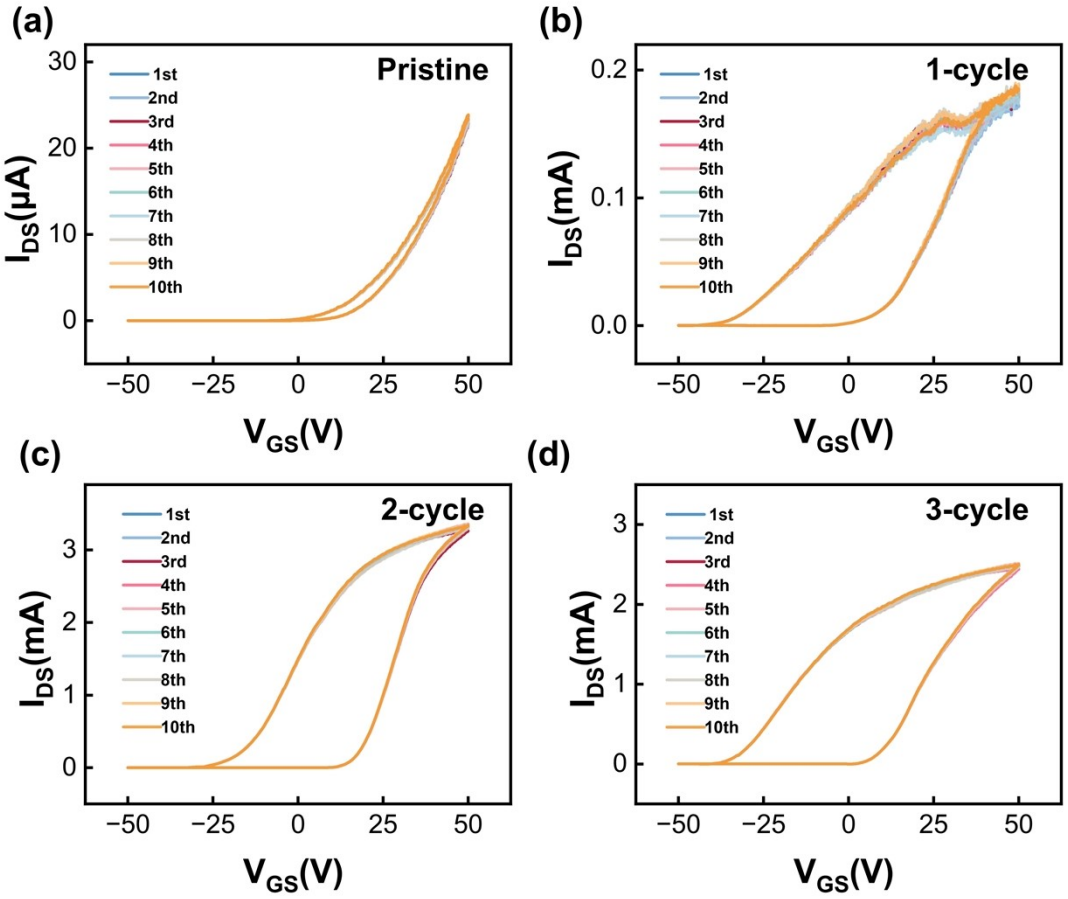

Figure S12. Stability of hysteresis curves over ten consecutive measurements. (a) Pristine, (b) one-cycle, (c) two-cycle, and (d) three-cycle contact-etched MoS_2 FETs. The measurements were performed at V_{DS} = 3 V. The curves largely overlap for each device, indicating good operational stability with only slight shifts during repeated measurements.

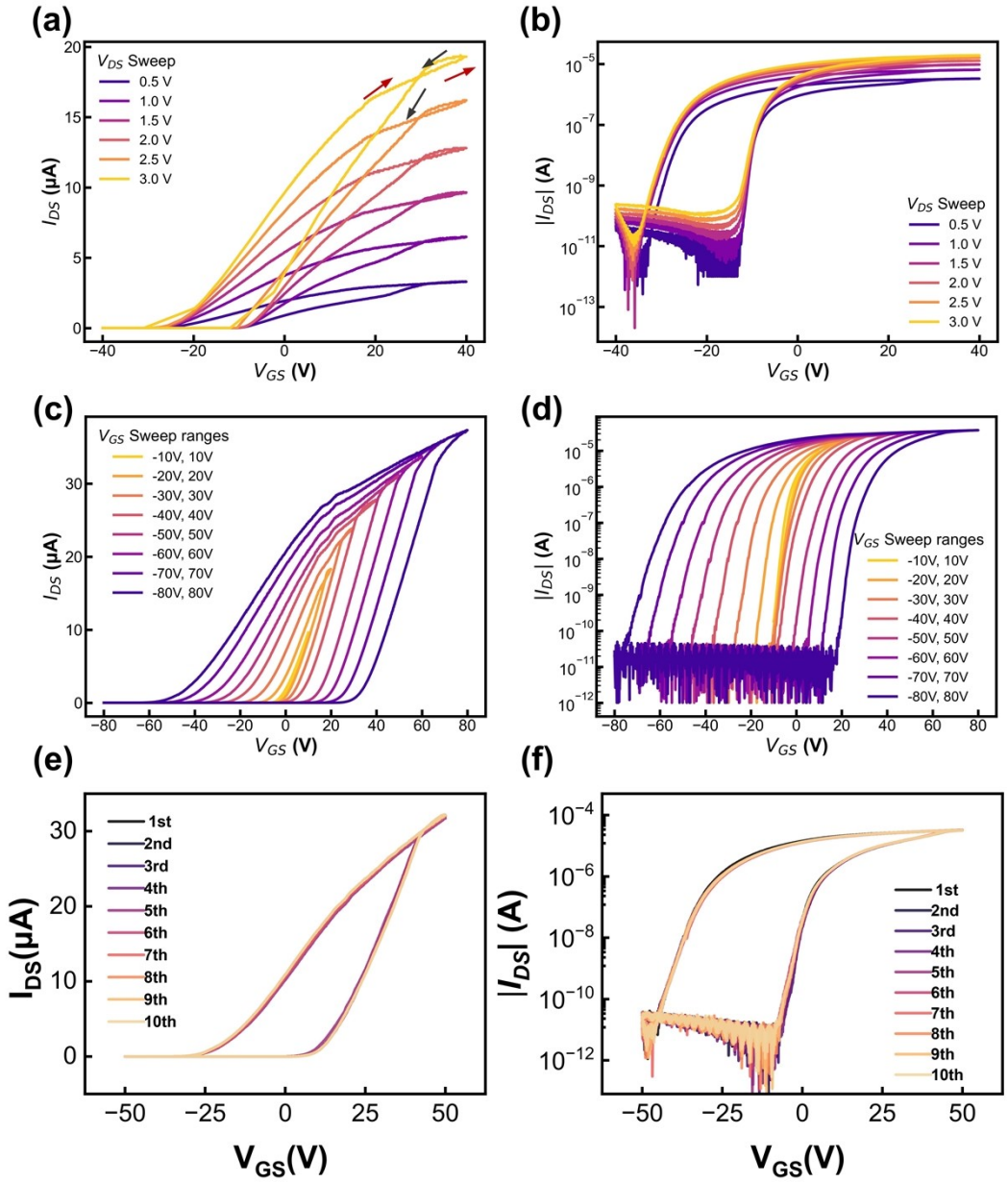

Figure S13. Hysteresis curves showing competing hysteresis features from another two-cycle contact-etched MoS_2 device. (a, b) Linear- and logarithmic-scale hysteresis curves measured at different V_{DS} values from 0.5 to 3.0 V. (c, d) Linear- and logarithmic-scale hysteresis curves measured under different bidirectional gate-voltage sweep ranges from ±10 V to ±80 V. (e, f) Ten consecutive hysteresis scans displayed on linear and logarithmic scales, respectively.

In panels (a) and (c), the hysteresis loops are predominantly clockwise, while a weak reversed feature appears near the high-V_{GS} end, forming a local counterclockwise loop and giving rise to a faint figure-eight-like shape. The repeated scans in (e) and (f) show that this small counterclockwise hysteresis feature is reproducibly observed.

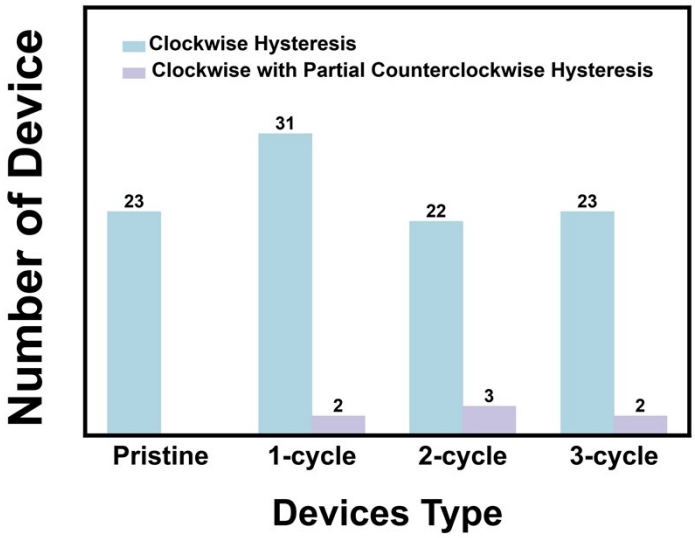

Figure S14. Statistics of hysteresis types for devices with different etching-cycle numbers. The numbers of devices exhibiting purely clockwise hysteresis and clockwise hysteresis with a partial counterclockwise feature are summarized for pristine, one-cycle, two-cycle, and three-cycle devices. The numbers of analyzed devices are 23, 33, 25, and 25 for the pristine, one-cycle, two-cycle, and three-cycle devices, respectively. Purely clockwise hysteresis is the dominant behavior in all groups, whereas devices showing a partial counterclockwise component account for only a small fraction of the etched devices. No such mixed hysteresis feature is observed in the pristine devices.

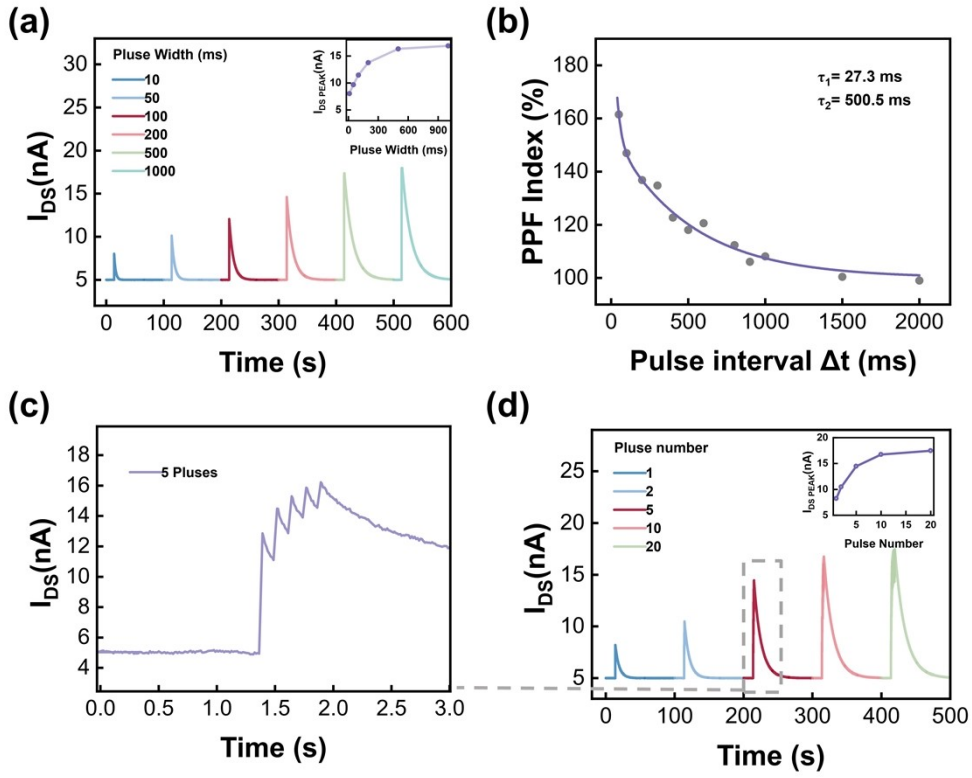

Figure S15. Pulse-modulated synaptic response of the pristine MoS_2 FET. (a) Transient current response to single gate pulses with different pulse widths; inset: extracted peak current as a function of pulse width. (b) PPF index as a function of pulse interval (Δt), together with a bi-exponential fit. (c) Transient response under five consecutive pulses. (d) Transient current response under repeated pulses with different pulse numbers; inset: extracted peak current as a function of pulse number. The pulse measurements were performed at V_{DS} = 1 V.

Table S1. Comparison of representative MoS_2-based devices modified by plasma treatment and related MoS_2-based synaptic devices.

Ref.	Treatment Species	Modified region	Main function	Processing Parameter	Device configuration	Representative device metrics
Our work	CF_4/Ar (1:1) Plasma	Contact region	Hybrid top/edge contact, ion-related modification, defect engineering	RIE Power: 27 W Time: 7 s Flow rate: 50 sccm Pressure: 30 mTorr	Si/SiO_2 back-gated few-layer MoS_2 FET	μ_{FE}: 142.4 $cm^2V^{-1}s^{-1}$, R_C: 1.15 kΩ·μm, N_{it}: 6×10^{12} cm^{-2}, I_{on}: 366 μA μm^{-1}, ΔV_{TH}: 95.25 V at V_G sweep from −80 to 80 V, τ_1 = 32.4 ms, τ_2 = 932.6 ms, PPF = 212%
1	CF_4 Plasma	Contact region	Ion implantation	RIE Power: 18 W Time: 5 s Flow rate: 50 sccm	Si/SiO_2 back-gated few-layer MoS_2 FET	I_{on}/I_{off}: 10^7-10^8, μ_{FE}: 15.1 $cm^2V^{-1}s^{-1}$, R_C: 1.96 kΩ·μm I_{on}: 90-130 $\mu A\cdot\mu m^{-1}$
2	Ar Plasma	Contact region	S-vacancy engineering, cleaning	Mild Ar plasma Power: 6 W Time: 35 s Flow rate: 12 sccm	Si/SiO_2 back-gated monolayer MoS_2 FET	I_{on}/I_{off}: 4×10^9, μ_{FE}: 153 $cm^2V^{-1}s^{-1}$, R_C: 1.7 kΩ·μm, I_{on}: 342 μA μm^{-1}
3	Ar Plasma	Contact region	Edge contact	ICP -	HfO_2/Si back-gated monolayer MoS_2 FET	I_{on}/I_{off}: 6×10^7, SS: 150 mV/dec, R_C: 1.25 kΩ·μm, I_{on}: 436 μA μm^{-1}
4	Ar Plasma	Contact region	Edge contact	Ion beam source Ion energy: 600 eV	SiO_2/Si back-gated monolayer/3L MoS_2 FET	R_C: 30.5 kΩ·μm, n_{2D} =1.2×10^{13} cm^{-2}
5	Ar Plasma	Contact region	Edge contact	End-Hall ion source Time: 300 s	SiO_2/Si back-gated monolayer/ few-layer MoS_2 FET	I_{on}/I_{off} ratio: 10^8, μ_{FE}: 38 $cm^2V^{-1}s^{-1}$, R_C: 200 kΩ·μm

6	Ar/O_2 (1:4) Plasma	Contact region	Ambipolar transport, Schottky barrier tailoring	ICP Power: 100 W Time: 30 s Pressure: 3×10^{-3}mbar.	SiO_2/Si back-gated few-layer MoS_2 FET	I_{on}/I_{off} ratio: 10^3, μ_{FE}: 30 $cm^2V^{-1}s^{-1}$, Schottky barrier height: 0.58 eV, Device resistance: 1.7 MΩ
7	FG (5% H_2 in N_2) Plasma	MoS_2/ high-k dielectric interface	High-k dielectric integration, surface passivation	ALD: remote forming gas plasma Time:60s	Al_2O_3 top-gated few-layer MoS_2 FET	I_{on}/I_{off} ratio: 10^9, μ_{FE}: 45.03 $cm^2V^{-1}s^{-1}$, SS: 85 mV/dec
8	O_2 Plasma	MoS_2 channel/ contact region	Phase transition	ICP Power: 7.2 W DC: 10 mA Time: 30 s Pressure: 5 mTorr.	SiO_2/Si back-gated few-layer MoS_2 FET	I_{on}/I_{off} ratio: 10^4, μ_{FE}: 237 $cm^2V^{-1}s^{-1}$, R_C: 4 kΩ·μm, Conductivity: 83.8 S m^{-1}
9	BCl_3 Plasma	MoS_2/high-k dielectric interface	Doping, High-k dielectric integration	ICP Power: 250 W Time: 300 s Pressure: 2.1 mTorr.	Al_2O_3 top-gated few-layer MoS_2 FET	I_{on}/I_{off} ratio: 10^6, μ_{FE}: 9 $cm^2V^{-1}s^{-1}$, SS: 140 mV/dec
10	SF_6 Plasma	MoS_2 channel	Etching，doping	Power: 10 W Time: 30–50 s Flow: 10 sccm Pressure: 1 Torr	SiO_2/Si back-gated monolayer MoS_2 FET	I_{on}/I_{off} ratio: 1.3 × 10^7 μ_{FE}: 16.2 $cm^2\cdot V^{-1}\cdot s^{-1}$
11	Ar Plasma	MoS_2 channel	S-vacancy defect	Plasma cleaner Power: 10 W Time: 5 s Pressure: 0.3 mbar	SiO_2/Si back-gated monolayer MoS_2 memristive/ synaptic FET	I_{on}/I_{off} ratio: 1.3 × 10^7 NLF: 2.81 MNIST accuracy: 97%
12	Toluene vapor	Whole devices	S-vacancy defect	Time: 20 min Flow rate: 10 sccm Pressure: 10^{-2} Torr Temperature: 350–450 °C	Vertical MoS_2 synaptic device with MoS_2 sandwiched between top and bottom electrodes	τ_1 = 49.8 ms, τ_2 = 265 ms, PPF: 170%

13	O_2 Plasma	Graphdiyne (GDY)	Etching, defect engineering	-	Graphdiyne /SiO_2/Si back-gated monolayer MoS_2 synaptic FET	I_{on}/I_{off}: 8×10^7, ΔV_{TH}: 90 V at V_G sweep from −80 to 80 V

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