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Supplemental Material for High-Performance p-Type MOSFETs Based on Janus MoSTe for Sub-5 nm CMOS Scaling

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1. The test of doping concentration for the Janus MoSTe MOSFETs

To achieve the most effective carrier injection, we calculated on-current (I_{on}) and subthreshold swing (SS) for high-performance (HP) in several doping concentrations of the Janus MoSTe FETs. Accordingly, five different doping concentrations (2.5×10^{13} e/cm^2 to 1.25×10^{14} e/cm^2 with an increment of 2.5×10^{13} e/cm^2) at the 3.2 nm gate length (L_g) MoSTe FETs with 1nm underlap (L_{UL}) have been investigated. To determine the optimal doping concentration for devices at the sub-5 nm scale with higher precision and with respect to SS, we carried out refined calculations over the range 5×10^{13} e/cm^2 to 7.5×10^{13} e/cm^2 with increments of 1×10^{13} e/cm^2, as illustrated in the inset of Figure S1. From these calculations we concluded that the optimal doping concentration for sub-5 nm devices is 7×10^{13} e/cm^2.

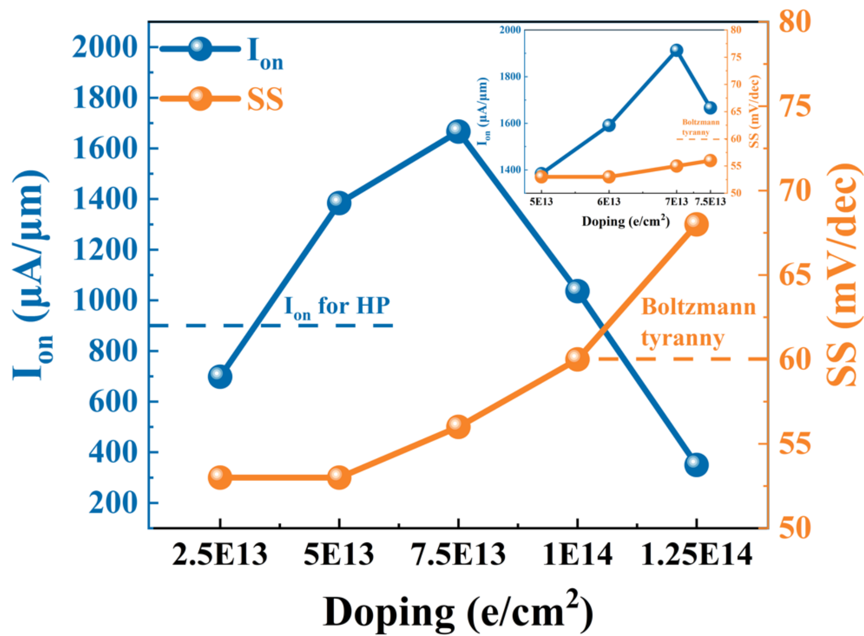

Figure S1. Dependence of the on-state current (I_{on}) and subthreshold swing (SS) on doping concentration for the Janus MoSTe device with L_g = 3.2 nm and L_{UL} = 1 nm. Inset: a more finely resolved selection of doping concentrations.

2. The transport properties of MoSTe MOSFETs with different gate lengths

Table S1. Benchmark of the ballistic performance upper limit of the sub-5 nm Janus MoSTe MOSFETs against the ITRS requirements for HP devices in 2028 (2013 version). I_{on} (μA/μm): the on-state current. SS (mV/dec): the subthreshold swing. C_g (fF/μm): the gate capacitance. τ (ps): the intrinsic delay time. PDP (fJ/μm): the power dissipation.

	L_g (nm)	L_{UL} (nm)	SS (mV/dec)	I_{on} (μA/μm)	I_{on} /I_{off}	C_g (fF/μm)	τ (ps)	PDP (fJ/μm)
	5	0	66.86	2234	2.23×10^4	0.5608	0.160	0.230
		1	50.02	1925	1.92×10^4	0.5155	0.171	0.211
		2	48.94	1194	1.19×10^4	0.4256	0.228	0.174
		3	44.3	665	6.65×10^3	0.3445	0.331	0.141
	3	0	92.02	1934	1.93×10^4	0.5355	0.177	0.219
		1	57.05	1901	1.90×10^4	0.5335	0.179	0.218
		2	50.42	923	9.24×10^3	0.3973	0.275	0.162
		3	44.88	528	5.29×10^3	0.2987	0.362	0.122
	1	0	437.07					
		1	136.54	519	5.2×10^3	0.3312	0.408	0.135
		2	98.59	484	4.84×10^3	0.2955	0.391	0.121
		3	73.68	419	4.19×10^3	0.2495	0.381	0.102
ITRS	5.1			900	9.00×10^3	0.60	0.423	0.24

Table S2. Benchmark of the ballistic performance upper limit of the sub-1(0.34) nm Janus MoSTe MOSFETs against the ITRS requirements for HP devices in 2028 (2013 version). I_{on} (μA/μm): the on-state current. SS (mV/dec): the subthreshold swing. C_g (fF/μm): the gate capacitance. τ (ps): the intrinsic delay time. PDP (fJ/μm): the power dissipation.

	L_g (nm)	L_{UL} (nm)	SS (mV/dec)	I_{on} (μA/μm)	I_{on} /I_{off}	C_g (fF/μm)	τ (ps)	PDP (fJ/μm)
	0.34	1	89.304	576	5.76×10^3	0.32	0.3	0.093
		2	64.609	601	6.01×10^3	0.30	0.270	0.087
		3	61.711	603	6.01×10^3	0.262	0.235	0.075
ITRS	0.34			326	3.26×10^3	0.26	0.424	0.07

Table S3. Benchmark of the ballistic performance upper limit of the sub-5 nm Janus MoSTe MOSFETs against the ITRS requirements for LP devices in 2028 (2013 version). I_{on} (μA/μm): the on-state current. SS (mV/dec): the subthreshold swing. C_g (fF/μm): the gate capacitance. τ (ps): the intrinsic delay time. PDP (fJ/μm): the power dissipation.

	L_g (nm)	L_{UL} (nm)	SS (mV/dec)	I_{on} (μA/μm)	I_{on}/I_{off}	C_g (fF/μm)	τ (ps)	PDP (fJ/μm)
	5	0	66.86	1393	2.79×10^7	0.5608	0.257	0.230
		1	50.02	1093	2.19×10^7	0.5155	0.302	0.211
		2	48.94	677	1.35×10^7	0.4256	0.402	0.174
		3	44.30	409	8.2×10^6	0.3445	0.539	0.141
	3	0	92.02	208	4.17×10^6	0.5355	1.647	0.21
		1	57.05	772	1.54×10^7	0.5335	0.442	0.218
		2	50.42	555	1.11×10^7	0.3973	0.458	0.162
		3	44.88	436	8.73×10^6	0.2987	0.438	0.122
	1	0	437.07					
		1	136.54					
		2	98.59	113	2.27×10^6	0.2955	1.673	0.121
		3	73.68	166	3.33×10^6	0.2495	0.962	0.102
ITRS	5.1			295	5.9×10^6	0.69	1.493	0.28

Table S4. Benchmark of the ballistic performance upper limit of the sub-1(0.34) nm Janus MoSTe MOSFETs against the ITRS requirements for LP devices in 2028 (2013 version). I_{on} (μA/μm): the on-state current. SS (mV/dec): the subthreshold swing. C_g (fF/μm): the gate capacitance. τ (ps): the intrinsic delay time. PDP (fJ/μm): the power dissipation.

	L_g (nm)	L_{UL} (nm)	SS (mV/dec)	I_{on} (μA/μm)	I_{on}/I_{off}	C_g (fF/μm)	τ (ps)	PDP (fJ/μm)
	0.34	1	89.304	216	1.98×10^6	0.32	0.8	0.093
		2	64.609	498	4.57×10^6	0.30	0.325	0.087
		3	61.711	424	3.89×10^6	0.262	0.334	0.075
ITRS	0.34			59	5.41×10^5	0.26	2.354	0.07

3. Cold-Source Effect Analysis

To further elucidate the physical origin of the steep-slope switching in our MoSTe FET, we conducted a comprehensive evaluation of the energy-resolved carrier concentration distributions at both the source and drain electrodes. The analysis was performed on a representative device configuration with a gate length (L_g) of 5 nm and an underlap (UL) region of 2 nm (SS_{min} = 40 mV/dec at V_g = 1.1 V). The fundamental requirement for a cold-source effect is a sharp truncation or bandgap in the source density of states (DOS) near the Fermi level, which would artificially cut off the high-energy thermal tail of injected carriers, leading to a super-exponential decay.

To verify this, we calculated the injected hole distribution, $n_h(E)$, which is the product of the local density of states (DOS) and the Fermi-Dirac distribution ($f_h(E)$). As shown in the source-side analysis (**Figure S2**), the DOS of the p-type MoSTe remains highly continuous and abundant below the source Fermi level (μ_S). Consequently, the injected hole distribution $n_h(E)$ (purple/pink curve) perfectly adheres to the standard exponential decay of the thermal distribution $f_h(E)$ (light blue curve). The absence of any truncation or super-exponential drop in the thermal tail provides definitive physical evidence that the source material does not act as an energy filter. Therefore, the cold-source effect is unequivocally ruled out.

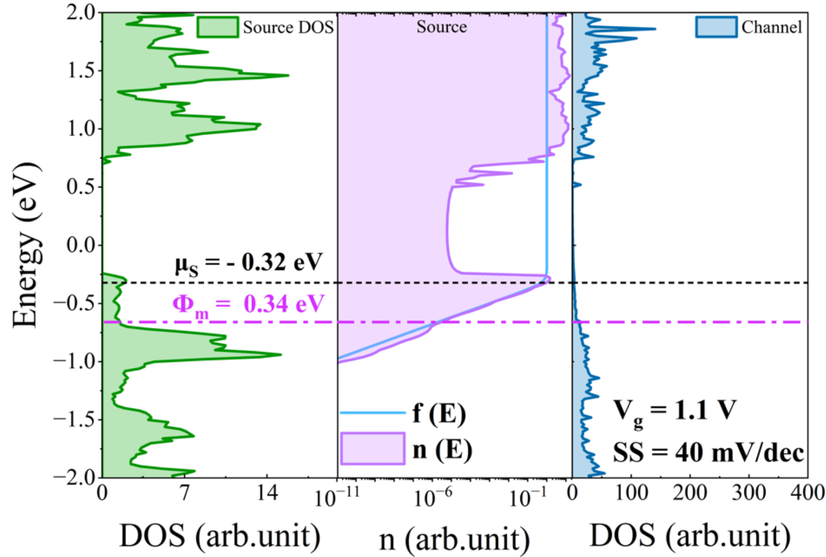

Figure S2. Energy-resolved electronic states and carrier distribution at the source side of the MoSTe FET. The left and right panels display the Local Density of States (DOS) for the source and channel regions, respectively. The central panel illustrates the energy-resolved hole distribution on a logarithmic scale. The light blue curve represents the standard Fermi-Dirac distribution for holes, $f_h(E)$, while the purple curve with the shaded area denotes the actual injected hole distribution, $n_h(E)$. The horizontal dashed line marks the source Fermi level, and the magenta dash-dot line indicates the effective barrier height (Φ_m = 0.34 eV) towards the channel.

Furthermore, to strictly exclude any potential cold-source effect originating from the drain, we

conducted an identical carrier distribution analysis at the drain electrode. As illustrated in **Figure S3**, the same phenomenon is observed: there is no obvious super-exponential distribution region truncating the thermal tail. Consequently, the energy-resolved carrier distribution profiles from both the source and drain electrodes collectively verify the absolute absence of the cold-source effect in our device.

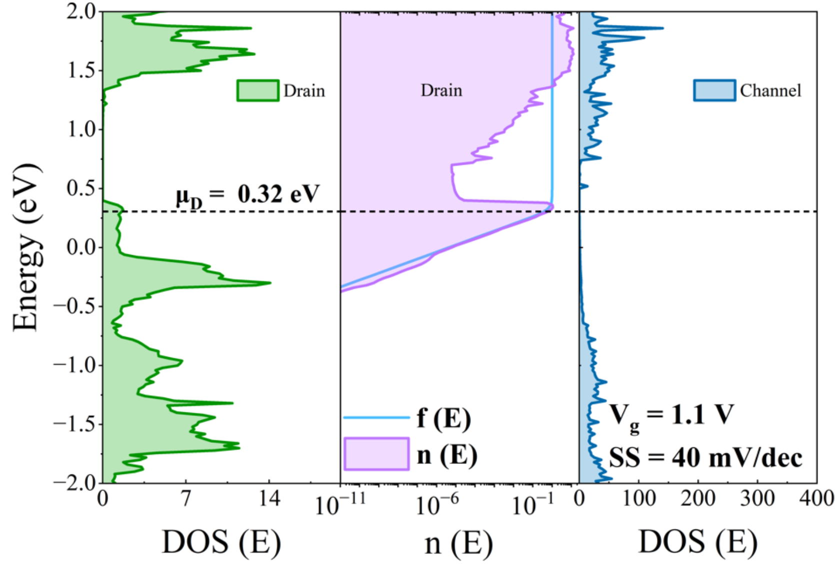

Figure S3. Energy-resolved electronic states and carrier distribution at the drain side of the MoSTe FET. The left and right panels display the Local Density of States (DOS) for the drain and channel regions, respectively. The central panel illustrates the energy-resolved hole distribution on a logarithmic scale. The light blue curve represents the standard Fermi-Dirac distribution for holes, $f_h(E)$, while the purple curve with the shaded area denotes the actual injected hole distribution, $n_h(E)$.

4. Transfer Characteristics and Performance Limits of n-type Devices

While our results demonstrate that the p-type MoSTe device exhibits exceptional performance, fulfilling the stringent ITRS requirements even at the extreme sub-nanometer scale, it is essential to concurrently evaluate its n-type counterpart, as practical CMOS technology fundamentally relies on complementary operation. To this end, we first evaluated the I-V characteristics of an n-type MoSTe FET at a 3 nm gate length (L_g = 3 nm) with a 1 nm underlap (L_{UL} = 1 nm). As shown in **Figure S4**, across a wide range of doping concentrations, the on-state current (I_{on}) consistently fails to meet the ITRS high-performance requirement of 900 μA/μm. Furthermore, as shown in **Figure S5**, we extended our investigation to an ultimate scaling limit of L_g = 0.34 nm with varying underlap lengths (L_{UL} = 1, 2, and 3 nm). The simulated results corroborate that, although increasing L_{UL} effectively improves electrostatic control, the maximum I_{on} for the n-type device remains strictly below the ITRS targets.

However, rather than undermining the viability of MoSTe, this intrinsic limitation in n-type transport paradoxically underscores its unique superiority as a specialized p-channel material. Therefore, we propose that the true potential of Janus MoSTe lies not in serving as a universal, standalone material for both polarities, but rather in advanced heterogeneous CMOS integration. By pairing a high-performance p-type MoSTe channel with an alternative, intrinsically optimized n-type 2D material (such as MoS_2), we can pave a highly promising pathway for next-generation sub-nanometer logic circuits.

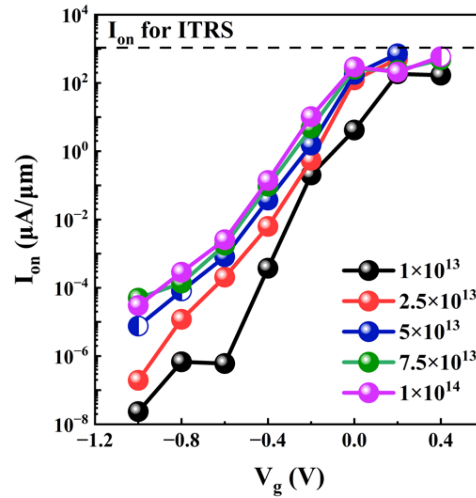

Figure S4. I–V characteristics of an n-type Janus MoSTe FET with a gate length of 3 nm and an underlap region (L_{UL}) of 1 nm, under different doping concentrations (e/cm²). Half-filled data points indicate currents that have not converged at the corresponding gate voltage.

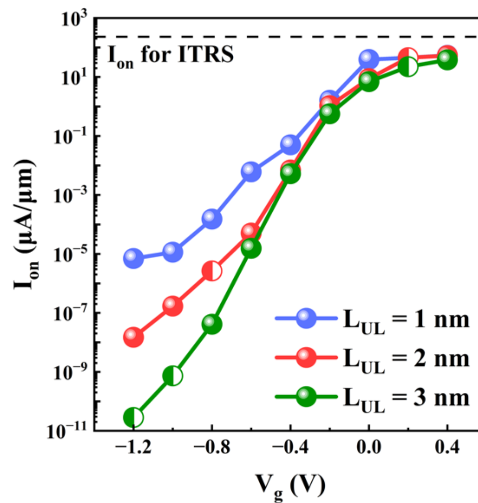

Figure S5. Simulated transfer characteristics of the n-type MoSTe MOSFET at an extreme scaling limit. Half-filled data points indicate currents that have not converged at the corresponding gate voltage.

5. Hole effective masses of monolayer MoSTe along the zigzag and armchair directions.

Table S5. Hole effective masses of monolayer MoSTe along the zigzag and armchair directions.

Zigzag	Armchair
3.667 m_0	3.673 m_0

Given that the anisotropy of carrier effective mass plays a pivotal role in determining the transport performance of devices[1][2], we explicitly evaluated the directional dependence of the charge carriers. Accordingly, Table S5 summarizes the calculated hole effective masses (m_h^*) of the MoSTe monolayer along the two principal in-plane crystallographic orientations. Our first-principles calculations yield m_h^* values of 3.667 m_0 and 3.673 m_0 along the zigzag and armchair directions, respectively. This negligible difference indicates highly isotropic transport behavior within our specific device model. This isotropy originates from the nearly identical band dispersions around the Γ point along the Γ-X (zigzag) and Γ-Z (armchair) paths. As illustrated in **Figure S6**, we have highlighted the band structure around the valence band maximum (VBM) with green rectangles. Physically, the effective mass is inversely proportional to the second derivative of energy with respect to the wave vector (i.e., the band curvature). Since the VBM of MoSTe is located exactly at the Γ point, the band structure in this highlighted vicinity governs the effective mass. Consequently, the symmetric band dispersions along Γ-X and Γ-Z directly result in the highly similar hole effective masses observed in the zigzag and armchair directions.

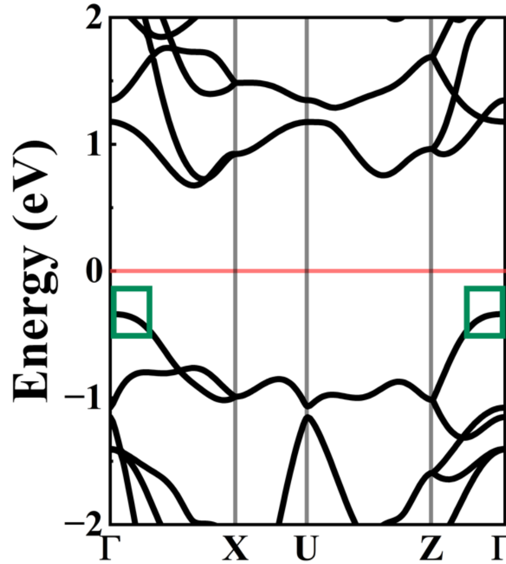

Figure S6. Band structure of monolayer MoSTe in the orthorhombic phase. The band dispersion around the valence band maximum (VBM) is highlighted by the green rectangles.

6. Performance of MoSTe FETs Against Analogous Janus TMDs FETs.

Table S6. Quantitative comparison of device performance metrics between MoSTe and other representative Janus TMD-based MOSFETs.

	L_g (nm)	SS (mV/dec)	I_{on} (μA/μm)
MoSTe	5	66.86	2234
MoSSe [3]	5.1	93.0	304
WSSe [3]	5.1	101.1	1027
WSeTe [4]	5.1	/	1146
ITRS	5.1	/	900

To comprehensively contextualize our work and substantiate the unique advantages of Janus MoSTe, we benchmarked the transport metrics of our p-type MoSTe MOSFETs against other representative Janus transition metal dichalcogenide (TMD) devices at the 5 nm technology node. As summarized in **Table S6**, recent theoretical investigations into n-type WSSe and MoSSe MOSFETs (L_g = 5.1 nm) reported maximum on-state currents (I_{on}) of 1027 μA/μm and 304 μA/μm, respectively. Furthermore, their gate electrostatics are severely compromised at this scale, exhibiting degraded subthreshold swing (SS) values of 101.1 mV/dec and 93.0 mV/dec, which are indicative of severe short-channel effects. Similarly, in-plane Janus WSeTe Schottky-barrier FETs yield a limited I_{on} of 1146 μA/μm even when utilizing optimized 1T-phase metallic electrodes.

7. Impact of Uniaxial Strain Engineering on Device Performance

While the underlap (UL) design effectively mitigates short-channel effects, it inherently increases the total physical footprint of the device. To explore footprint-neutral optimization strategies—which are critical for sub-1 nm CMOS scaling—we systematically investigated the impact of uniaxial strain engineering on the transport properties of the MoSTe MOSFET. The simulations were performed on a baseline p-type device configuration featuring a gate length (L_g) of 0.34 nm and a moderate underlap (L_{UL} = 1 nm).

The application of uniaxial strain fundamentally alters the electronic band structure of the Janus MoSTe monolayer, as illustrated in **Figure S7**. Our calculations indicate an asymmetric response of the bandgap to the applied strain. Specifically, compressive strain induces an expansion of the bandgap, which elevates the transport barrier in the channel region and subsequently leads to a suppression of the on-state current (I_{on}). Conversely, the application of tensile strain effectively narrows the bandgap. This bandgap reduction lowers the energy barrier, facilitating more efficient carrier injection from the source to the channel and resulting in a substantial increase in I_{on}. The modulation of the electronic structure directly translates into the transport characteristics of the device, as demonstrated by the I-V curves under various strain conditions (**Figure S8**). The introduction of tensile strain significantly enhances the device performance, aligning seamlessly with the objective of maximizing drive current without extending the channel footprint. Under optimal tensile strain conditions, the I_{on} reaches a maximum value of 681 μA/μm.

This result highlights the superiority of strain engineering over pure geometric modifications for this system. For comparison, the highest I_{on} achieved through the original underlap strategy alone was 603 μA/μm (obtained with a significantly larger L_{UL} of 3 nm at L_g = 0.34 nm, as detailed in **Table S2**). Consequently, strain engineering provides a highly effective alternative, offering a significantly higher I_{on} without incurring the spatial penalty associated with extended underlap regions, thereby demonstrating its exceptional suitability for optimizing ultra-scaled MoSTe devices.

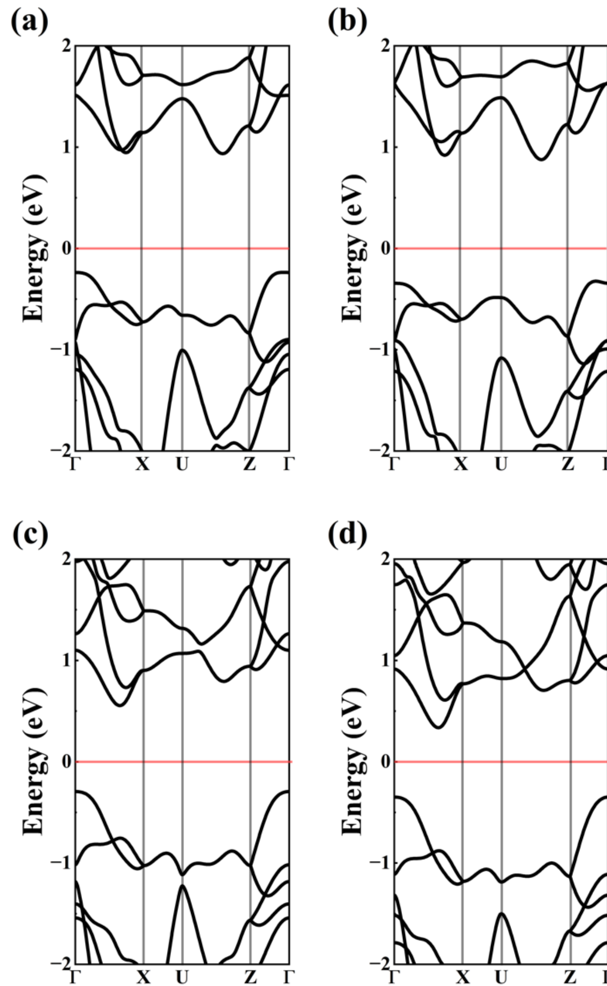

Figure S7. The band structures of monolayer MoSTe subjected to 2% and 4% compressive strain are presented in (a) and (b), respectively, whereas those under 2% and 4% tensile strain are shown in (c) and (d), respectively.

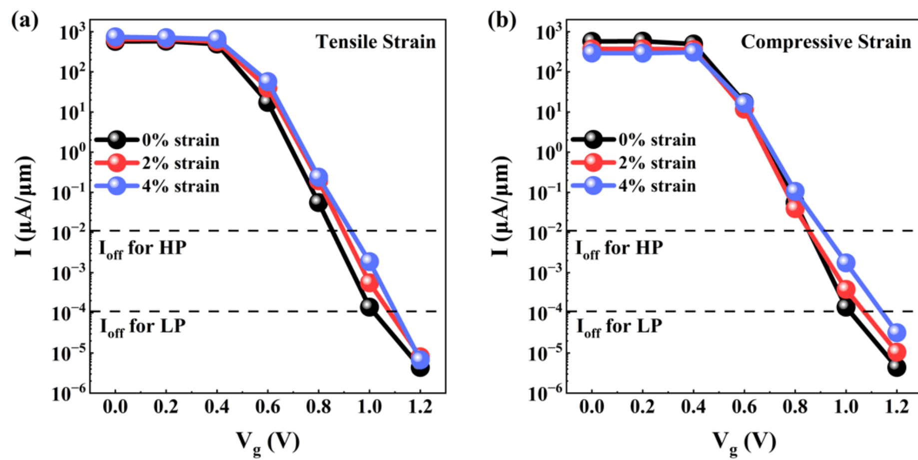

Figure S8. (a) I-V curves under tensile strain, and (b) under compressive strain, respectively.

8. Analytical Modeling of Sub-thermionic Subthreshold Swing via Quantum Tunneling

In our ultra-short channel MoSTe devices, the subthreshold swing (SS) is observed to fall below the conventional room-temperature thermionic limit of 60 mV/dec. This sub-thermionic behavior is fundamentally driven by pronounced quantum tunneling effects inherently present at the few-nanometer scale, rather than contributions from negative capacitance or source-drain tunneling filtering. Further details are elaborated as follows:

1. The Conventional Thermionic Limit (Boltzmann's Tyranny)

In a conventional MOSFET, carrier transport is primarily driven by thermal injection (thermionic emission). The Boltzmann tail of the semiconductor band distribution imposes a fundamental thermionic limit on the switching efficiency. Under the thermionic-only assumption, the subthreshold swing (SS) is expressed as:

$$SS = \frac{dV_G}{d\log_{10} I_D} = \frac{dV_G}{d\psi_s}\frac{d\psi_s}{d\log_{10} I_D} \cong \left(1+\frac{C_d}{C_{ox}}\right)\ln 10\frac{kT}{q},$$

where ψ_s is surface potential, kT/q is the thermal voltage, and C_d and C_{ox} represent the depletion and the oxide capacitances, respectively. If temperature is selected as 300 K, $\ln 10\frac{kT}{q}$ would be around 60 mV/dec. That is, SS has a lower limit 60 mV/dec at room temperature.

2. Breaking the Limit via Tunneling Mechanism

In this work, since the channel length is sub-5 nm, the tunneling current cannot be neglected. As a result, the expression of SS needs to be modified as

$$SS = [r_{\text{tunnel}} SS_{\text{tunnel}}^{-1} + (1-r_{\text{tunnel}}) SS_{\text{therm}}^{-1}]^{-1},$$

where $SS_{\text{tunnel}} = \frac{\partial V_G}{\partial \lg I_{\text{tunnel}}}$, $SS_{\text{therm}} = \frac{\partial V_G}{\partial \lg I_{\text{therm}}}$, $r_{\text{tunnel}} = \frac{I_{\text{tunnel}}}{I_D}$ and I_D is the total current, or $I_{\text{therm}} + I_{\text{tunnel}}$. Because r_{tunnel} is the ratio of I_{tunnel} in I_D, it is in the range between 0 and 1, and the SS should meet the following condition that

$$\frac{1}{SS} = \frac{r_{\text{tunnel}}}{SS_{\text{tunnel}}} + \frac{1-r_{\text{tunnel}}}{SS_{\text{therm}}} > \frac{1}{SS_{\text{therm}}},$$

or $SS < SS_{\text{therm}}$. Therefore, the inclusion of the tunneling effect allows the device to potentially surpass the Boltzmann thermionic limit of 60 mV/dec at room temperature. Our calculations show that the tunneling current is nonnegligible in the sub-5nm Janus MoSTe FET, which makes SS lower than 60 mV/dec, hence breaking the “Boltzmann’s tyranny”.[5-9]

9. Standardized Extraction Methodology for Channel Capacitance and Voltage Window

In our atomistic quantum transport simulations, the intrinsic gate capacitance (C_g) is a fundamental parameter for assessing the dynamic switching performance of the MoSTe MOSFET, including the intrinsic delay time (τ) and power-delay product (PDP). The capacitance per unit width is defined as the derivative of the total channel charge (Q_{ch}) with respect to the applied gate voltage (V_g):

$$C_{ch} = \frac{\partial Q_{ch}}{W \partial V_g}$$

Because the ultra-thin 2D channel acts as a space charge region, the total charge Q_{ch} can be quantitatively evaluated by summing the Mulliken charges across the entire channel for each gate voltage. However, the $Q_{ch} - V_g$ transfer curve is inherently nonlinear. Consequently, the extracted C_g is highly dependent on the specific selection of the V_g operating point used for the slope fitting. To ensure a rigorous evaluation and allow for a fair benchmark against state-of-the-art literature, we strictly adopted the standardized methodology to determine the operational voltage window and extract C_g, which proceeds as follows:

1. Determination of Operational Voltage Window (V_{off} and V_{on}):

Following the performance criteria specified by the International Technology Roadmap for Semiconductors (ITRS), the off-state current (I_{off}) is initially fixed at a standardized target to identify the off-state gate voltage (V_{off}). For instance, I_{off} is anchored at 0.1 μA/μm for High-Performance (HP) devices and 5×10^{-5} μA/μm for Low-Power (LP) devices. With the supply voltage (V_b) set to a constant value (e.g., 0.64 V), the corresponding on-state gate voltage is then explicitly defined by the relationship:

$$V_{\mathrm{on}} = V_{\mathrm{off}} - V_b$$

2. Calculation of Channel Charge (Q_{ch}): We systematically calculate the total Mulliken charge (Q_{ch}) in the channel region under discrete gate voltages (V_g) ranging across the entire operational window from V_{off} to V_{on}.

3. Capacitance Extraction Strategy (C_g at V_{off}): Following conventional treatments widely validated in computational nanoelectronics, the representative gate capacitance is determined by fitting the linear slope of the Q_{ch}-V_g curve in the vicinity of V_{off} (denoted as $C_g(off)$). Extracting the slope around V_{off} precisely captures the onset of charge accumulation as the device transitions from the subthreshold regime to the on-state. This approach provides a reliable and conservative estimation of the effective gate control, avoiding the severe non-linear charge saturation at high overdrive voltages.[10-13]

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