Electronic Supplementary Material (ESI) for Energy & Environmental Science

Supporting Information

A novel wrap-around metal contact optimized for radial p-n junction wire solar cells

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Fig. S1 J-V curves for solar cells with (a) conventional planar grids, and (b) wrap-around wire contacts. Different cell sizes are compared for each scheme.

By employing the wrap-around contact design, we have intended to emphasize the realization of robust, reliable collection of charge carriers which is irrespective of varying the cell sizes and/or pattern design of metal grids. To specifically compare our wrap-around contact with conventional metal grids, we actually thought that too small area (<< 1 cm^2) samples which were difficult to fabricate metal grids on their tops were rather inappropriate because the fill factors for these small cells cannot sufficiently reflect the information affected by top-contact structure. For example, following I-V curves of planar Si solar cell with finger/bus bar electrodes (Fig. S1a) demonstrate the completely different I-V and fill factor behaviors due to different cell areas although they are identically fabricated, in which the small one was cut (for measurement with different grid design) right after the large one (sample size: 1×1 cm^2) had been measured. In general, the fill factors are degraded with increasing the sample sizes. In case of conventional top electrodes, therefore, metal grids (finger/bus bar) need to be optimized according to the cell sizes (Ref. H.B. Serreze, *13th IEEE Photovoltaic Specialists Conference*, Washington, D.C., USA, 1978). On the other hand, note that the I-V curves for the wrap-around contact cells are observed to be almost identical irrespective of the cell sizes (see Fig. S1b).

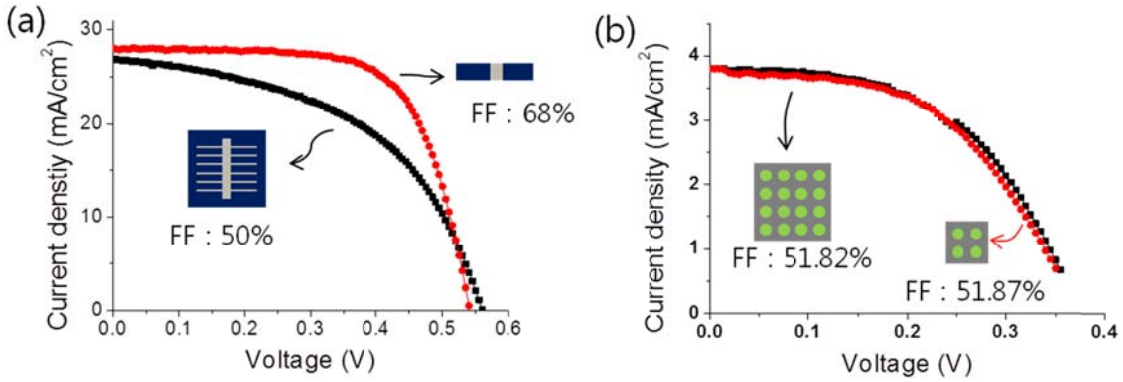
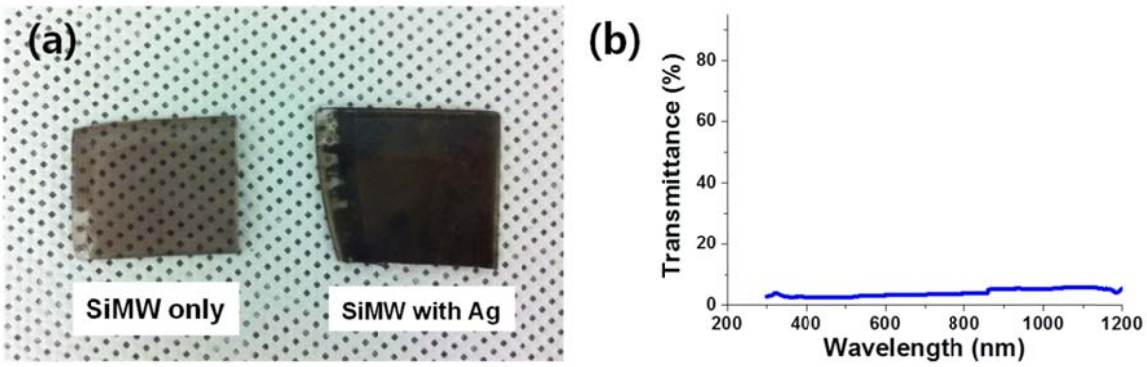


Fig. S2 (a) A digital photograph comparing transparency of two Si microwire samples embedded in PDMS, Si microwires only (left), Si microwires surrounded by wrap-around Ag contacts (right), and (b) transmittance spectra of the sample (right) in (a).



Our light absorptance (Fig. 1c) data were measured by using the wire arrays [Fig. S2(a)] detached from the substrate. However, the electrical properties were measured before removing from the substrate because we have confirmed that light absorption into a substrate was negligible [Fig. S2(b)]. After removing from the substrate, low transmittance of 3~4% was observed from the wire arrays containing Ag electrodes.

Fig. S3 Absorption spectra of PDMS. Low average absorption of ~0.8% was observed in the wavelengths from 400 nm and 1100 nm, but two peaks at short (<400 nm) and long (>1100) wavelengths were notable to reveal high absorption (>10%) of PDMS.

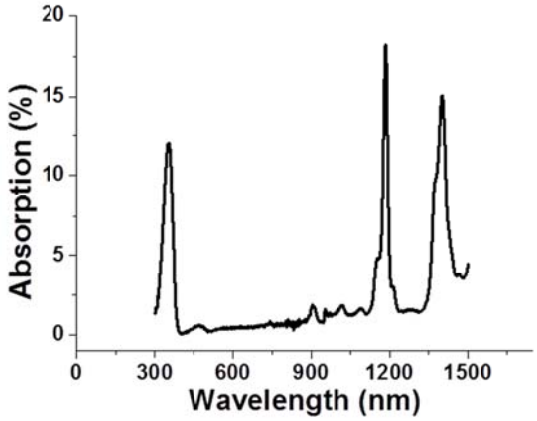
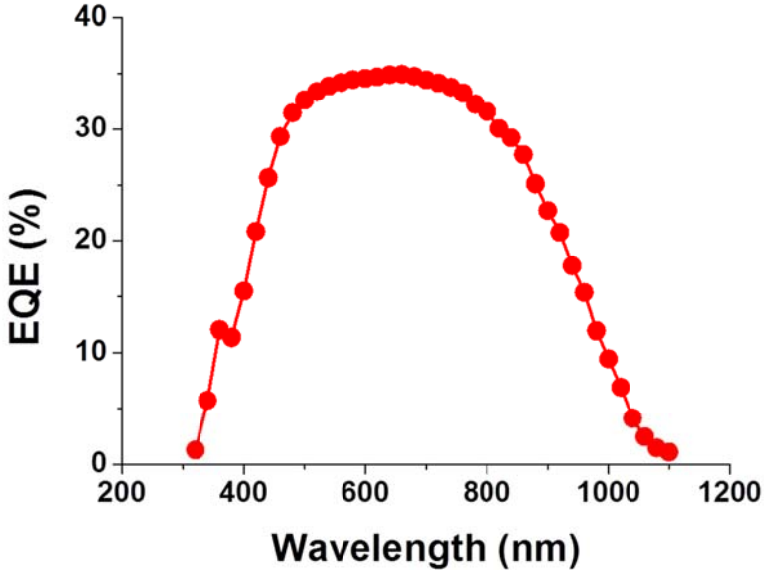


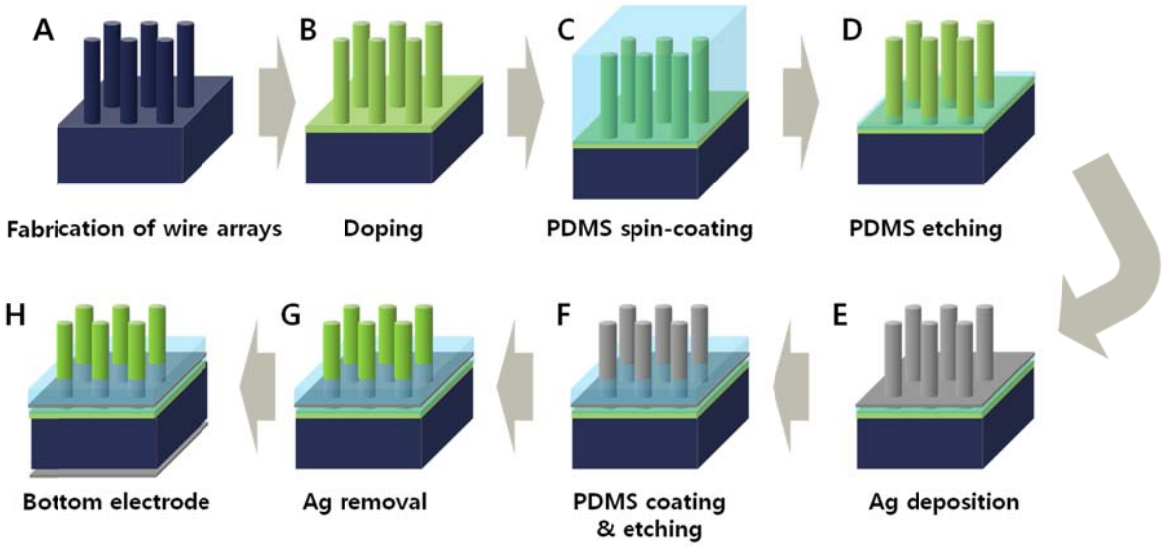
Fig. S4 External Quantum Efficiency (EQE) result of the wrap-around Ag contacted microwire sample which is measured in Fig. 2b.



The reasoning why the short circuit current was poorer than the light absorptance of ~80% was originated mostly from the fact that there was no surface passivation processes in our work, despite the remarkably increased surface-to-volume ratio because of the presence of a microwire-arrayed-absorber removed from the substrate.

The wire arrays were fabricated by RIE process causing severe plasma damage to the wire surfaces in which the RIE proceeded for long time in order to pattern 60-μm-long wires, which then resulted in degradation (~0.7 μs) in minority carrier life time.

Fig. S5 Schematics showing the overall process sequences for fabricating a Si microwire solar cell with wrap around Ag contacts (without detaching wires from the substrate).



Step A: A periodic array of silicon microwires

- An 1.5-μm-thick SiO_2 layer was deposited on a 8-inch n-doped (5 Ωcm), Si(100) wafer using high-density plasma chemical vapor deposition
- The substrate was patterned using low-level lithography and reactive ion etching in a mixture of CF_4 and CHF_3 plasma.
- Periodic SiO_2 dot arrays (2 μm in diameter) were used as etch masks. The plasma etching process, including etching (SF_6) and polymerization (C_4F_8) steps, was adopted to define the high aspect ratio Si microwire arrays.
- The wire pitch (a center-to-center distance in between microwires) and diameter were determined by the patterned size of a photo mask. Previous experimental work by *Park* et al.[10] described more details about this procedure.

Step B: Formations of a radial p–n junction and back surface field (BSF)

- A cost-efficient, conformal doping technique was employed to co-dope the top and bottom sides of a wafer using different dopants in one thermal cycle.
- This approach produces a high-efficiency p+nn+ structure across the thickness direction of a wafer, which concomitantly incorporates a radial p–n junction MWs on a front side and a BSF on backside.
- First, boron and phosphorus silicate precursors (B155 for B and P509 for P, supplied

by Filmtronics) were spin-coated on each dummy wafer.

- Then, the SOD dummy wafers were baked at 150 °C for 20 min. To form the BSF, a phosphorus-coated dummy wafer was directly contacted to the bottom side of a target wafer so as to degenerately dope boron into the backside.
- The boron-coated dummy wafer, however, was located in proximity mode on the front side of the target wafer to tailor the doping profile of boron diffusion.
- Simultaneous diffusion doping was carried out in a tube furnace under a mixed ambient of N_2 and O_2 at 900°C for 5 min. Previous work by *Jung* et al.[14] reported more details about this procedure.

Step C: Spin-coating of PDMS.

- A mixed solution (10:1 wt %) of PDMS base (sylgard 184) and curing agent was spin-coated on the wire arrays at 4000 rpm for 480 sec.
- To maintain the height of PDMS uniform, a solution should be stirred enough to cover whole sample surface prior to dropping for spin-coating.
- Then, the coated sample was cured at 80°C for 8 hrs. The vacuum oven was necessary to remove air bubbles originated from the mixing process of PDMS base with curing agent.
- A drastic change in temperature should be avoided because the PDMS film can be cracked due to the difference in thermal expansion coefficients. Previous work performed by *Putnam* et al.[4] reported more details about this procedure.

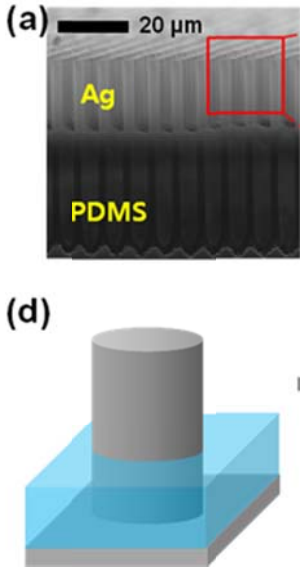
Step D: PDMS etching

- Spin-coated PDMS was etched using a solution of tetrabutylammonium fluoride (TBAF) mixed with dimethyl fluoride (DMF) in a 1:1 volume ratio. The etch rate was 10 μm/min, but was normally sensitive to temperature.
- A height of PDMS was variable by adjusting dipping time. After dipping in the solution, the sample was rinsed in DMF solvent. This process was to remove the PDMS residues on wire arrays.
- Then, cleaning using deionized (DI) water was conducted. This cleaning process was important because the PDMS residue was likely remained in between wire arrays.

Step E: Ag deposition

- Ag electrodes were thermally evaporated onto Si microwires in which the bottoms of wires were embedded in PDMS remained. The deposition rate was ~10Å/sec, and the metal thicknesses were varied from 100 to 1300 nm by adjusting deposition time.
- The reason why we coated Ag on top of PDMS remained at wire bottoms was to physically separate Ag electrode from the substrate while controlling the gap between the substrate and Ag. In our work, the gap (corresponding to the height of PDMS remained) was fixed at 10 μm.

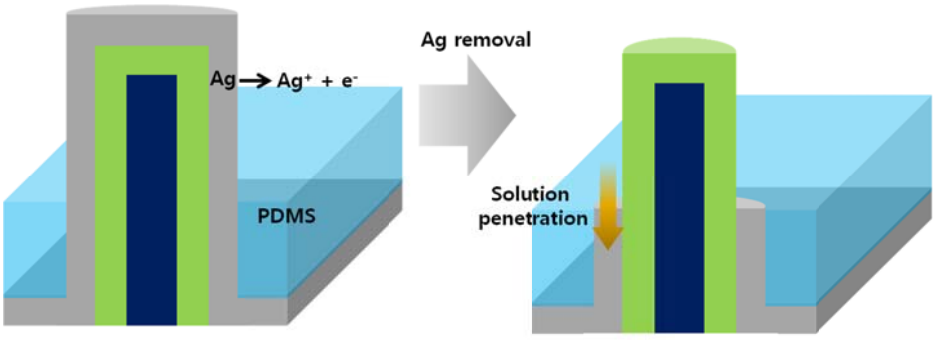
Step F: PDMS coating and etchback



- PDMS coating and etchback steps, i.e., steps C and D above, were repeated once again because we needed to protect a planar Ag layer, not sidewall-coated Ag.
- Then, the Ag-coated wire top and sidewalls were protruded out of PDMS [see left figures, Figs. S5(a) & (d)], in which the Ag in protruded parts could be selectively removed by wet etching.

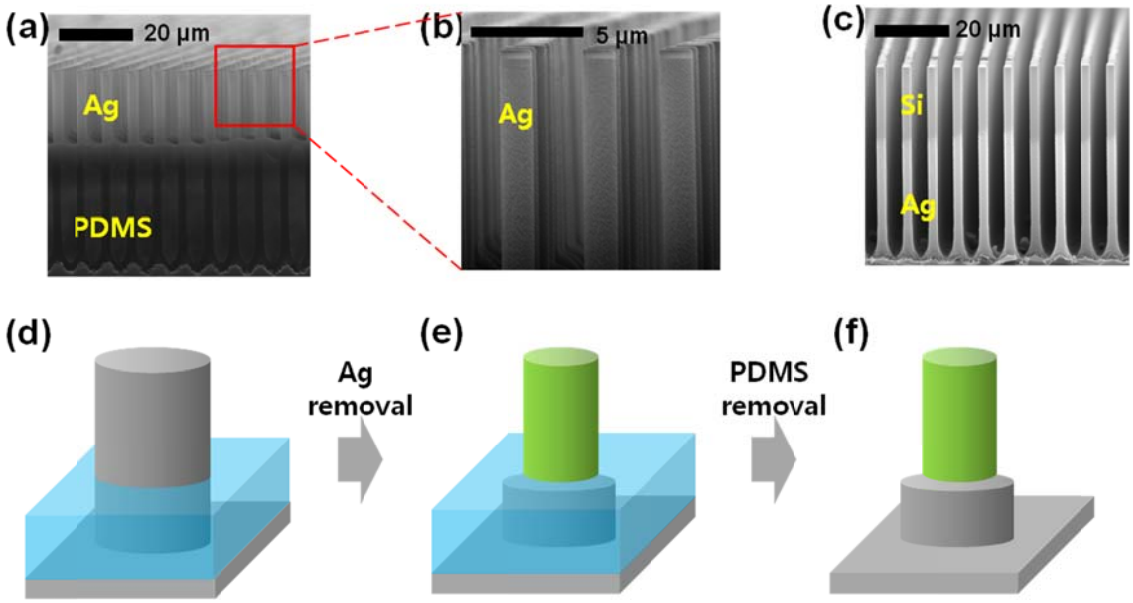
Step G: Selective Ag removal

- The Ag coated on protruded parts of wires was removed for 1 min using Ag etching solution (methanol : ammonia : hydrogen peroxide=4:1:1, volume ratio). Since the etching solution likely penetrated along the interface between Ag and PDMS, the etching time was required to precisely limit in order to prevent the overetching of Ag infiltrated into the interfacial region of PDMS/wire (see figures below).



Step H: Finally, the bottom contact was thermally deposited onto a back side of the solar cell.

Fig. S6 SEM images (a-c) describing how the contact height was adjusted by using PDMS coating and etchback processes. (d) Ag-coated-top regions of a microwire were protruded out of PDMS after etchback process; (e) selective removal of Ag; (f) wrap-around Ag contact formed after removal of PDMS. (d) and (f) correspond to (a) and (c), respectively.



Contact resistance of ITO/Si [Fig. 3(c)]

We extracted the contact resistance of ITO/Si while maintaining the same contact area compared to Ag/Si contacts. Contact resistance (R_c) is determined by:

$$R_c = \frac{\rho_c}{A} \quad \text{(eq. 1)}$$

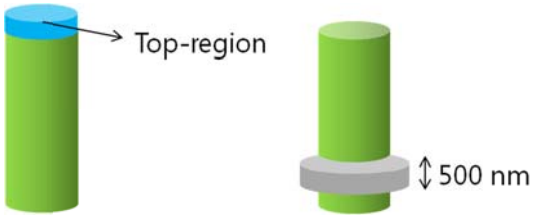
where ρ_c is contact resistivity, and A is contact area. The ρ_c of ITO/Si is 71.43×10^{-3} mΩ cm^2. A circular area of ITO/Si contact is directly compared with a sidewall area of a cylindrical Ag/Si contact where L denotes a height of a cylinder.

The wire tops are calculated by

$$A_{top-region} = \pi r^2 \quad \text{(eq. 2)}$$

where r is a wire radius of 1 μm. Note that the area of wire-top is equal to the contact area of Ag/Si when the L is 500 nm.

$$A\big|_{L=500nm} = 2\pi rL\big|_{L=500nm} \quad \text{(eq. 3)}$$



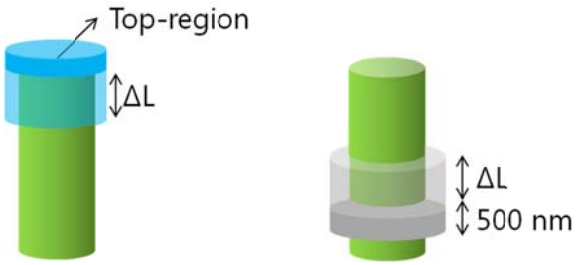
For this reason, a black dot connected with red dotted lines [Fig. 3(c)] stands for a planar R_c by ITO/Si, which corresponds to the same area formed by Ag/Si contact at L of 500 nm.

We can also calculate the Rc of ITO/Si when ITO attempts to three-dimensionally surround top-regions of microwires. The contact area can be described using L as follows:

$$\Delta A = 2\pi r \Delta L \quad \text{(eq. 4)}$$

$$A_{\text{ITO/Si}} = A_{\text{top-region}} + \Delta A \quad \text{(eq. 5)}$$

$$A_{\text{ITO/Si}} = A\big|_{L=500nm} + \Delta A = 2\pi rL\big|_{L=500nm} + 2\pi r\Delta L \quad \text{(eq. 6)}$$



where ΔA and ΔL stand for the extended contact area and contact height, respectively. By using the equations above, we could sum up the contact resistance of ITO/Si.

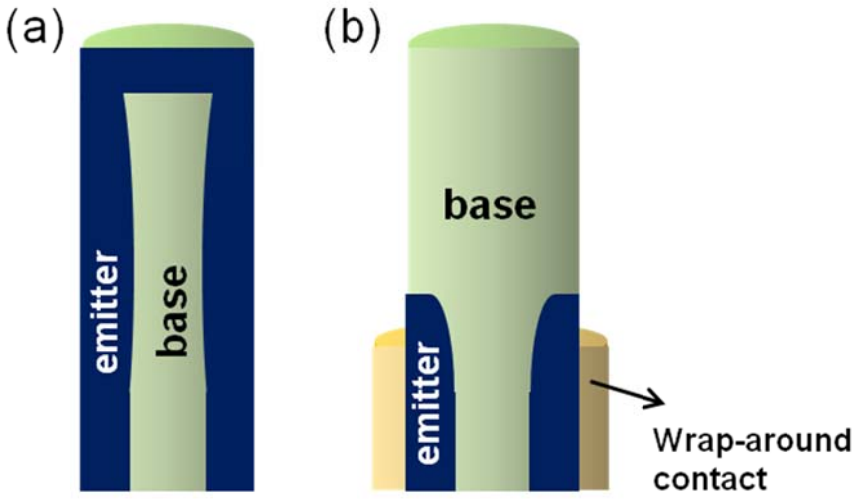
$$R_{c\_\mathrm{ITO/Si}} = \frac{\rho_{c\_\mathrm{ITO/Si}}}{A_{\mathrm{ITO/Si}}} \qquad \text{(eq. 7)}$$

$$R_{c\_\mathrm{ITO/Si}} = \frac{\rho_{c\_\mathrm{ITO/Si}}}{2\pi r\big|_{L=500nm} + 2\pi r\Delta L} \qquad \text{(eq. 8)}$$

To extract the contact resistance per unit cell area, the information of a cell area was necessary; then, the unit was converted from [Ω] into [Ω cm^2].

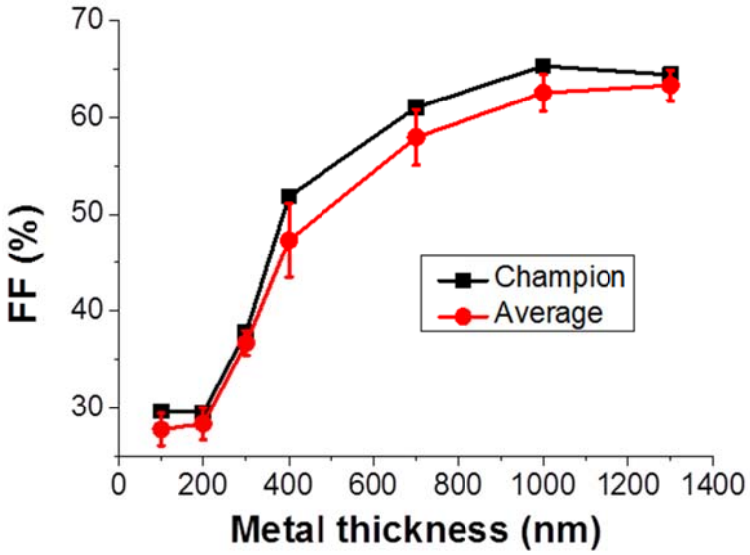
$$R_{c\_\mathrm{ITO/Si}} = \frac{\rho_{c\_\mathrm{ITO/Si}}}{2\pi r\big|_{L=500nm} + 2\pi r\Delta L} \times (\text{unit cell area}) \qquad \text{(eq. 9)}$$

Fig. S7 Schematics of (a) conventional radial p-n junction, and (b) selective emitter concept adopting wrap-around contacts



Radial p-n junction wire solar cells conventionally require a large amount of the emitter area, yielding high Auger recombination; thus, we need to find out how to effectively shallower the junction depth while reducing the emitter surface area. To make a junction depth shallower, plasma doping techniques[23] would be highly recommendable because it can provide a conformally doped, ultrashallow junction underneath a degenerately doped thin emitter layer, with a very abrupt junction doping profile. To further reduce the emitter surface area, we are currently developing the advanced selective emitter structure (see Fig. S7) for radial junction wire solar cells. Since our contact is located close to the wire bottoms, not a top side of wires, it is possible to remove the unnecessary emitters positioned at the top side of wire arrays. This selective emitter concept adopting plasma doping and wrap-around contacts will further improve cell conversion efficiencies reported to date in radial junction wire cells.

Fig. S8 Plots of FF values and a table showing the detailed sample information. Experimentally obtained, champion and averaged FF data are shown as a function of metal thickness with their standard deviations.



Metal thickness* (nm)	FF@champion, %	FF@ average %	Standard deviation
100	29.69	27.8	1.65
200	29.56	28.4	1.65
300	37.85	36.7	1.28
400	51.86	37.3	3.81
700	61	57.9	2.85
1000	65.4	62.5	1.89
1300	64.42	63.3	1.58

*At each condition, five samples were identically fabricated to evaluate the fill factors.

Fig. S9 A detailed procedure describing how to extract R_s from the variables of R_c and R_m.

1. At Line 57, Page 2, the following equation is denoted,

$$R_s = R_o + R_c + R_m = R_o + R_e \quad \text{where } R_e=(R_c+R_m),\ R_o=\text{constant}$$

The influence of R_o (base and emitter resistances) can be precluded because it is unchanged while varying the metal thickness adopted for a front electrode. R_o is determined by wafer resistivity and emitter sheet resistance. To extract R_s, we need to only know the R_c and R_m at the same time.

2. The R_c values can be obtained as a function of contact height (L) from the equation (1) used for plotting figure 3c.

$$R_c = \frac{L_T}{W} R_{\square} \coth(L/L_T) = \frac{\sqrt{R_{\square}\rho_c}}{W} \coth\left(L\sqrt{\frac{R_{\square}}{\rho_c}}\right) \quad (1)$$

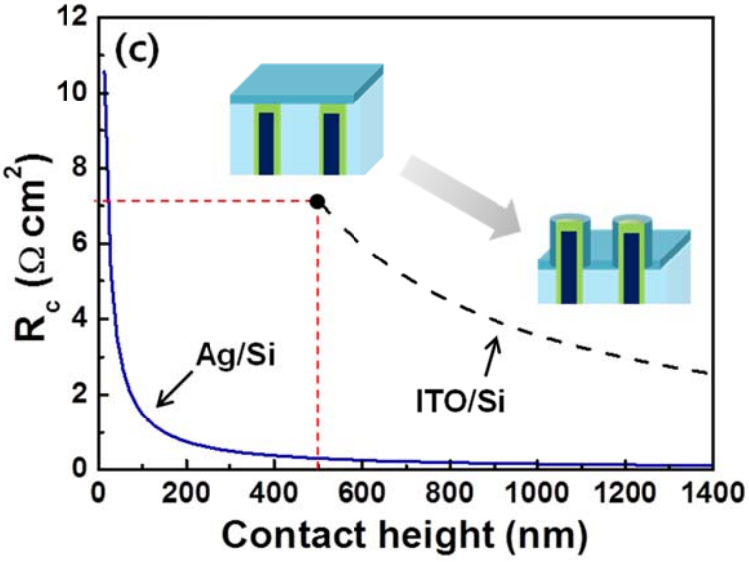


Figure 3c

3. We can also know the R_e values from a right-handed, y-axis of Fig. 2a below.

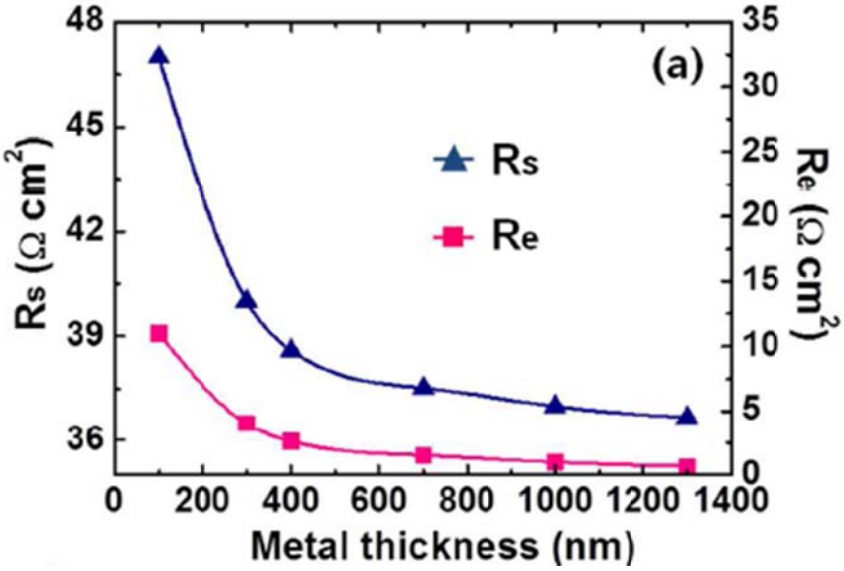


Figure 2a

4. Since the $R_e=R_c+R_m$, R_m can be obtained from the values of R_e and R_c (see Fig. 3d below). As a result, we can finally extract a total series resistance (R_s) as a function of R_c and R_m.

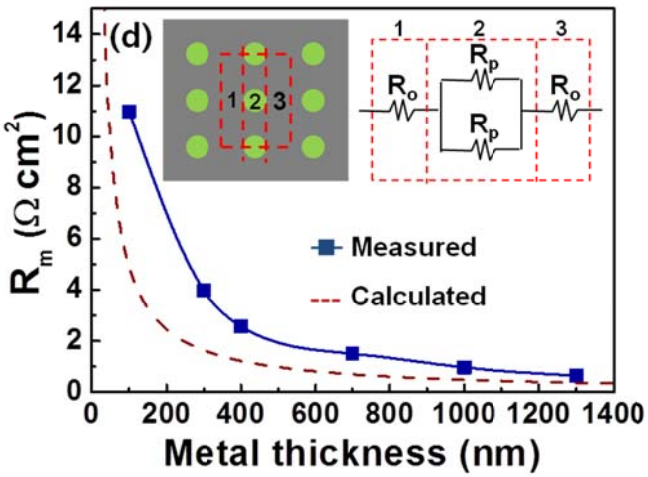


Figure 3d