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Full ceramic micro solid oxide fuel cells: Towards more reliable MEMS power generators operating at high temperatures

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- ELECTRONIC SUPPLEMENTARY INFORMATION -

In-plane microstructural and electrochemical characterization of porous LSC films

The particular study of porous LSC films deposited by PLD for their use as cathodes in Si-integrated μSOFC is reported in reference [64] (in the main manuscript). Here, top and cross section views of one of the fabricated LSC cathodes are also included, for easy finding.

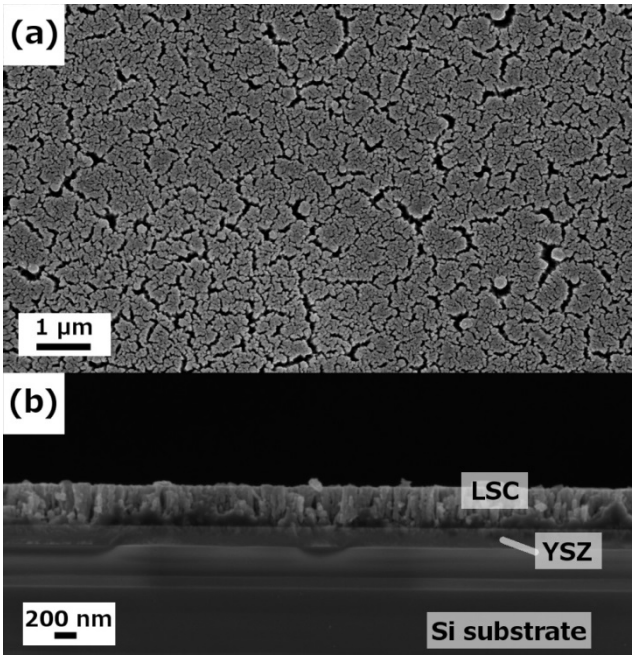

Fig. S1 Top view (a) and cross-sectional view (b) SEM images of a porous LSC cathode layer deposited by PLD, after thermal treatment up to 700ºC.

In-plane microstructural and electrochemical characterization of porous CGO films

The microstructural study was made by scanning electron microscopy (SEM) on a Zeiss Auriga equipment. The evolution of the microstructure with temperature was characterized by imaging samples before and after thermal treatments up to μSOFC operating temperatures (T=700ºC). In addition, phase identification and its evolution with temperature was made by means of in-situ X-ray diffraction (XRD) on a Brucker-D8 Advance equipment. Data acquisition was performed every 50ºC for studying pattern evolution while heating up.

In order to evaluate the electronic conductivity of the thin CGO, in-plane conductivity measurements were carried out on as-deposited porous CGO films (250 nm thick), by using the Van der Pauw technique. Four gold electrodes were defined on top of the CGO films (close to the corner edges) for their use as electrical contacts. Measurements were carried out at different temperatures from 25ºC to 700ºC by means of a Keithley 2400 sourcemeter, on a Probostat cell placed inside a furnace and using slow heating and cooling ramps ($1ºC \cdot min^{-1}$). As intended to be used as anode, a reducing atmosphere based on 5% H_2 – 95% Ar mixture was fed inside the furnace.

Figure S2 shows the evolution with temperature of the XRD pattern of a CGO/YSZ bilayer deposited over bulk $Si/SiO_2/Si_3N_4$ substrates, where the spectrum marked as RT (room temperature) corresponds to the as-deposited sample and consecutive annealing temperatures are shown, from 400ºC to 700ºC. Diffraction peaks from both crystalline YSZ and CGO diffraction patterns (cubic Fm-3m structure from JCPDS-ICDD #30-1468 and #75-0161, respectively) were already observed on as-deposited samples, despite having been prepared with very different conditions, i.e. 100ºC for the CGO and 600ºC for the YSZ. As expected since deposited at high temperatures, YSZ layer was fully crystalline as-deposited and no peak evolution was observed when heating up to 700ºC. However, sharper and more intense peaks were observed for the CGO when increasing the temperature (see the increment on T_a on Figure S2). This observation points to the crystallization of a certain amount of the amorphous CGO expected to be present in the as-deposited films due to the lower deposition temperature. In terms of fabrication, this improvement on crystallinity at such intermediate temperatures is considered very convenient. More crystalline films are expected to present better electrochemical performance, due to the improvement on mass transport properties of the crystallites compared to the amorphous form.

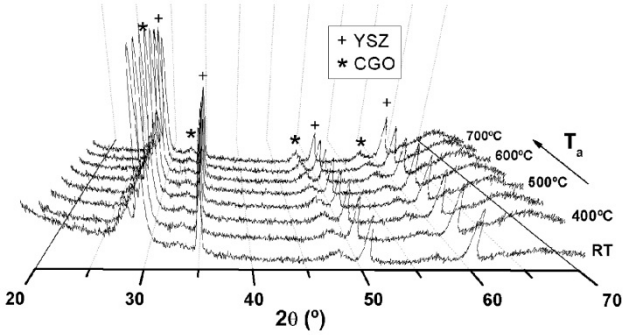

Fig. S2 X-Ray diffraction patterns of a porous CGO film deposited over dense YSZ on a $Si_3N_4/SiO_2/Si$ substrate, measured at different annealing temperatures (T_a).

Figure S3 shows top view and cross-section SEM images of as-deposited (a,b) and post-annealed at 700ºC for 5 h (c,d) CGO porous layers deposited over dense YSZ films, as complementary microstructural study to the XRD experiment. The experiment was carried out under reducing atmospheres (5% H_2-95% Ar), using heating/cooling rates of 5ºC/min. No significant differences were observed on the YSZ film before and after the thermal treatment, showing a great stability with temperature (consistent with previous XRD observations). Meanwhile, more faceted grains were observed on the CGO film and a much more open porosity was attained (see Figure S3c). The crystallization of the partially amorphous CGO is probably the reason for the microstructural change promoted by temperature, and it is considered to be beneficial for the electrode performance as it facilitates the diffusion of gas species through it.

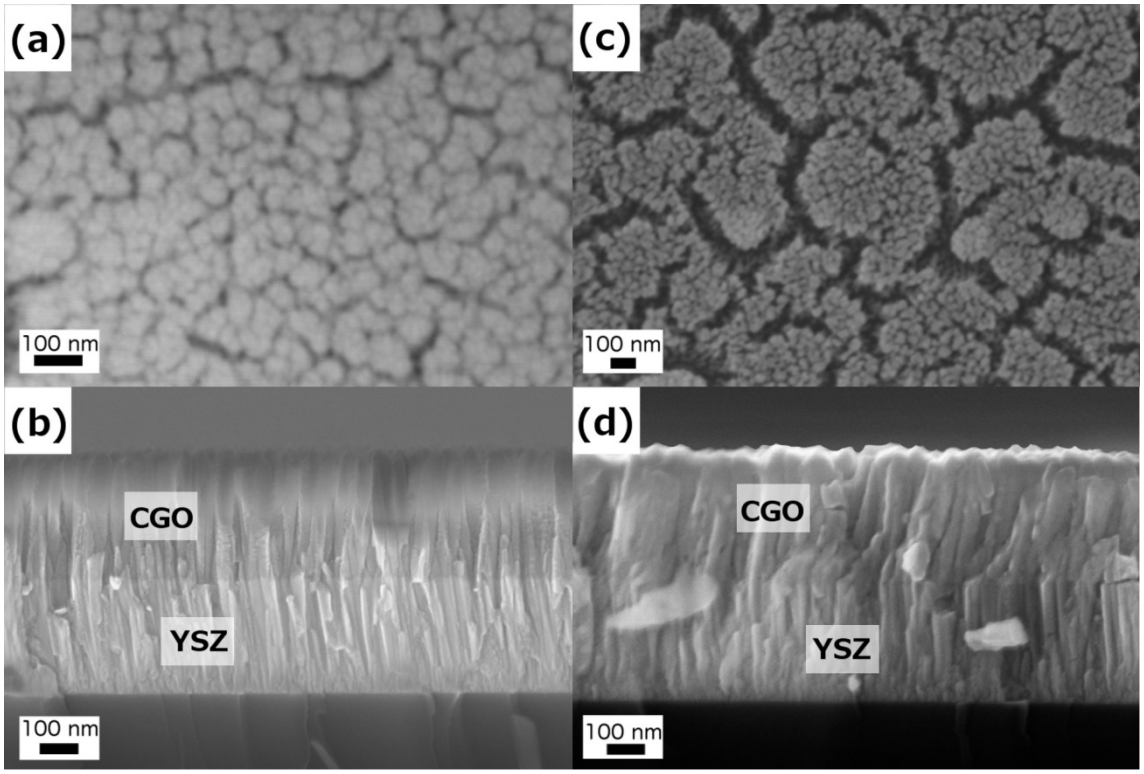

Fig. S3 Top view and cross-section SEM images of as-deposited (a,b) and post-annealed (c,d) 250 nm-thick porous CGO layers over previously deposited dense YSZ.

As can be observed in Figure S4, good step coverage was found on the backside of the wafer when depositing the porous CGO anode. This was possible due to (i.) the typical step profile generated by anisotropic etching the Si with KOH (following the 111 planes, i.e. 54º versus the substrate surface, which was 100-oriented), and (ii.) the relatively high thickness of the CGO films deposited in this work (t>200 nm) which ensured a good coverage.

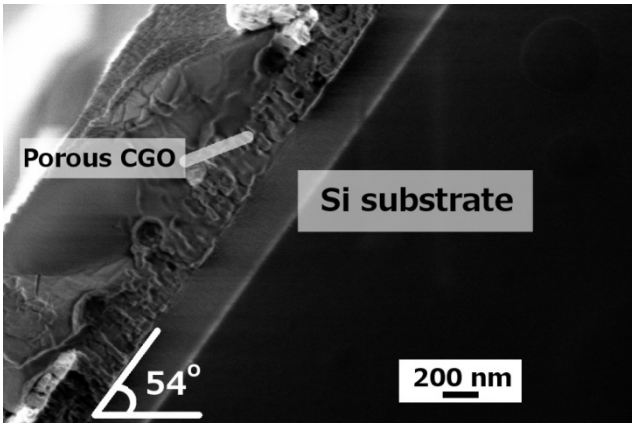

Fig. S4 Cross-section SEM image of the porous CGO anode showing the covering of the backside tilted profile (54º) on the Si-based supporting platform.

Porous CGO films of both 250 nm and 1 µm thick were fabricated, for testing the maximum thickness achievable while remaining thermomechanically stable. Problems of detachment and cracking appeared under operating conditions (T=700ºC) on the thicker films, while the thinner ones remained stable. Figure S5 shows top view and cross-sectional images of a 1 µm-thick CGO/YSZ bilayer delaminated from the Si-based substrate after thermal treatment, opposed to the 250 nm-thick films shown in Figure S3 (c,d). Maximum CGO thickness for fabricating reliable thin film CGO/YSZ bilayers was therefore limited to less than 1 µm.

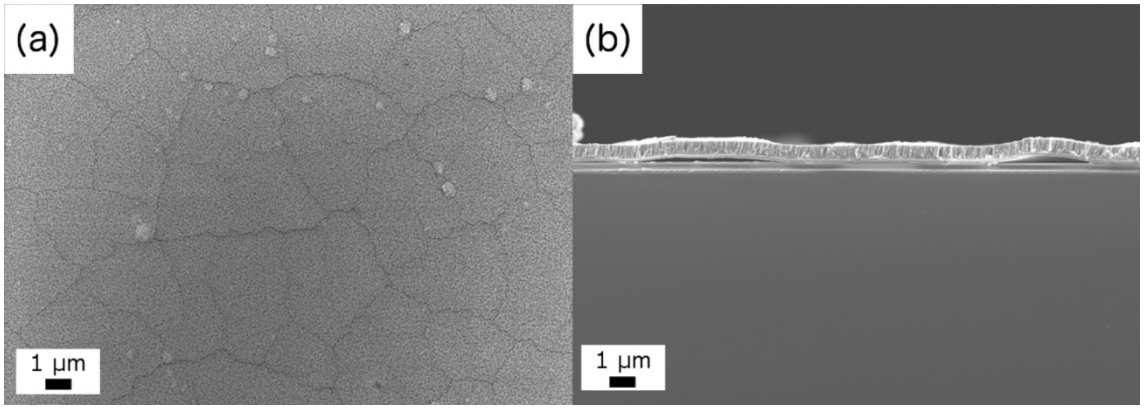

Fig. S5 Top view and cross-section SEM images showing delamination when increasing CGO thickness up to 1 µm.

Figure S6 shows an Arrhenius plot of the CGO conductivity as a function of temperature. As expected, low conductivity values (less than 0.1 S/cm) were measured on the porous films in the whole range of operating temperatures, i.e. up to 700ºC. Although still showing the anode functionality of the fabricated CGO films, that low conductivity was clearly insufficient for current percolation. Therefore, for effectiveness of porous CGO thin film anodes, adding an electronic conductor element on top (current collector) was definitely needed, reducing as much as possible the distance between the reaction points and the collector.

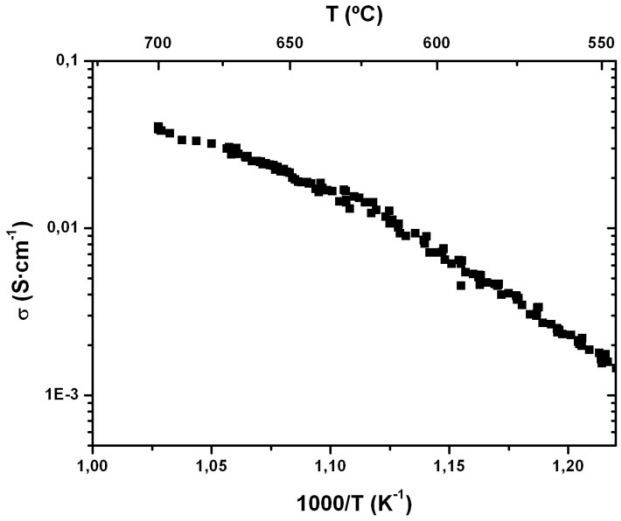

Fig. S6 Evolution of the in-plane conductivity of a 250 nm-thick porous CGO anode deposited over dense YSZ on a $Si_3N_4/SiO_2/Si$ substrate, measured by the van der Pauw method.

Thin film electrolyte chemical composition

The chemical composition used in this work for the electrolyte was 8YSZ ($(Y_2O_3)_{0.08}(ZrO_2)_{0.92}$). According to a previous publication by the authors (reference [46] in the main text), 3YSZ ($(Y_2O_3)_{0.08}(ZrO_2)_{0.92}$) would be however a better choice, mainly due to the better mechanical properties of the PLD targets and the corresponding reduction of particle ejection.

In this work, we used a large-area PLD equipment in order to develop an industrial process (able to carry out depositions at a wafer-level). Unfortunately, the unavailability of a proper 3YSZ target (prepared by SPS as suggested in the cited reference) for its use in large area PLD forced us to use 8YSZ instead. Despite this, the new equipment presents a 60º angle configuration (vs. the typical 45º) that greatly reduces the presence of particulates in the membranes. In addition, a double deposition process (with a cleaning step in the middle) was also implemented with the same objective. Finally, the results (although following a more cumbersome process) were comparable to the ones employing 3YSZ SPS targets.

Open Circuit Voltage and power density evolution of the µSOFC during the test experiment

Figure S7 shows the evolution of the open circuit voltage (OCV) of the cell and the power density at V=0.7V during the test experiment. As shown in the figure, an OCV close to the theoretical one (OCV>1.0V) was obtained after heating up to 700ºC and sealing during *ca.* 2h at such temperature (Ag O-ring was used for this purpose). After that, the cell was heated up to 750ºC and the OCV was maintained at ~1.05V for more than 2.5 h. No drop of OCV was observed during that time. Stable values of power density around P~85mW/cm^2 were maintained during dwelling time at 750ºC. At t=460min (>7.5h), the cell was heated up to 800ºC, showing membrane failure and final drop of the OCV.

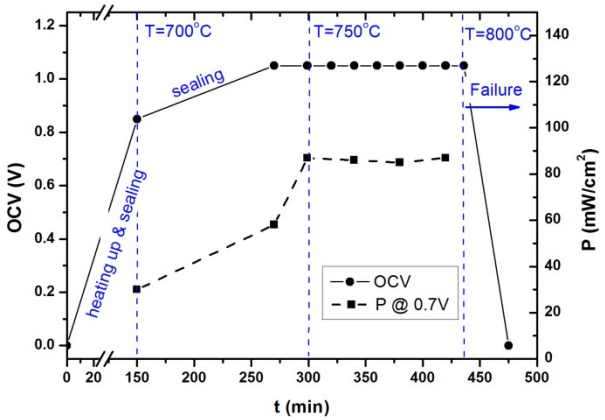

Fig. S7 Evolution of the Open Circuit Voltage (OCV) and power density at V=0.7V (P) of the µSOFC during the test experiment.

Disambiguation of the possible silicon diffusion through thin functional films deposited over Si-based substrates

Silicon diffusion into YSZ is a potential problem in thin film μSOFCs based on silicon technology, since it blocks the ionic conductivity by increasing the grain boundary resistance (where Si accumulates). Although previous studies have shown a negligible grain boundary contribution to the total resistance of YSZ membranes in silicon platforms, for this study, SIMS depth profiling carried out at the Imperial College London (in collaboration with Dr. M. Burriel and Prof. J. Kilner) showed that Si does not diffuse at 800ºC through the YSZ layer (see Figure S8).

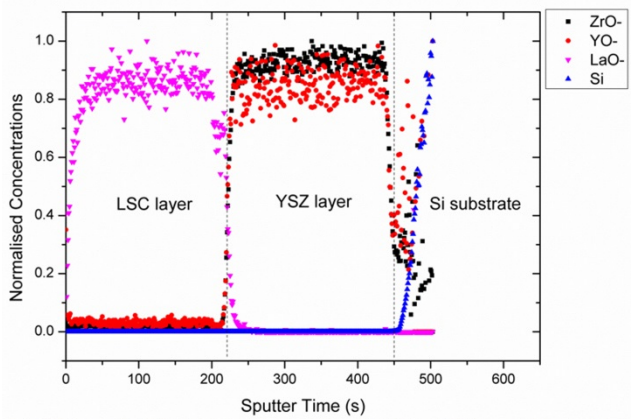

Fig. S8 SIMS depth profile coming from a LSC/YSZ thin film bilayer deposited on a $Si_3N_4/SiO_2/Si$ substrate, similar to the ones used for the μSOFC fabrication.

Electrode microstructural stability under operating conditions – Comparison with thin film Pt electrodes

Figure S9 shows top view SEM images of the here-fabricated electrodes, before and after thermal treatment at 700ºC for >10h, compared to one of the traditional metallic electrodes used on Pt/YSZ/Pt µSOFC configurations. The images are taken on thin film electrodes deposited over YSZ electrolytes on bulk Si-based substrates ($Si_3N_4/SiO_2/Si$). Oxidizing atmosphere (synthetic air) were used on LSC and Pt electrodes thermal treatments, while a reducing atmosphere (5% H_2-95% Ar) was used for the CGO anode. As it can be observed, the ceramic nanostructure remains stable with temperature (porous but continuous layer) while the Pt drastically agglomerates from starting dense layers (room temperature) into isolated particles after annealing, thus losing the electrode performance (breakdown of in-plane percolation). A similar behaviour was observed on the Pt films when annealing under reducing atmospheres (not shown here).

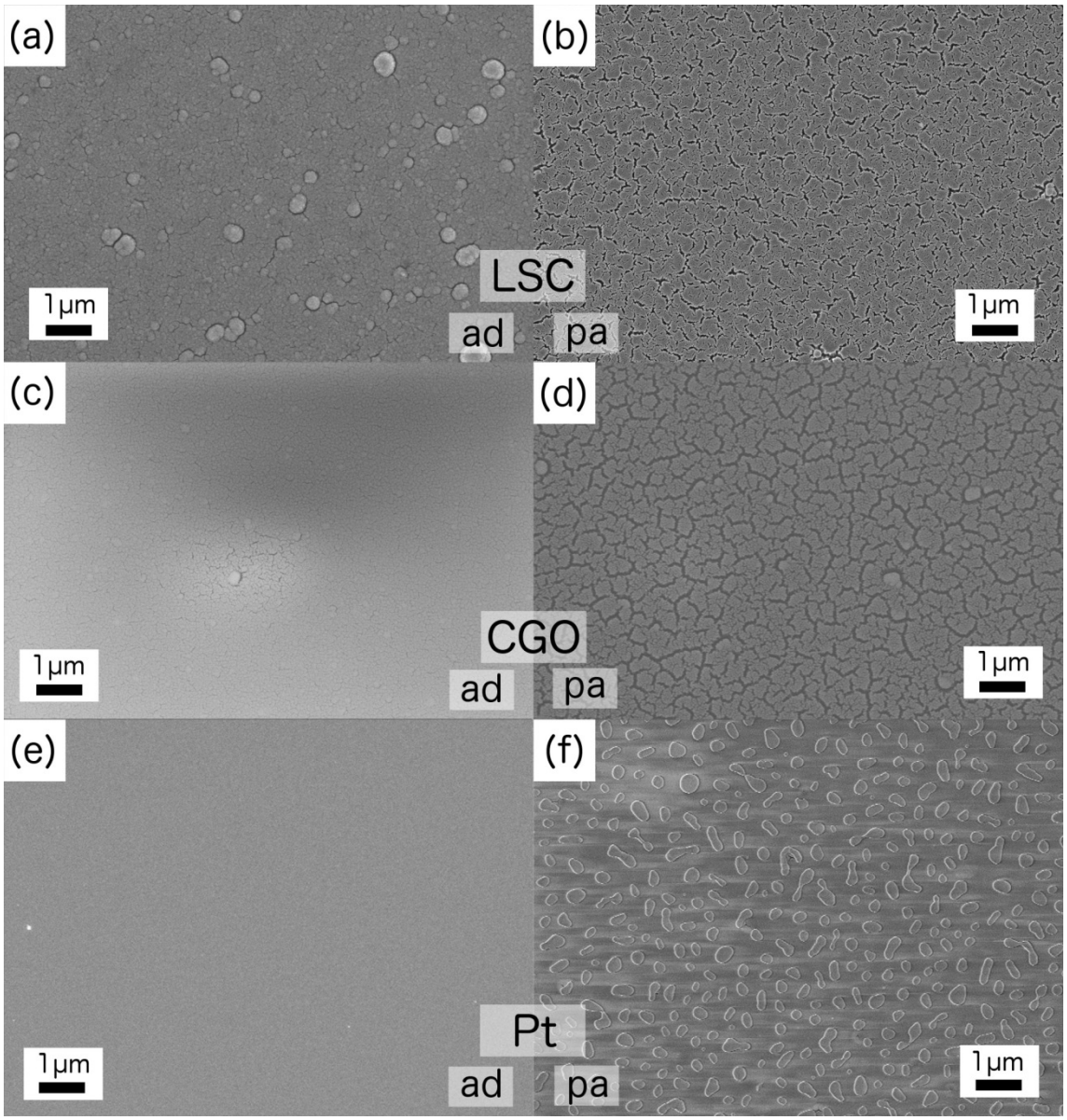

Fig. S9 Top view SEM images of the different electrodes fabricated in this work as-deposited (a, c, e - label *ad*) and post-annealed (b, d, f - label *pa*) at 700ºC.