Supporting Information

S1. Characterization of Self-Assembled Bottom-Gate FET: The self-assembled transistor with ZnO NR network as an active channel exhibits n-type conduction, and the characteristics of devices are shown in Figures S1a and b. The threshold voltage, on/off current ratio, and subthreshold swing are estimated to be about -5 V, 2.83×10^3, and 4.47 V/decades, respectively. From the SEM image in Figure 1b, the actual coverage with ZnO NRs is roughly over the 80% implying W/L value is similar with physical W/L. Thus, assuming 100% coverage, the μ_e was calculated to be $\sim 8.1\times 10^{-2}$ $cm^2/V\cdot s$ using devices dimension. Although the complete NR path that is composed of several tens of NRs acts as a polycrystalline semiconductor, the drain current was not ohmic behavior and does not exhibit a clean saturation regime and high mobility. We believe that the inferior performances originated from channel configuration (undefined and multi stacking channel) and the large barrier between the Au electrodes and the ZnO NRs. [S. H. Ko, I. Park, H. Pan, N. Misra, M. S. Rogers, C. P. Grigoropoulos, A. P. Pisano, *Appl. Phys. Lett.* **2008**, 92, 154102] & [J. E. Jang, S. N. Cha, T. P. Butler, J. I. Sohn, J. W. Kim, Y. W. Jin, G. A. J. Amaratunga, J. E. Jung, J. M. Kim, *Adv. Mater.* **2009**, 21, 1]

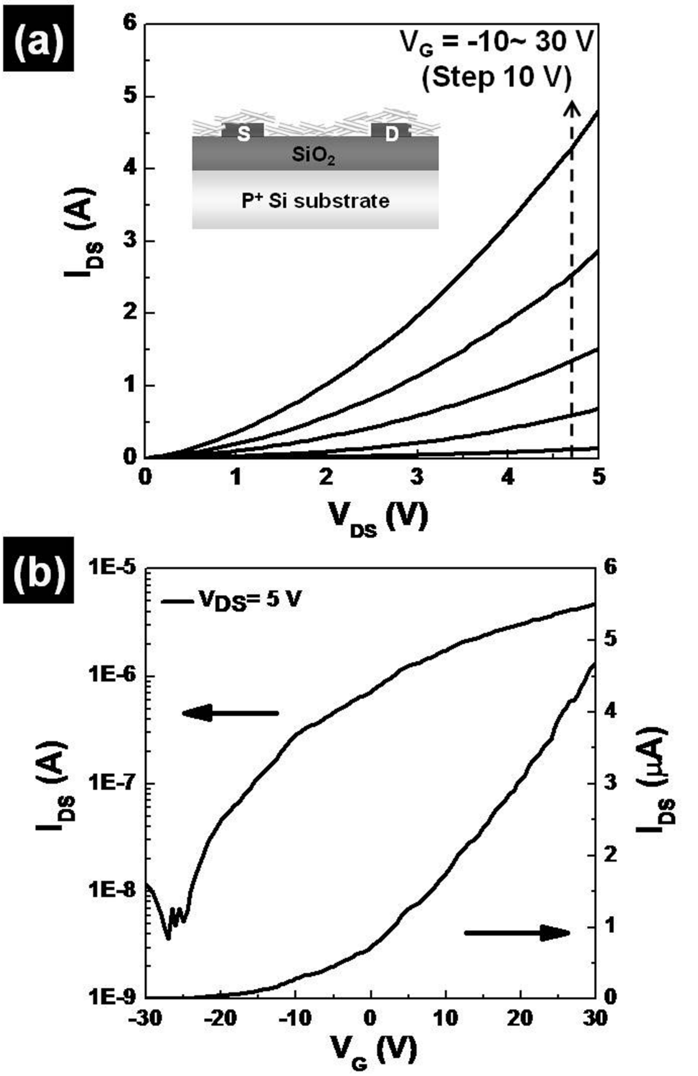

Fig. S1 Output characteristic (a) and transfer characteristic (b) of the device with a type-2 ZnO nanostructure on SiO_2/degenerated p-Si. Inset : schematic of devices with the self-assembled ZnO NR network channels.

S2. Characterization of NR-patterned Bottom-Gate FET: The transistor with ZnO NR network on Si substrate exhibits n-type conduction, and the characteristics of devices are shown in Fig. S2. The threshold voltage, on/off current ratio, and subthreshold swing are estimated to be about -4.2 V, 6.12x 10^4, and 2.38 V/decades, respectively. The μ_e was calculated to be ~1.18 $cm^2/V{\cdot}s$ using effective width.

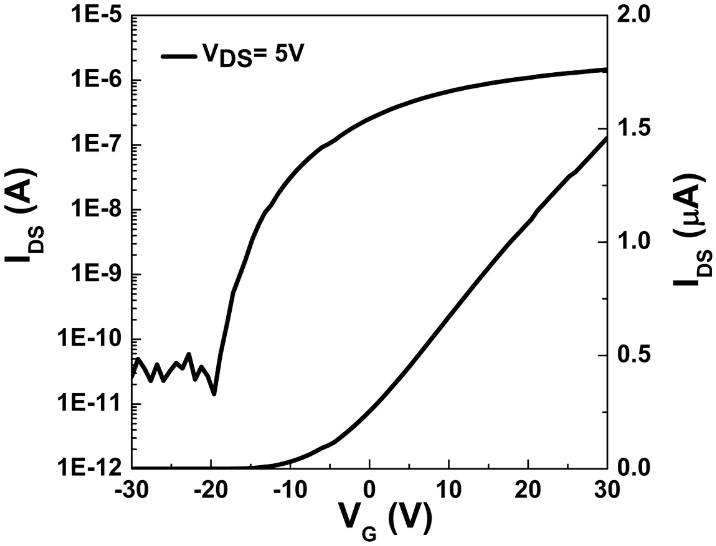

Fig. S2 Transfer characteristic of the device with a patterned type-2 ZnO NR on SiO_2/degenerated p-Si.

S3. Distributions of the density of the picked-up and the transferred NRs. The quantitative statistics between the areal densities of the NRs and the device performance. And the distribution of the device performances during repeated handling of 5 cycles: The density of the picked-up NRs was varied from 0.1 to 0.30 NRs/μm^2 after applying a pressure of ~5 kPa. The deviation of the NR density in our process might be caused by a nonuniformity of the NR synthesis on the substrate and handling mistakes during the pick-up process. Therefore, if the process is controlled elaborately by using a micro-aligner, fabrication yield is expected to be improved. The quantitative statistics between the areal densities of the NRs and the device performance are summarized in Fig. S3c. The changes in electrical properties are not significant. It is believe that the mobility of the devices with the higher density of NRs slightly increased mainly due to the increase in the electrical pathway. The Fig. S3d shows the distribution of the device performances during repeated handling of 5 cycles. We believe that the variation of the device performance is attributed to the change in the areal density of the NRs between source and drain. The deviation in electrical properties is not significant implying the density of the NRs can be controlled in our process.

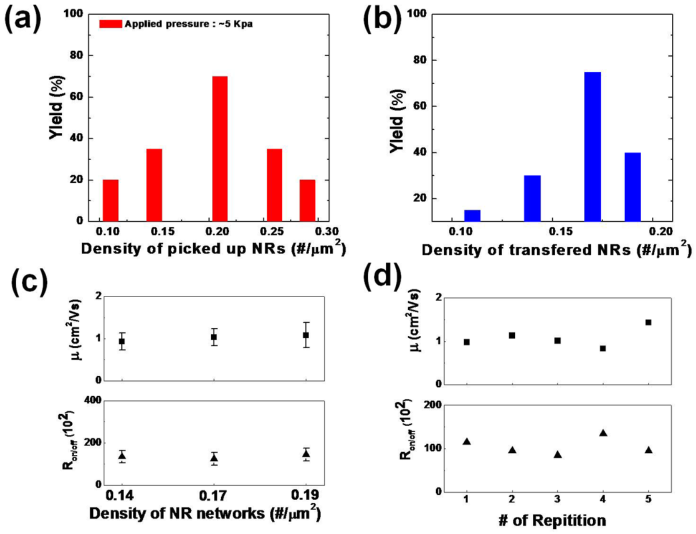

Fig. S3 Fabrication yield of (a) the picked-up NR density and (b) the transferred NR density. (c) The quantitative statistics between the areal densities of the NRs and the device performance. (d) The distribution of the device performances during repeated handling of 5 cycles.