Supporting Information

Intrinsic memory behavior of rough silicon nanowires and enhancement *via* facile Ag NPs decoration

*By Ji-Hyuk Choi, Jinwoo Sung, Kyeong-Ju Moon, Joohee Jeon, Youn Hee Kang, Cheolmin Park and Jae-Min Myoung**

Department of Materials Science and Engineering, Yonsei University,

* Correspondence should be addressed to 134 Shinchon-dong, Seodaemoon-gu, Yonsei University, Seoul, Postal #120-749. Telephone: (82-2)2123-2843. Fax: (82-2)312-5375. E-mail: jmmyoung@yonsei.ac.kr.

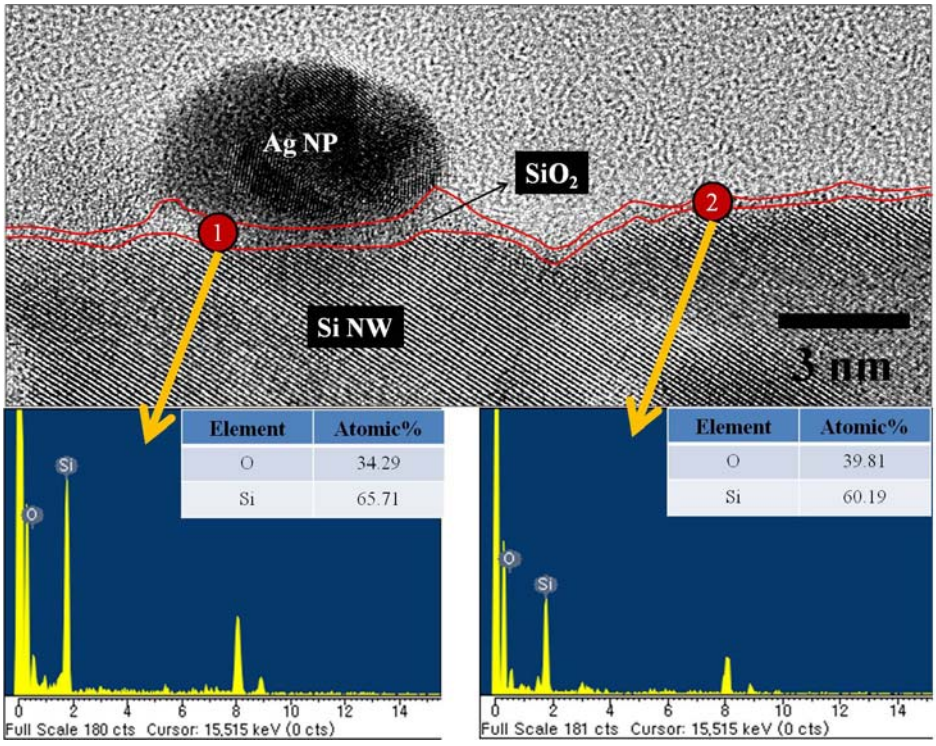

Fig. S1. The HRTEM image shows an EE Si NW with Ag NP on the SiO_2 surface. Non-uniform and very thin native oxide layer can be seen in this image. Moreover, STEM-EDS analyses on the oxide layers with and without Ag NPs (region 1 and 2, respectively) show different compositions. These results imply that their identities are distinguishable. For better understanding, more detailed experiments are needed. Here, we just hypothesize that SiO_2 blocking layer can be synthesized by simple chemical reaction, finally leading to a stable memory operation.

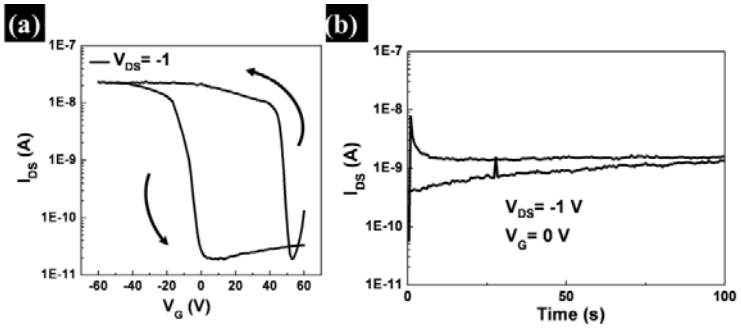

Fig. S2. (a) The transfer curves for EE Si NW FET at different ranges of V_G sweep of ± 60 V. For hysteresis measurement, transfer curves of forward sweep and backward sweep are shown. The directions of the forward and backward sweeps are indicated. (b) Time dependent stability of conductance in the two states. The off-state "0" was obtained with a V_G of −40 V and on-state "1" with a V_G of 40 V for 1s, showing very short charge storage duration.