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Supporting Information

Solution processed non-volatile top-gate polymer field-effect transistors

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Figure S1. (a) Transfer characteristics obtained after different gate pulse conditions for control GSID 1208719 transistor (pure PS-b-P4VP and 50wt% Cytop as dielectric stack layers). The channel length and width was 150 μm and 500 μm respectively.

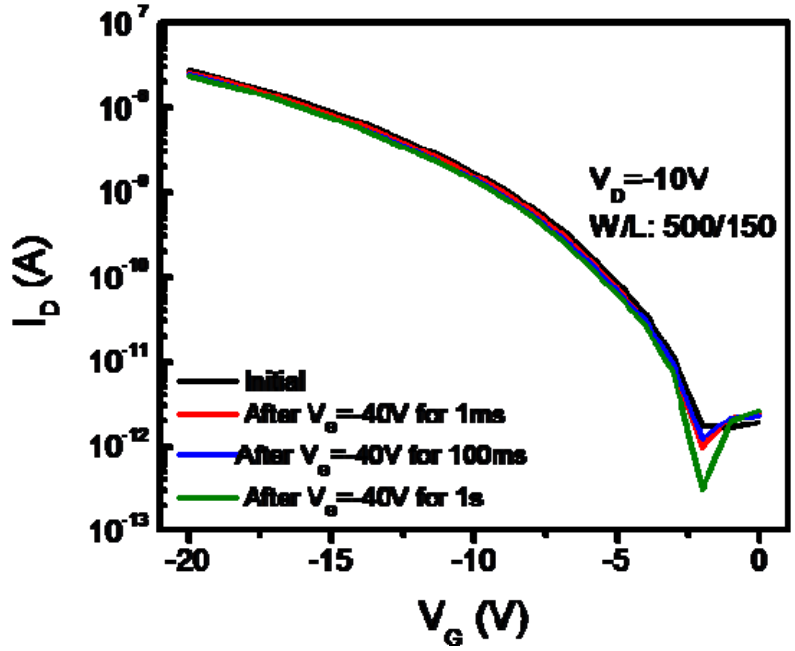


Figure S2. (a, b) Transfer characteristics obtained after a gate pulse voltage of -30V for 1ms with different magnitude of gate leakage current levels. The gate leakage currents are plotted in dotted lines. 50wt% Cytop was used as the control dielectric layer. The molar ratio of Au^{3+}:P4VP is 0.2.

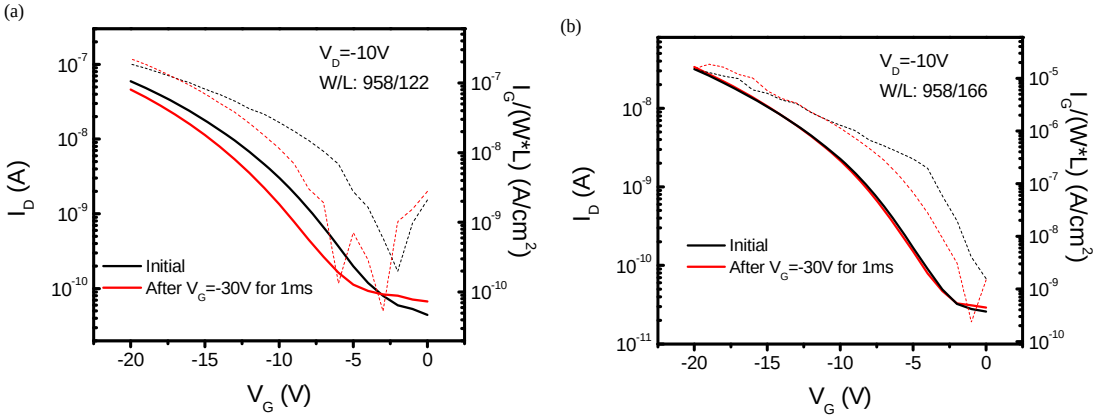
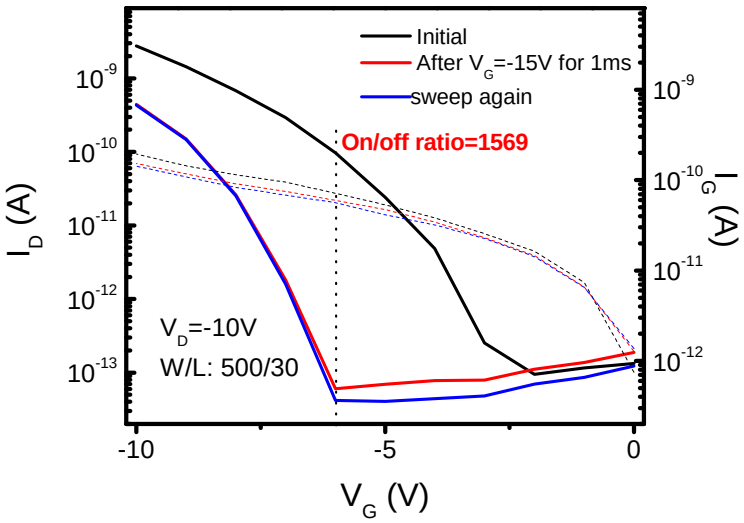


Figure S3. Transfer characteristics of GSID 1208719 top-gate transistor memory on PET substrate obtained after a gate pulse voltage of -15V for 1ms (left). The channel length and width was 30 μm and 500 μm respectively. The gate leakage currents are plotted in dotted lines. Digital camera image of the flexible top-gate transistor memory on PET substrate (right). The molar ratio of Au^{3+}:P4VP is 0.3.



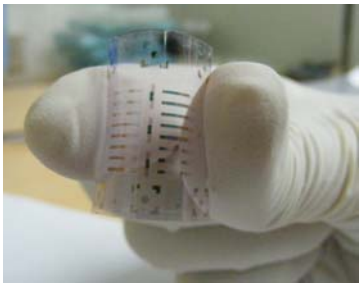


Figure S4. Transfer characteristics obtained after different gate pulse conditions for (a) control P3HT transistor channel length of 30 μm and width of 500 μm. (b) top-gate P3HT memory transistor with channel length of 60 μm and width of 1200 μm. The drain voltage, V_D, is -5V. The transfer characteristic of pristine device is black curve. The molar ratio of Au^{3+}:P4VP is 0.2.