Supporting Information

Figure S1. Schematic images of the CFL process for fabricating gold dot pattern and fabrication of electrode and electric field assisted deposition.

Figure S2. Scanning electron microscopy (SEM) images of the gold nano-patterned substrate   and Photo-lithographically pattern electrodes

Figure S3.   Schematic image of the experimental process during electric field assisted deposition

Figure S4.   SEM image about the aligned SWNTs in small gold dots(120nm) patterned substrate

Figure S5. The partial magnified SEM image of sample having well aligned SWNTs along to gold dot pattern in large area-1 (dot diameter = 500nm, period = 1000nm)
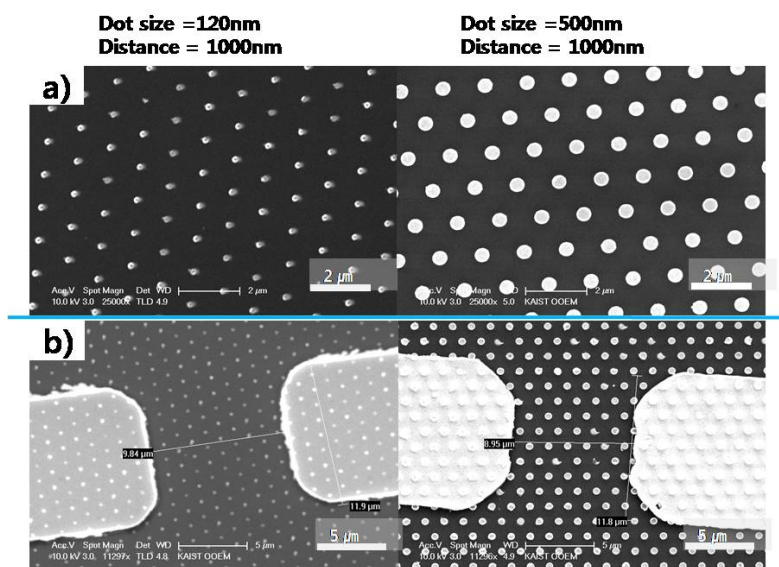
Figure S6. Scanning electron microscopy(SEM) images of density difference of positioned SWNTs along gold dots varying channel size.

Figure S7. The partial magnified SEM image of sample having well aligned SWNTs along to gold dot pattern in large area-3(ellipsoidal shaped dot diameter = 1500-2000nm, period = 1500nm).

Figure S8. Repeatability and time stability of gold patterned SNWT-FET devices
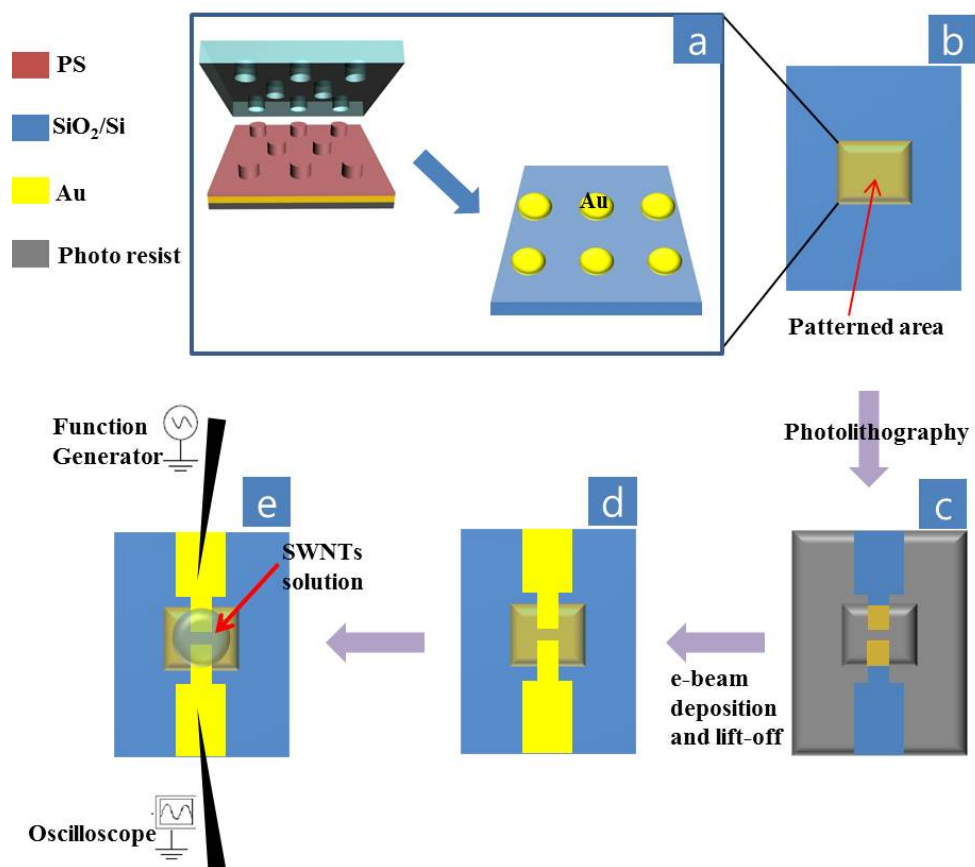
Figure S1. Schematic images of the CFL process for fabricating gold dot pattern and fabrication of electrode and electric field assisted deposition.

Figure S2. Scanning electron microscopy (SEM) images of (a) the gold nano-patterned substrate with different sizes and distances and (b) the Photo-lithographically pattern electrodes having wide and long channel between electrodes on patterned substrate.
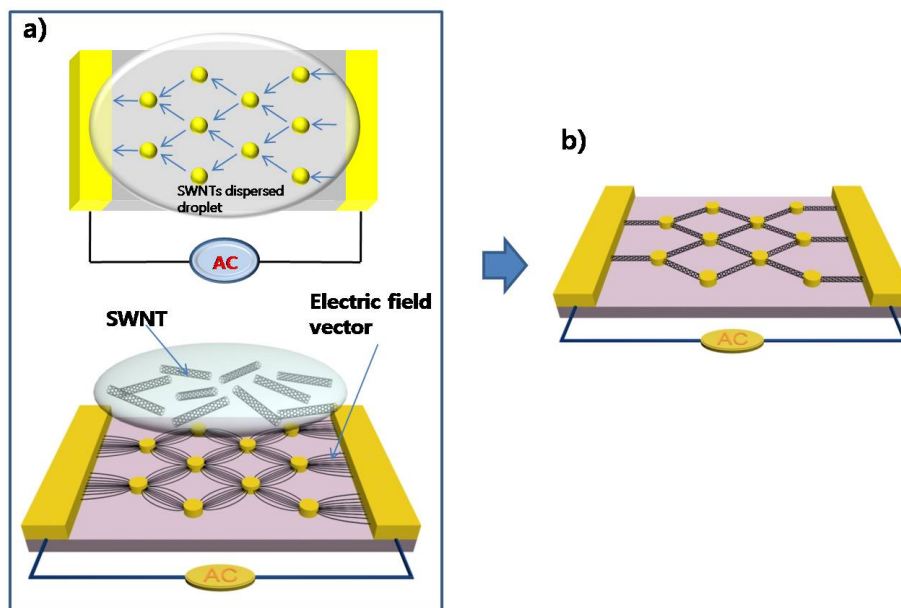
Figure S3. Schematic image of the (a) formation of high electric field density between gold dots in the SWNTs dispersed solution when ac function is applied, (b) positioned SWNTs in this channel between gold dots. .

Dot size =120nm, period = 1000nm
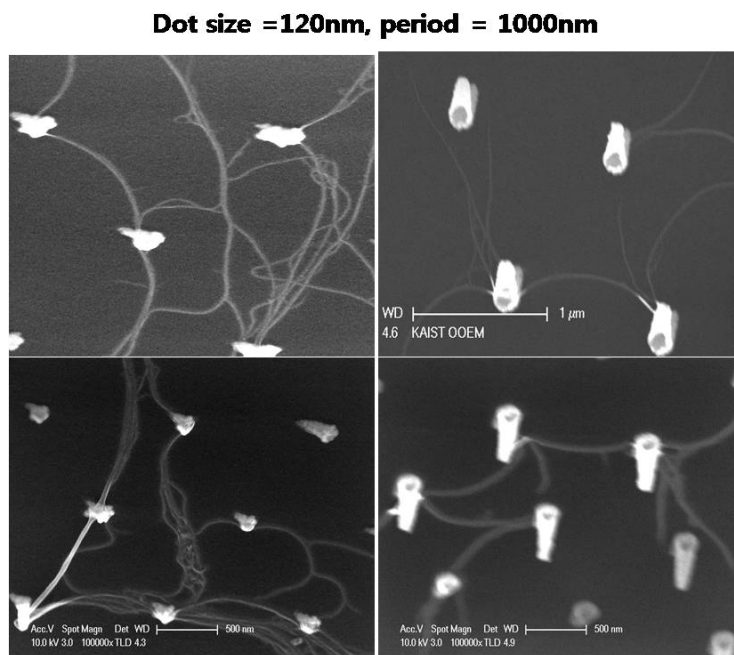
Figure. S4. SEM image of sample having aligned SWNTs along to small gold dots(120nm). Although confirming the aligned each SWNTs along small gold dots, SWNTs are positioned in specific part of device, not whole area. Furthermore this FET device using small gold dot pattern is difficult to get the high FET performance.
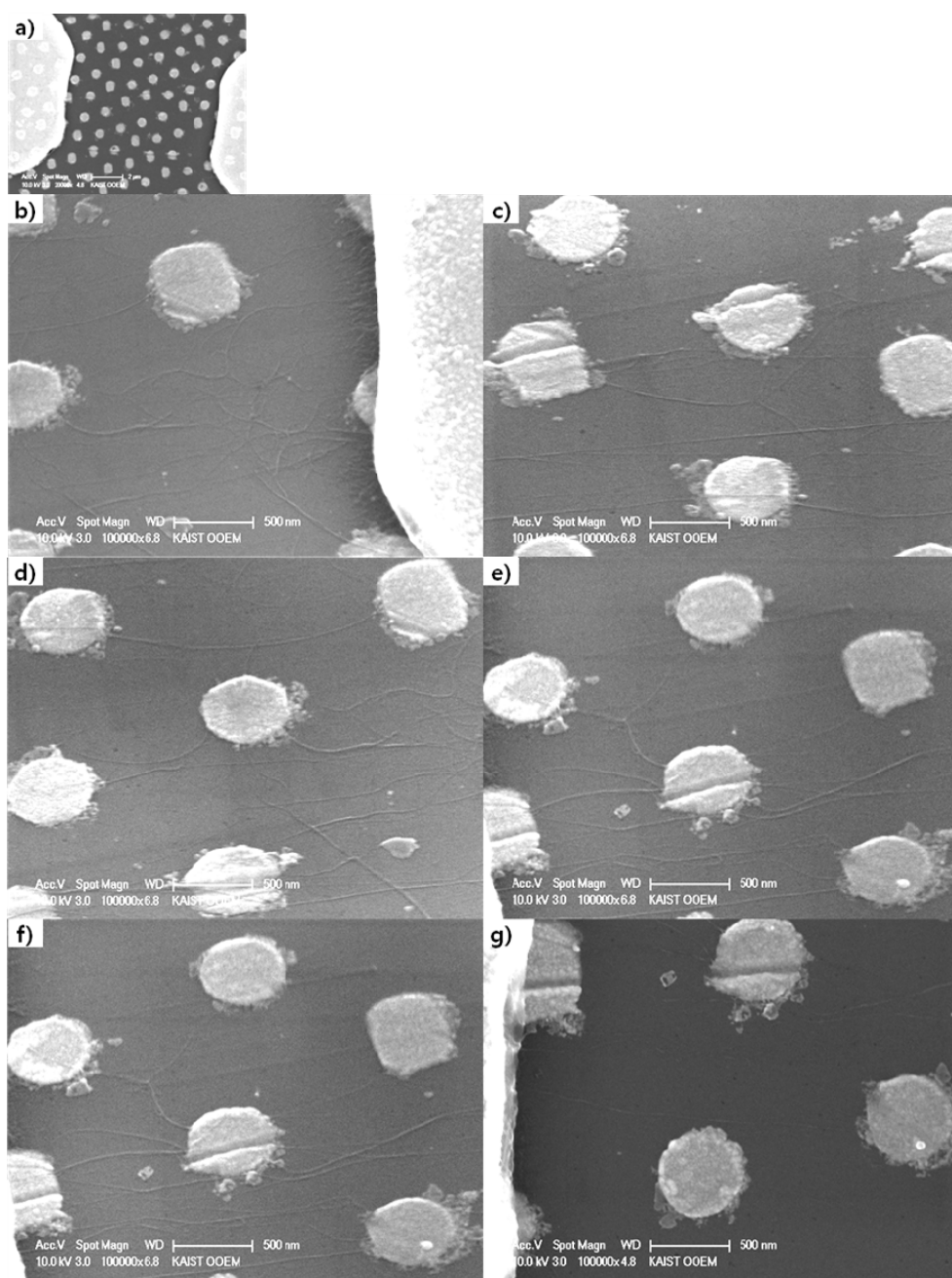
Figure S5. a) Whole SEM image of sample having aligned SWNTs along to gold dots. But due to tiny size of SWNT, cannot confirm the aligned each SWNTs in whole pattern image. And by seeing the magnified SEM images(b-g), we can find the placement of SWNTs in patterned substrate. (dot diameter = 500nm, period = 1000nm, channel size = 10.0 μm ×9.0μm)
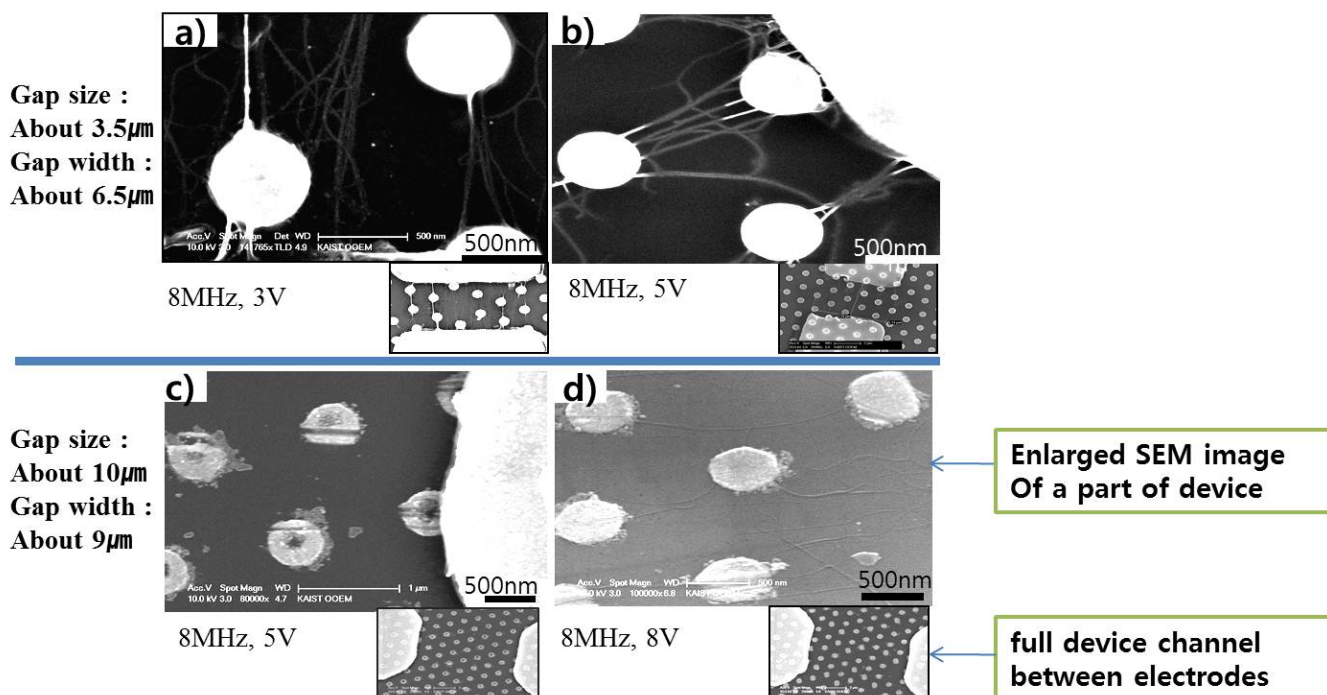
Figure S6. Scanning electron microscopy(SEM) images of density difference of positioned SWNTs along gold dots varying with (a, b) 5, 8V in about 3.5 μm ×6.0μm channel size and (c, d) 5, 8V in 10.0 μm ×9.0μm channel size. a) A few bundle and strand of SWNTs are interconnected along to gold dots at 3V. b) Some SWNTs bundles are presence between gold dots at 5V c) Any SWNTs does not exist on substrate at 5V. d) Many number of SWNTs is interconnected along the gold dots in large channel area at 8V. We found that large channel sized substrates are required higher voltage than small sized channel to pull SWNTs onto the desired area between gold dots and the optimum electrical condition is 3-5V, 8MHz in case of about 3.5 μm ×6.0μm channel size and 8V, 8MHz in 10.0 μm ×9.0μm channel size.
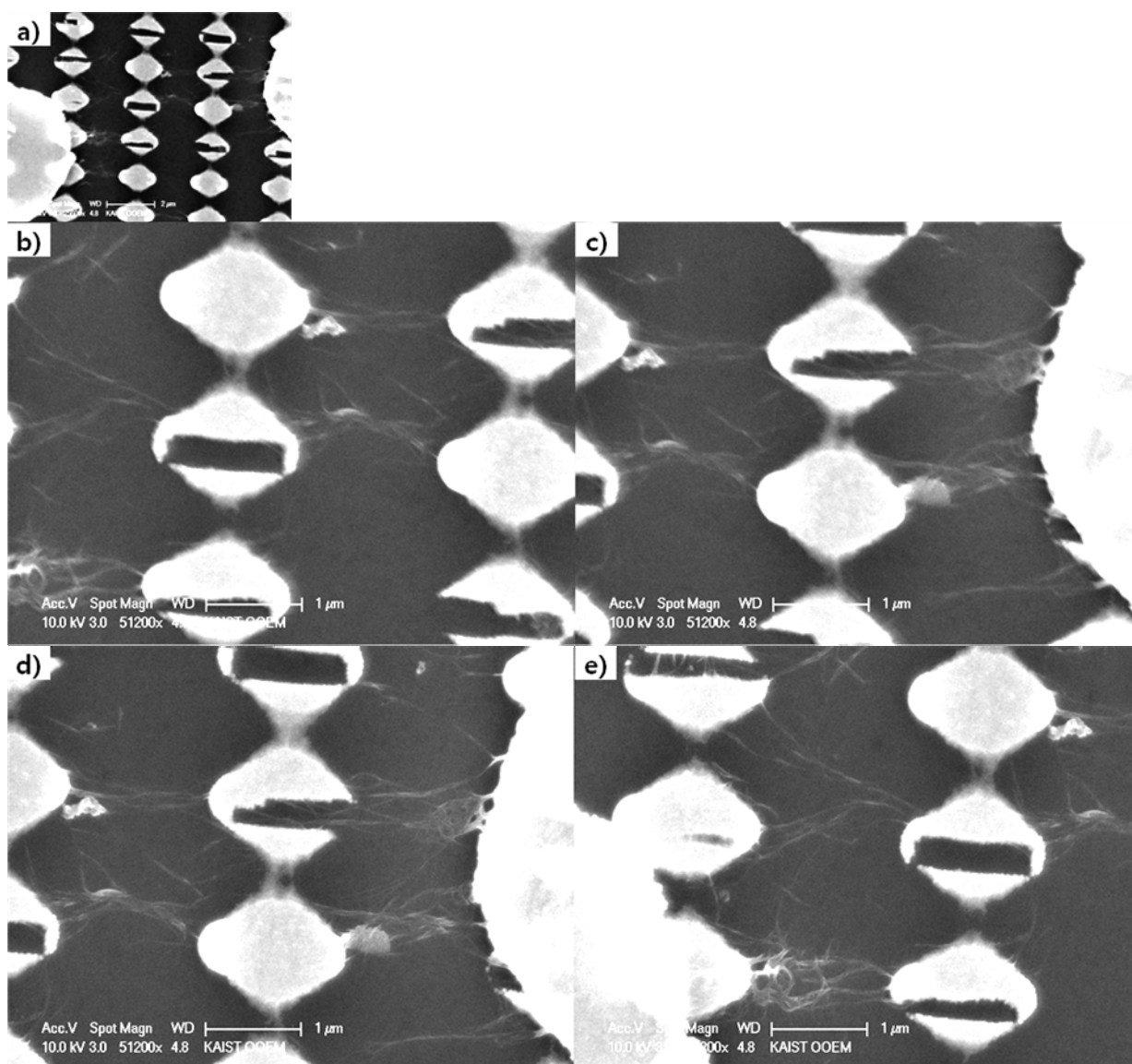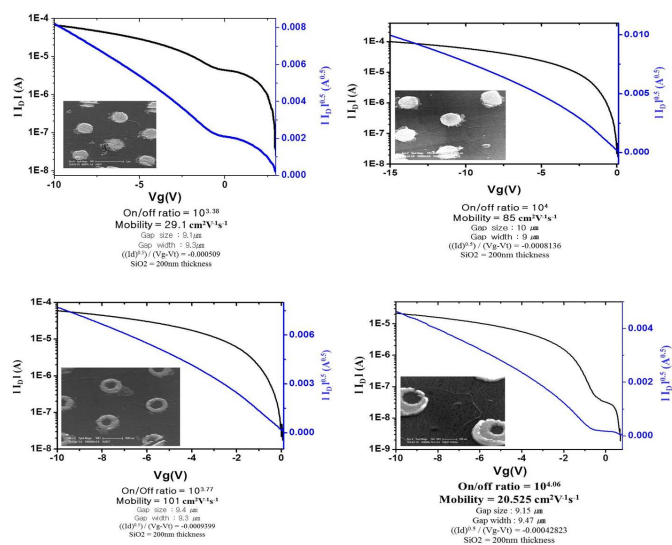
Figure S7. This pattern has many aligned SWNTs between gold dots. The above SEM images prove that gold dots can control the flow of dielectrophoresis and orientation of SWNTs.

(dot size =about 1500nm×1000nm, distance between dots = 1500nm, channel size = about 8.5 μm ×4.5μm) .

Figure S8. Repeatability and time stability of gold patterned SNWT-FET devices.

(Id-Vg curve of different gold patterned SWNT-FET samples)

Our gold patterned SWNT-FET devices with different samples show good FET performances, indicating good repeatability. The high on/off ratios and high mobility are likely due to the reduced contact points of (semiconducting-semiconducting SWNTs and metallic-semiconducting SWNTs).
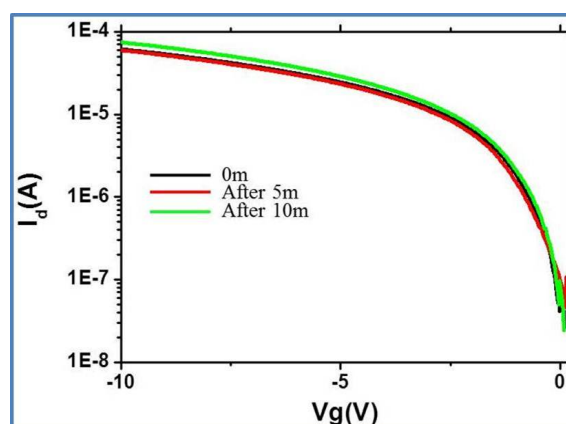
Time stability of FET characteristics.

(We tested the Id-Vg curve of a sample as a function of time, showing good stability.