Supporting Information

Low-Voltage Solution-Processed Graphene Transistors Based on Chemically and Solvothermally Reduced Graphene Oxide

Beom Joon Kim^{1†}, Moon Sung Kang^{2†}, Viet Hung Pham³, Tran Viet Cuong³, Eui Jung Kim³, Jin Suk Chung³, Seung Hyun Hur³*, Jeong Ho Cho¹*

¹Department of Organic Materials and Fiber Engineering, Soongsil University, Seoul 156-743, Korea

²Department of Chemical Engineering and Materials Science, University of Minnesota, 421 Washington Avenue SE, Minneapolis, Minnesota 55455 USA

³School of Chemical Engineering and Bioengineering, University of Ulsan, Ulsan 680-749, Korea

[†]B. J. Kim and M. S. Kang contributed equally to this work

*Corresponding authors: jhcho94@ssu.ac.kr and shhur@ulsan.ac.kr



Figure S1. AFM images of chemically- and solvothermally-reduced graphene oxide films.



Figure S2. AFM image and its corresponding height profile of chemically-reduced graphene oxide film.



Figure S3. (a) $ln(\sigma_{min})$ vs. T^{1} plots (b) $ln(\sigma_{min})$ vs. $T^{1/3}$ plots of ion gel-gated graphene FETs based on chemically- and solvothermally-reduced graphene oxides.



Figure S4. (a) $ln(\sigma_{min})$ vs. T^{1} plots and (b) n_{i} vs. T^{1} plots of SiO₂-gated graphene FETs based on chemically- and solvothermally-reduced graphene oxides.