Heterojunction with Organic Thin Layer for Three Dimensional High Performance Hybrid Solar cells

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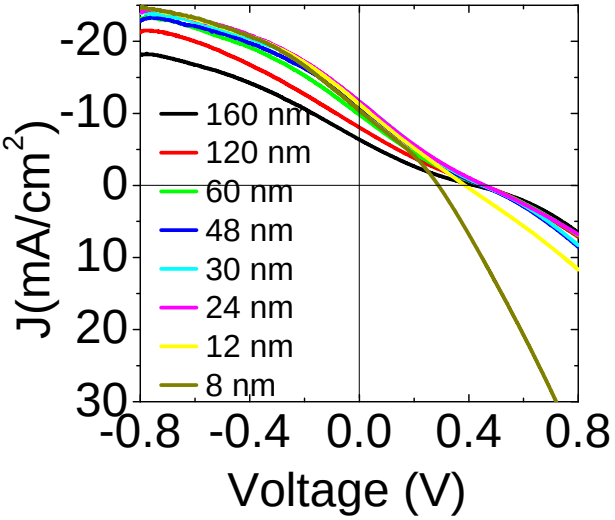

Fig. S1 J-V curves of solely planar junction devices based on polished silicon substrates with different thicknesses of P3HT films.

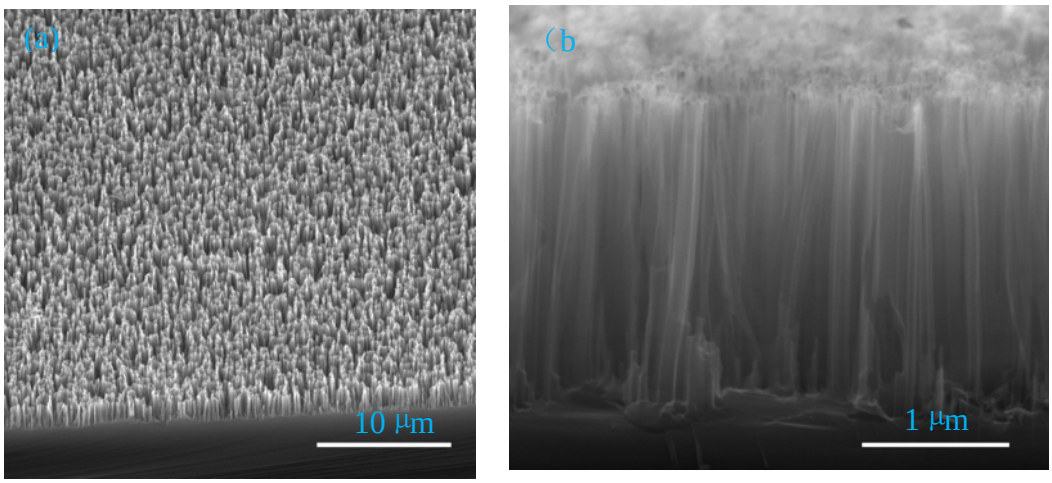

Fig. S2 Scanning electron microscopy (SEM) images of freshly prepared silicon nanopillar arrays (SiNPs) with view angle of (a) 45° and (b) 90°.

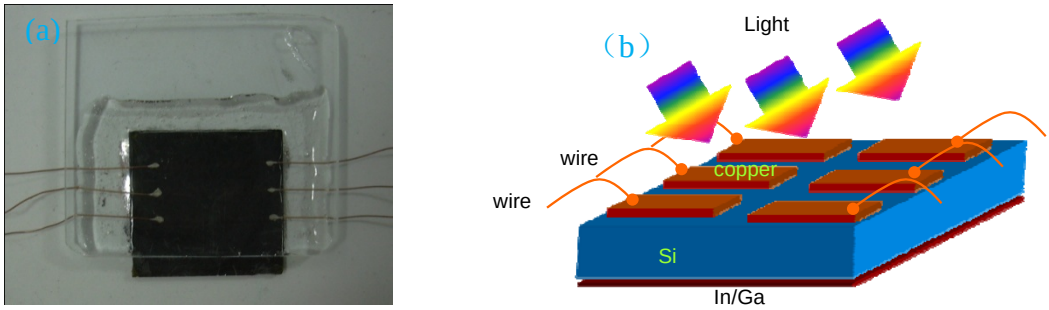

Fig. S3 (a) Real SiNPs device encapsulate with glass and epoxy resin. As shown in (b) (not in real scale), there is six pixels on the top surface. Due to strong light trap capability of SiNPs, the ultrathin copper electrodes (1.5 mm×5 mm) were difficult to be observed in images. The copper wires are adhered on electrodes by silver paste.

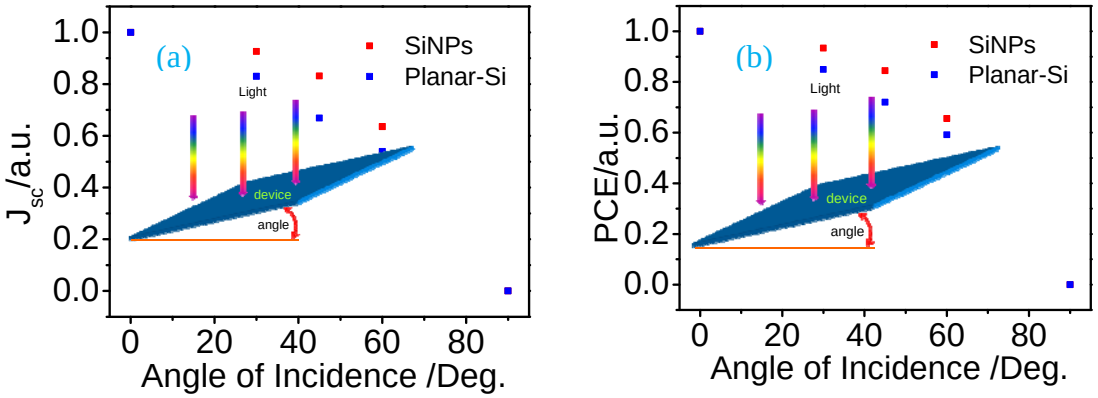

Fig. S4(a) Measured short circuit current density (J_{sc}, normalized) and (b) power conversion efficiency (PCE, normalized) of hybrid devices with SiNPs and planar silicon as top layer over different angles of incidence under AM 1.5 G illumination at 100 $mWcm^{-2}$.

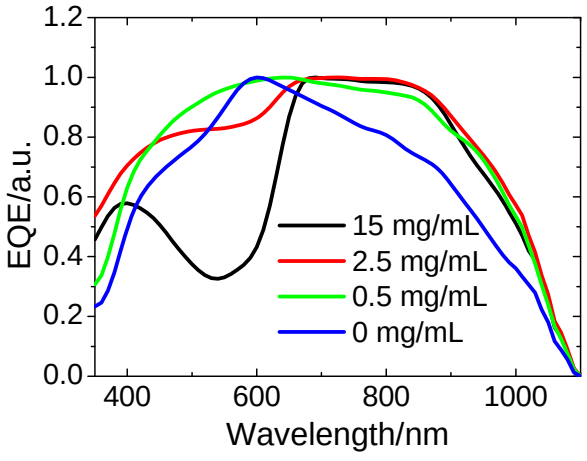

Fig. S5 Normalized short-circuit external quantum efficiency (EQE) of devices made by spin coating 15 mg/mL, 2.5 mg/mL, 0.5 mg/ml P3HT on SiNPs. 0 mg/mL means direct metal contact without P3HT layer.

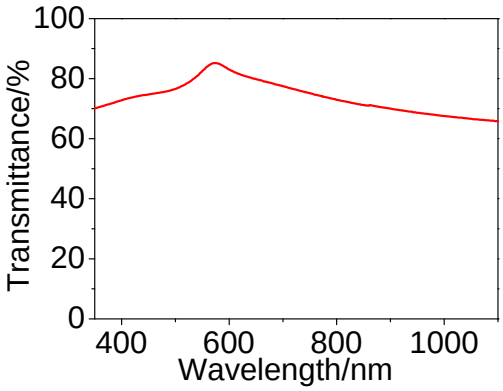

Fig. S6 Transmittance spectra of ~10 nm Cu film on glass.

Table S1 Electric output characteristics of hybrid devices based on planar silicon substrates with different thicknesses of P3HT.

Device	Thickness of P3HT (nm)	J_{sc} ($mAcm^{-2}$)	V_{oc} (V)	FF	PCE (%)
1	160	6.4	0.422	0.20	0.5
2	120	8.1	0.453	0.21	0.7
3	60	9.8	0.447	0.21	0.9
4	48	11.0	0.447	0.21	1.0
5	30	11.6	0.452	0.21	1.1
6	24	11.6	0.459	0.21	1.1
7	12	11.3	0.386	0.24	1.0
8	8	10.4	0.289	0.29	0.9