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Supplementary Information

Solution-Processed Yttrium Oxide Gate Insulator for High-Performance All-Solution-Processed Fully Transparent Thin Film Transistors

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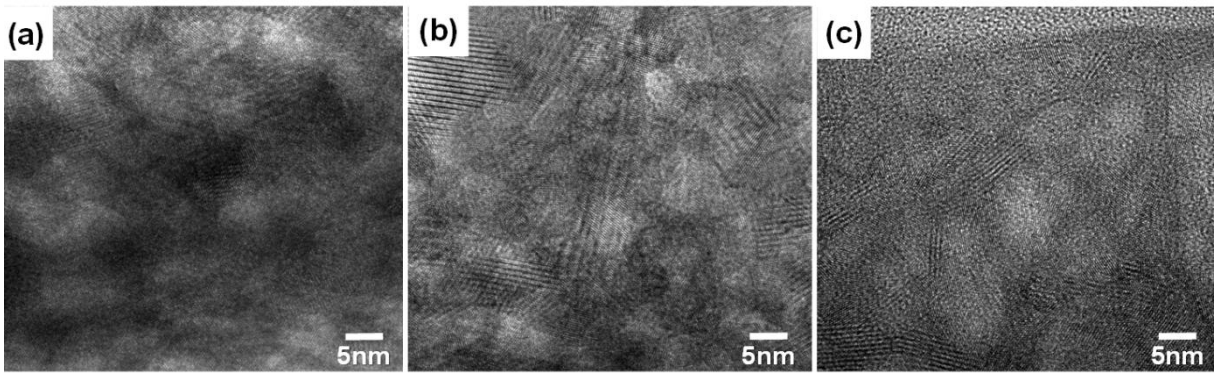

Figure S1. HR-TEM images show crystallinities of the spin-coated YO_x as a function of the annealing temperature of (a) 300 °C, (b) 400 °C, and (d) 500 °C. Enhanced crystallinity with increasing annealing temperature is apparent.

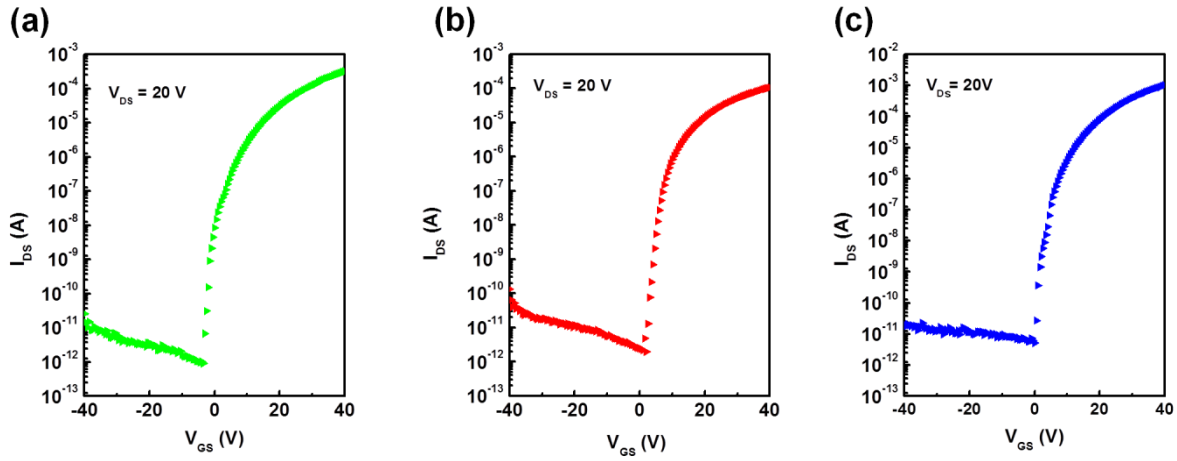

Figure S2. Transfer characteristics of (a) ZnO (annealed at 350 °C), (b) ZTO (annealed at 500 °C), and (c) ZnO (annealed at 400 °C) TFTs with thermally grown silicon oxide are plotted. Soluble ZnO and ZTO semiconductors were spin-coated onto cleaned SiO_2 (thermal grown)/heavily doped Si substrates. Channel width and length are 3000 μm and 120 μm, respectively. Field-effect mobility and threshold voltage were calculated from transfer characteristics for each TFT (a) ZnO-TFTs: 2.41 $cm^2 V^{-1} s^{-1}$ and 10.76 V, (b) ZTO-TFTs: 0.74 $cm^2 V^{-1} s^{-1}$ and 8.43 V. (c) ZnO-TFTs with thermally grown SiO_2/Si substrate: 10.5 $cm^2 V^{-1} s^{-1}$ and 14.09 V.

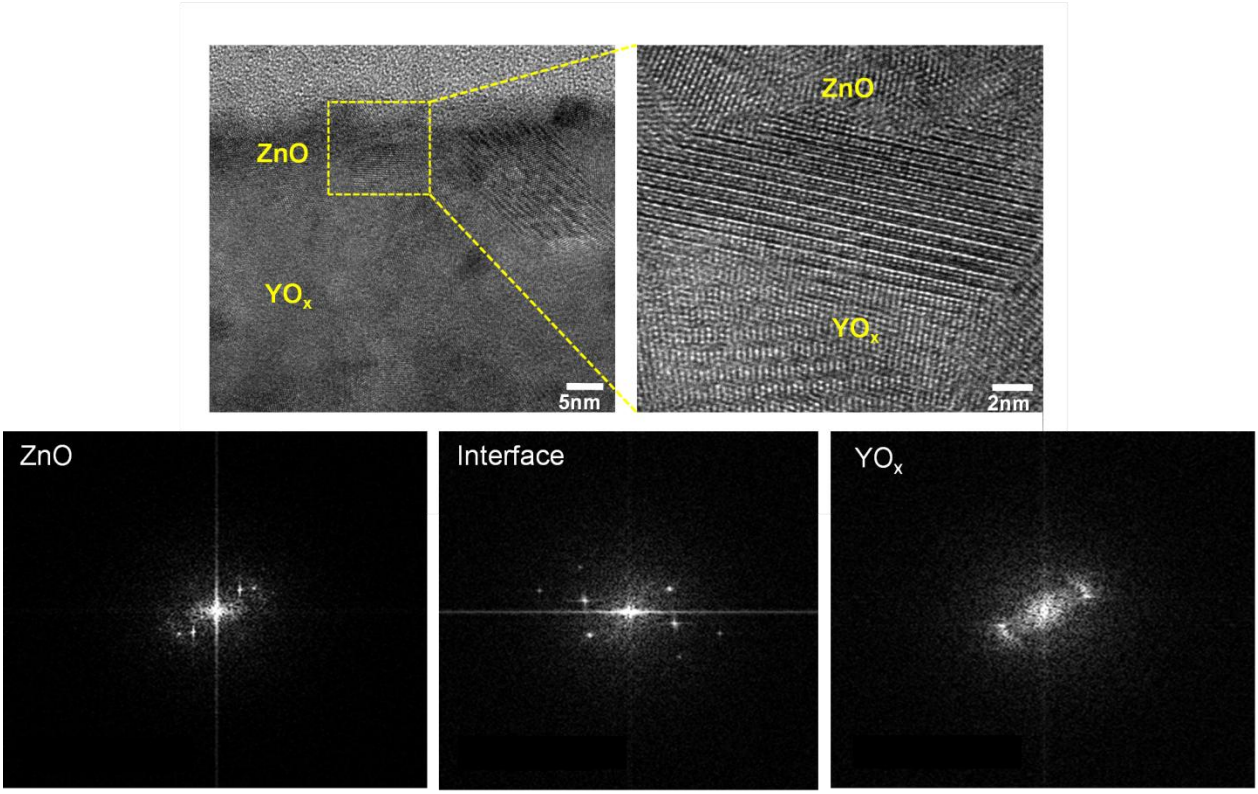

Figure S3. HR-TEM images of the interfaces between solution-processed ZnO semiconductor (annealed at 400 °C) and YO_x gate dielectric (annealed at 400 °C). Local homogenous lattice match forms at near the channel, suggesting that these well-defined interfaces lead to enhanced performance of solution-processed oxide TFTs. Three FFT images obtained across the ZnO-YO_x boundary are different one another and the spots observed in the image at the interface are discernible.