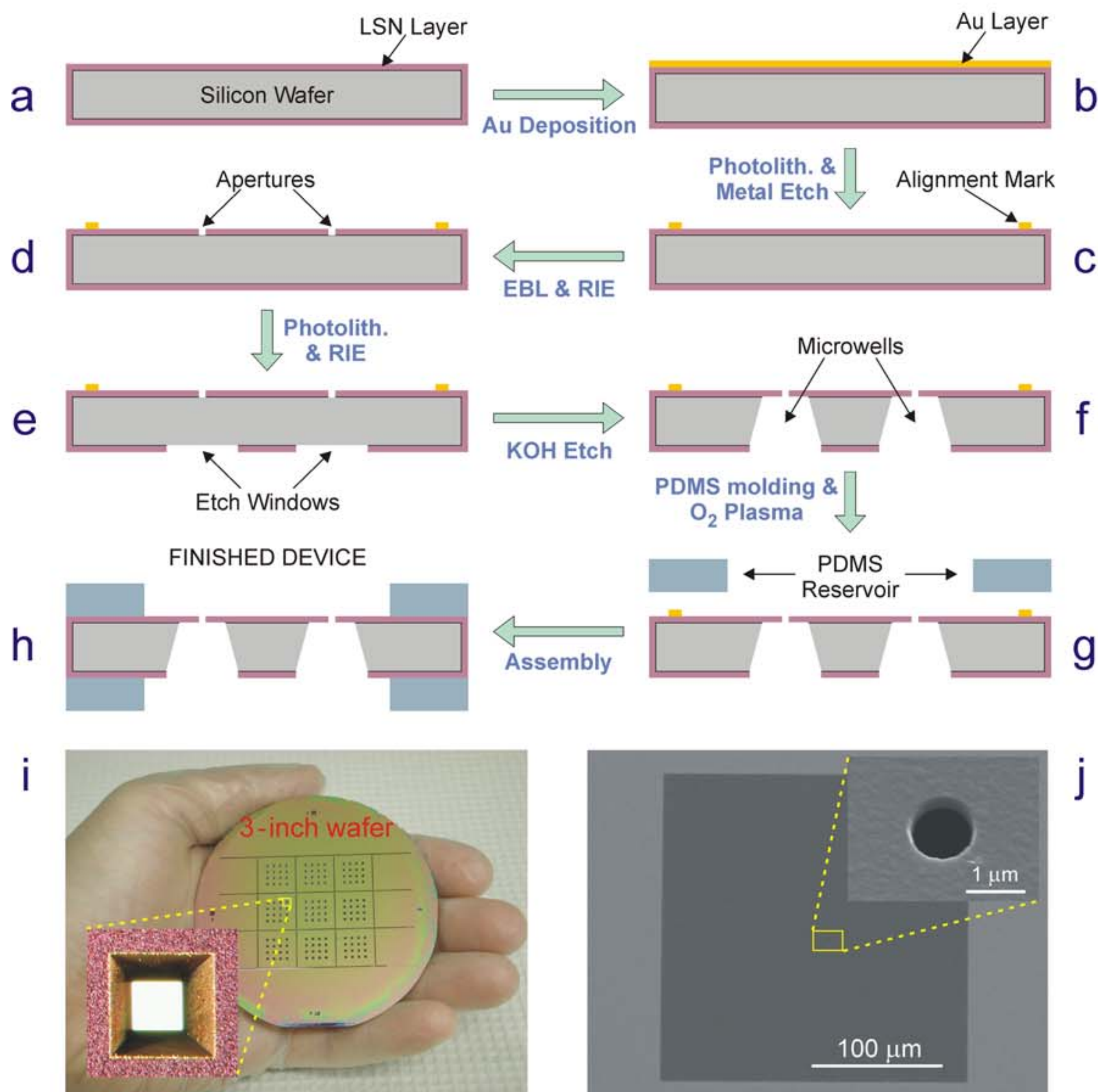
This journal is © The Royal Society of Chemistry 2006



Supplementary Figure 1: Nanofabrication of the planar apertures. **(a)** First, a 300 nm layer of low-stress silicon nitride (LSN) is deposited on the whole wafer. **(b)** The front (polished) side of the wafer is coated with a 100 nm layer of gold. **(c)** Using photolithography and gold etching, gold alignment marks are created. **(d)** Apertures, which are in registration with the alignment marks, are etched in the LSN layer using electron beam lithography (EBL) followed by reactive ion etching (RIE). **(e)** Etch windows, which are in registration with the alignment marks, are patterned in the LSN layer on the back side of the wafer via photolithography followed by RIE. **(f)** The wafer is then immersed in hot KOH bath, which anisotropically etches inverted-pyramid pits (microwells) until the pits reach the bottom of the front LSN layer and creates an array of suspended LSN membranes with a planar aperture at the center of each membrane. **(g-h)** Finally, the device chip is sandwiched and sealed between two fluidic reservoirs made of PDMS. **(i)** Optical micrograph showing the backside of a wafer (after step **f**) with nine identical chips (in a 3×3 array), each with a 4×4 array of microwells; the inset shows a magnified view of a microwell. **(j)** SEM image showing a suspended LSN membrane (darker square) with the inset zooming in on the 500 nm diameter aperture at the center of the membrane.