Electronic Supplementary Information:

Polysilsesquioxane (PSQ) in xylene was purchased from Gelest, Inc., Morrisville, PA with a trade name "HardSil^{TM} AP". It was used as is or further diluted in xylene for the sealing cap fabrication.

25 sccm O_2 flow was used and oxygen plasma was generated by an RF generator in an "Oxford 80+" (Oxford Instruments, Concord, MA) reactive ion etching (RIE) system for PSQ surface treatment. All other RIE etchings for device fabrication were also carried out using the same system.

To fabricate the 1D nanochannel substrate, an HTG contact mask aligner was used to pattern lines of different widths from 1 μm to 500 μm into a photoresist on a Si, or thermally oxidized Si wafer. Cr was then deposited by an e-beam evaporator. The Cr on top of the photoresist was lifted off in a warm acetone bath. Trenches were then etched by RIE with a CHF_3/O_2 chemistry using the remaining Cr as the etching mask. The trench depth ranged from 8 nm to 200 nm.

To fabricate the 2D nanochannel array substrate, a 320-nm-period grating mold was used to pattern the grating structure into a polystyrene film on a Si or thermally oxidized Si wafer by thermal nanoimprint lithography. Cr was then evaporated only on top of the grating lines by shadow evaporation. Oxygen RIE was used to remove the residual polystyrene at grating bottom with Cr as the mask. The grating pattern was transferred into the substrate by CHF_3/O_2 RIE either using Cr/polystyrene directly as etching mask, or using Cr fabricated by additional Cr evaporation and lift off as the etching mask.

To fabricate the integrated micro-, nanochannel devices with a micro-to-nano interface, a channel pattern of 1 cm long, 100 μm wide, containing micropost and 10 μm wide channel array patterns (refer to Fig. 3b in main paper), was transferred into photoresist first by contact photolithography. Cr evaporation and liftoff exposed the channel area for subsequent etching. The substrate was fused silica slide, Si or thermally oxidized Si wafer with a size about 1 in^2. With Cr as mask, the whole channel area was etched into the substrate by RIE with a depth of < 100 nm. Then a second mask was used and gradient photolithography (Ref. 17 in main paper) was carried out with the second layer features aligned to the first layer channel features using designed align marks. After the gradient photolithography, the intended nanochannel area (10 μm wide channel array) was covered by photoresist and the microchannel area was exposed for further dry etching. The photoresist patterns had sloped sidewalls between the nanochannel and microchannel areas due to the gap between the mask and substrate in gradient photolithography. After a further RIE with CF_4 chemistry, 0.5 μm deep microchannel and sloped interfaces to the protected nanochannel area were formed simultaneously. Then an additional photoresist was spun to protect the front surface of the substrate, and the loading holes were drilled from backside of the substrate at the ends of the whole channel by sand blasting. Finally, the photoresist and Cr were removed and the substrate was cleaned for PSQ sealing.