Supporting Information: Model Based Design of a Microfluidic Mixer Driven by Induced Charge Electroosmosis

Cindy K. Harnett[†], Yehya M. Senousy[†], Katherine A. Dunphy-Guzman[#], Jeremy Templeton[*] and Michael P. Kanouff[*§],

[†]University of Louisville

Louisville, Kentucky 40292

[#]Systems Studies Department

[*]Thermal/Fluid Science and Engineering Department

Sandia National Laboratories

P.O. Box 969

Livermore, California 94550

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1. Supplementary Information on Modeling

Figure S-1 shows the model used for the diffuse and Stern layers. Finite volume numerical calculations were carried out on multi-processor systems containing from 8 to 32 processors.

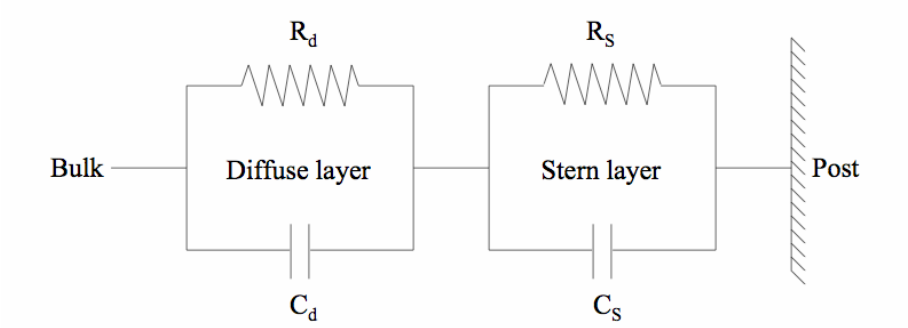

Figure S-1. **Schematic of the linear circuit used to model the electric double-layer.**

2. Test Device Layout and Metrology

Figure S-2a shows a full image of the test chip which had a 5x10 array of conductive posts. An oblique scanning electron micrograph (SEM) of several of the test-device posts is shown (Fig. S-2b). One chip was filled with epoxy and cut and polished to create a cross sectional view through the center of one of the posts (Fig. S-2c). This was used to quantify dimensions of the posts for the purpose of making the model (Fig. S-2d).

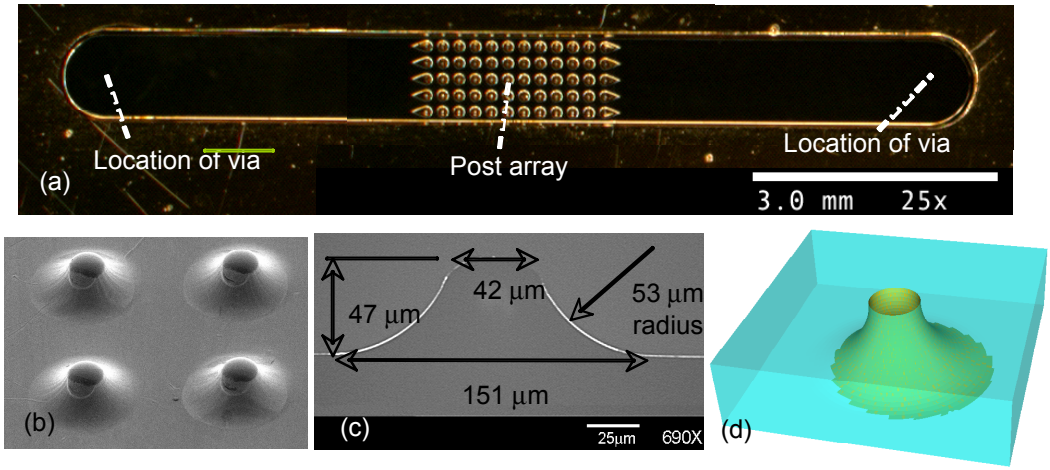

Figure S-2. **(a)**The metallized polymer test chip used to characterize ICEO flows. **(b)** An oblique scanning electron micrograph of a volcano shaped post, and **(c)** a micrograph of a cross section of the posts. **(d)** The computer model incorporates the measured shape and the observed off-center alignment of the metal pad.

3. Integrated Electrode Device Fabrication Sequence

The next generation devices had through-wafer microfabricated electrical contacts which reduced the requirement on the applied voltage to ~10V from ~300V due to the integrated electrodes' proximity to the polarizable ICEO posts. These devices were fabricated on 4-inch diameter, (100)- orientation silicon-on-insulator (SOI) substrates (Ultrasil Inc.) typically having a 100-micron thick high resistivity (>5000 ohm-cm) silicon layer on the via side, a 2-micron thick buried oxide layer, and a 300 micron thick, low-resistivity (<0.02 ohm-cm) highly-doped silicon device side.

Electrical and fluid feedthroughs were micromachined through the low-conductivity side by wet chemical etching, while ICEO posts and electrodes with vertical sidewalls were created from the 300-micron thick, high conductivity silicon side. The 2-micron thick buried oxide served to insulate the channel floor between the conductive posts.

To create an etch mask for wet chemical etching, the SOI wafers were first coated with a 650-nm silicon dioxide (SiO_2) layer by wet thermal oxidation for 2 hours at 1000 C in an oxygen atmosphere. Fluid and electrical via holes were created on the low-conductivity side by photolithography and removal of the oxide by buffered oxide etch (BOE) solution, followed by etching in tetramethylammonium hydroxide (TMAH) at 75 C (approximate etch rate 12-15 microns per hour) through a depth of 100 microns. The etch stopped at the buried oxide layer.

Afterwards, to insulate the sidewalls of the etch pits from the contact electrodes, a 650-nm thick oxide layer was applied by thermal oxidation. Cr metal was sputtered over the oxide on the etched side to promote resist adhesion over the corners of the etch pits, followed by hexamethyldisilazane (HMDS) priming and photoresist spinning at a slow speed (Shipley 1827, 1500 RPM). For electrical contact, the highly-doped silicon was exposed at the bottom of the etch pits by photolithography and wet chemical etching with Cr etchant (Transene) and BOE. Subsequently, the resist and chrome masks were removed by acetone and Cr etchant. After this step, the wafer has insulated etch pits on the low-conductivity side as illustrated in Figure S-3a.

Electrodes were then produced on the etched side by sputtering a Cr adhesion layer of approximately 50 nm (3 minutes in a 30 mTorr argon atmosphere at 350 W incident RF power) and a gold layer approximately 135 nm thick (3 minutes in a 30 mTorr argon atmosphere at 120 W applied DC power.) Pads and traces were protected by patterned photoresist, followed by immersion in potassium iodide gold etchant (Transene Inc.) and Cr etchant (Transene.) The wafer with electrical contacts is shown in Figure S-3b.

The other side of the wafer was then coated with 50 nm of Cr to promote adhesion, followed by HMDS and photoresist spinning. Channels were aligned and patterned in the photoresist, and wafers were temporarily bonded to a silicon carrier wafer for deep reactive ion etching (DRIE) down to the buried oxide layer and fluid vias, creating the vertical-walled electrodes and ICEO posts.

For ICEO operation, metal must coat the sidewalls of these posts, but should be absent from the floor between the posts. Conventional lithography cannot readily be used to pattern metal over this topography because the photoresist will coat the structures unevenly, filling areas between the posts with a thick polymer layer and leaving the edges exposed. The key to this process is *ion milling*, conducted at Cornell University, which preferentially removes metal on horizontal surfaces but not sidewalls. The designs described in this paper were fabricated using this process as detailed below:

After deep silicon etching, the photoresist and Cr masks were removed. Titanium and gold were then conformally coated on the DRIE-etched side to as follows: A titanium

adhesion layer of approximately 50 nm thickness was sputtered in a Technics sputter system (3 minutes in a 30 mTorr argon atmosphere at 350 W incident RF power) followed by a gold layer of approximately 135 nm thickness (3 minutes in a 30 mTorr argon atmosphere at 120 W applied DC power.) This process coated the entire surface, including the vertical sidewalls of the ICEO devices, with a conducting layer, as shown in Figure S-3c. To produce isolated conducting posts, the metallized side was ion milled (Veeco Ion Mill, Cornell Nanofabrication Facility, Ithaca, NY) at 500 V for 4 minutes in a 100 mTorr argon atmosphere. Because the ion milling rate of many metals is highly dependent on incident angle, for instance etching gold on horizontal surfaces 9 or 10 times faster than on vertical surfaces, the resulting devices had metallized vertical sidewalls and an insulating microfluidic channel floor between the ICEO posts. Metal was removed from the tops of the posts as well, as shown in Figure S-3d.

Fluidic fittings were then epoxy bonded (3M Scotch-Weld DP-420) to the top-side of the devices over the fluid via ports, and wires were soldered to the bond pads for electrical contact.

Elastomer lids were fabricated by casting poly(dimethylsiloxane) (PDMS) into a separate silicon mold wafer etched to the same depth as the SOI devices. These parts served as both the lids and insulating channel walls for the devices. Lids were produced by casting Sylgard 182 (Dow Corning) into the silicon molds. The PDMS was mixed in a weight ratio of 10 parts resin to 1 part curing agent, vacuum pumped to remove bubbles, and allowed to cure in the molds for at least three days at room temperature or 1 hour at 60 C.

After removal from the molds, the patterned side of the PDMS was exposed to an air plasma at 9 W RF and approximately 100 mTorr pressure. This treatment made the channels hydrophilic, for easier introduction of aqueous solutions from the fluid ports. Plasma-treated PDMS channels were then aligned with silicon devices by mechanical interlocking. The PDMS served several purposes. It confined the liquid to the area of the channel where the ICEO posts were located, enabled inverted fluorescence microscopy of the channel contents due to its optical transparency, and it provided an insulating barrier between the liquid and the outer silicon channel sidewalls, which remained conducting from the non-photolithographic sputter/ion milling process. The combined silicon and PDMS device is illustrated in Figure S-3e. In these next-generation ICEO mixers, instead of dipping wires into fluid reservoirs, the electric field was applied by attaching clips to wires soldered onto gold pads connected to the through-wafer electrical contacts.

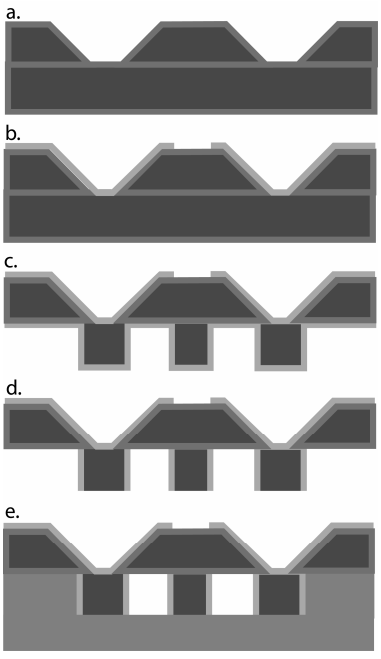

Figure S-3. **(a)** Chemical etching produces fluid and electrical feedthroughs in the low-conductivity side of a silicon-on-insulator wafer. An oxide coating provides electrical insulation. **(b)** Thin-film metal traces make electrical contact through the wafer and oxide, to the highly-conducting silicon on the other side. **(c)** Deep reactive ion etching produces conductive silicon ICEO posts and electrodes on the underside, which are then conformally coated with metal by sputtering. **(d)** Ion milling selectively removes metal from horizontal surfaces on the underside, re-exposing the oxide on the floor of the channel. This electrically isolates the ICEO posts from each other while preserving their metal-coated sidewalls. **(e)** An elastomer lid, molded on a wafer etched to the same depth, interlocks with the electrode features to create a sealed fluidic chamber, with insulating elastomer sidewalls wherever electrodes are not desired. The chamber can be viewed through the elastomer on an inverted microscope stage, while fluid reservoirs and electrical contacts are attached to the top.