Supplementary Material (ESI) for Lab on a Chip

Electronic Supplementary Information

Microfluidic Pneumatic Logic Circuits and Digital Pneumatic Microprocessors for Integrated Microfluidic Systems

Minsoung Rhee[1] and Mark A. Burns[1,2,*]

[1]Department of Chemical Engineering, the University of Michigan

[2]Department of Biomedical Engineering, the University of Michigan

Pressure level visualization through differences in light reflection

The presented pneumatic circuits operate based on the pneumatic Boolean rules (Bit 0 and Bit 1). All input and output ports in a pneumatic circuit maintain either Bit 0 or Bit 1 pressure level. Such binary pressure levels can be easily visualized at the valves with a thin diaphragm membrane. Due to the membrane deflection, any open valve chambers exhibit strong light reflection while closed valves reflect little light. All circuits are built in separate closed systems maintaining the same pressure level over their volume. Regular channels and chambers in the "flow" layer do not have deflectable membranes so that it might be difficult to distinguish their pressure levels visually. However, one can easily infer their pressure levels by visually checking the pressure level at the valve connected to the channels.

Utilization of pneumatic signals for pumping, venting, and fluid routing

Pumping, venting, droplet positioning, or fluid routing is achievable with such microprocessors. Such actuators (i.e., pumps, channel crossovers) utilize the layer-separating air-permeable PDMS membrane that stops liquid flow but allows air to pass. When vacuum signals are supplied to the bottom part, due to the deflected membrane, the upper part experiences an abrupt pressure decrease at the same time. When the vacuum in the pump vanishes, the upper part restores its original pressure. However, if the vacuum input in the bottom part persists for a while, the air-permeable membrane will allow air in the upper channel to vent slowly. The ability of such actuators to actively control the movement of liquid in

the channel thus can help many other microfluidic applications such as selective routing, controlled reaction, and convective mixing. Figure S-10 shows a 8-bit digital pneumatic processor capable of converting serial input data (8-bit commands) to eight final output signals used to control membranous air-bypasses for liquid positioning. Depending on the command and its parallelized outputs, drops of liquid or air-bubbles will be guided toward specific air-bypass positions. Successive commands will let the drops or bubbles move around in the channel independently for drop merging, mixing, and selective reaction.

Other materials for pneumatic microprocessor construction

Although all devices presented here have been fabricated in PDMS, a wide variety of materials can be used for a whole or parts of the devices in order to suit specific needs, including silicon and glass, especially for the tasks involved with PDMS-incompatible solvents. The normally closed pneumatic valves can be also constructed with diaphragms made in different elastomers *(1-2)* that may exhibit less air-permeability. However, applications of air pumping or venting may become very limited with such airtight materials, since pumping mechanics is based on the slow air flow through the porous membrane. In our PDMS systems, air leaking through the valve membrane does not cause any critical operational problems since the membrane itself is an extremely high resistance to air flow and all circuits produce and

deliver new full strength pneumatic signals to the consecutive circuits.

References

1. P. A. Willis, B. D. Hunt, V. E. White, M. C. Lee, M. Ikeda, S. Bae, M. J. Pelletier, and F. J. Grunthaner, *Lab Chip* **7**, 1469-1474

2. W. H. Grover, M. G. von Muhlen, S. R. Manalis, *Lab Chip, 2008,* **8**, 913-918.

Table S-1. Truth Table for Pneumatic NOR Logic Gate

INPUT 1	INPUT 2	OUTPUT
Atmosphere	Atmosphere	Vacuum
Atmosphere	Vacuum	Atmosphere
Vacuum	Atmosphere	Atmosphere
Vacuum	Vacuum	Atmosphere

Table S-2. Truth Table for Pneumatic NAND Logic Gate

INPUT 1	INPUT 2	OUTPUT
Atmosphere	Atmosphere	Vacuum
Atmosphere	Vacuum	Vacuum
Vacuum	Atmosphere	Vacuum
Vacuum	Vacuum	Atmosphere

Table S-3. Truth Table for Pneumatic XNOR Logic Gate

INPUT 1	INPUT 2	OUTPUT
Atmosphere	Atmosphere	Vacuum
Atmosphere	Vacuum	Atmosphere
Vacuum	Atmosphere	Atmosphere
Vacuum	Vacuum	Vacuum

Table S-4. Truth Table for Pneumatic XOR Logic Gate

INPUT 1	INPUT 2	OUTPUT
Atmosphere	Atmosphere	Atmosphere
Atmosphere	Vacuum	Vacuum
Vacuum	Atmosphere	Vacuum
Vacuum	Vacuum	Atmosphere

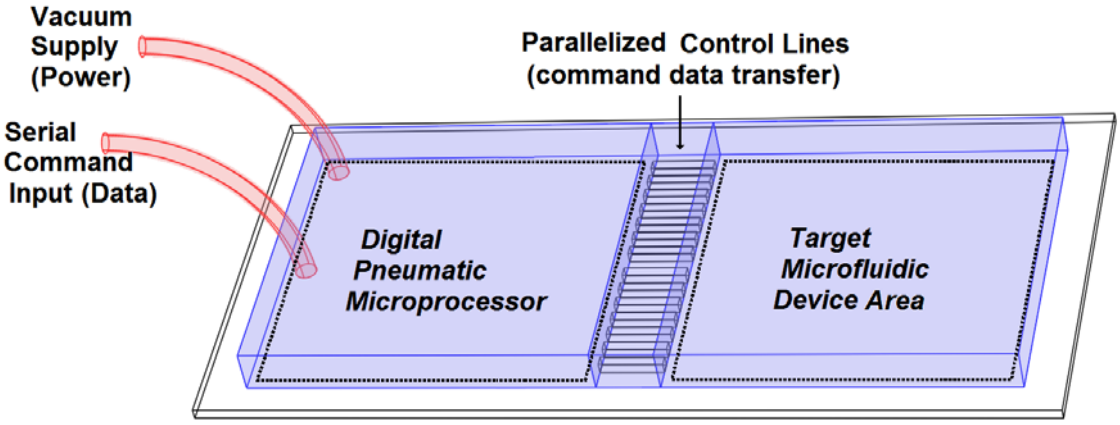

Figure S-1. Schematic concept of a pneumatic microprocessor embedded in a target microfluidic device. The microprocessor is connected to the vacuum reservoir and receives serially-encoded pneumatic commands from a *single* input line, parallelizes the command using various logic circuits, and transfers the decoded commands to multiple on-chip control lines in the target device.

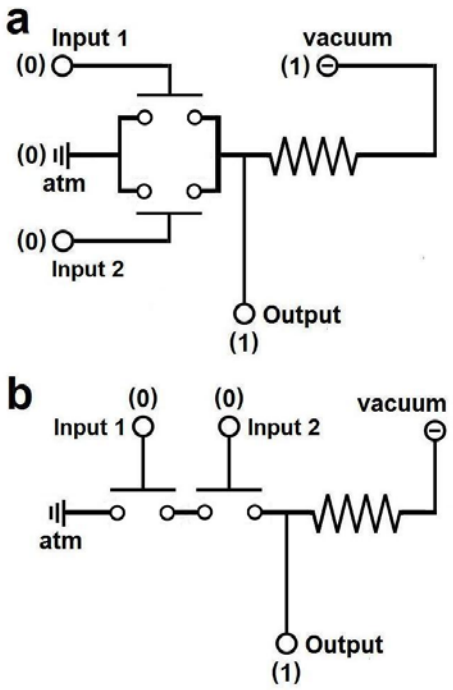

Figure S-2. Schematics of universal pneumatic logic gates constructed by modifying the asymmetric pneumatic inverters. (a) NOR gate with two parallel inputs, producing the output of 1 at the inputs of 0 and 0. (b) NAND gate with two sequential inputs, producing the output of 1 at the inputs of 0 and 0.

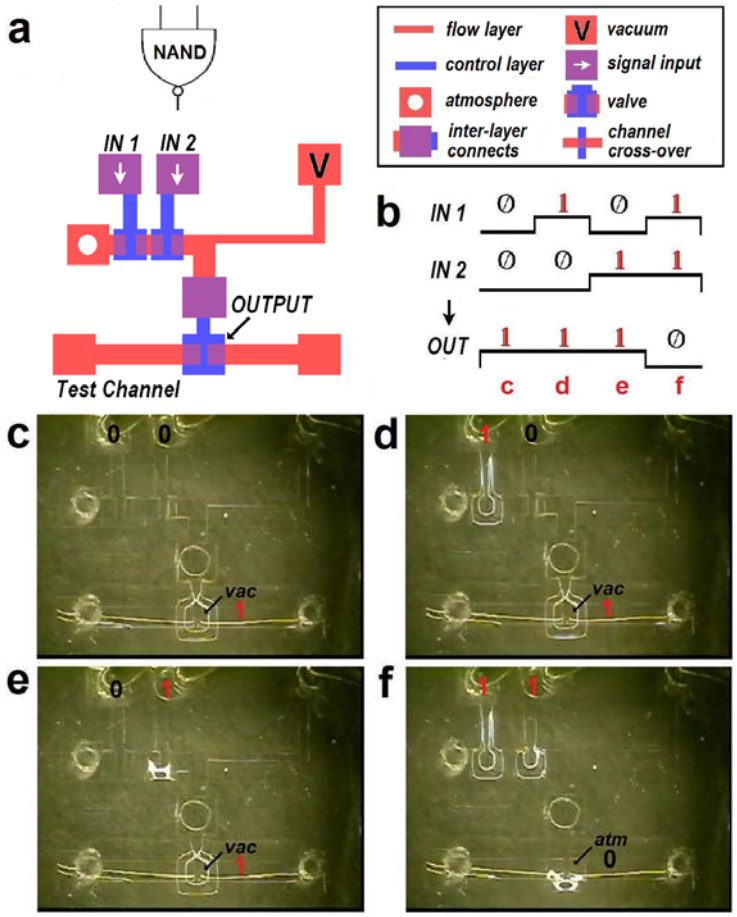

Figure S-3. NAND gate schematic and operation. (a) CAD design of a NAND gate. In this and later figures, the bottom 'control' layer is shown in blue while the upper 'flow' layer is in red. The overlapped regions are visible in violet. Red squares with an empty circle are the holes that remain open to atmosphere during operation and those with 'V's indicate connections to vacuum reservoir. White arrows in the squares show the signal input locations and violet squares represent inter-layer connections between the bottom and upper layers. Channel crossovers between two layers are also shown in violet, but not as an individual square. (b) Output variations depending on two inputs. (c) NAND gate working with the 0-0 input. The output channel shows deformation or increased light reflection around the boundaries due to the existing vacuum (i.e., an output state of 1). (d) NAND gate with the 1-0 input. The left input valve is open while the right remains closed. (e) NAND gate with a 0-1 input and (f) NAND gate with a 1-1 input. The output channel is now connected to atmosphere and light reflection decreases as the channel redeems the original shape.

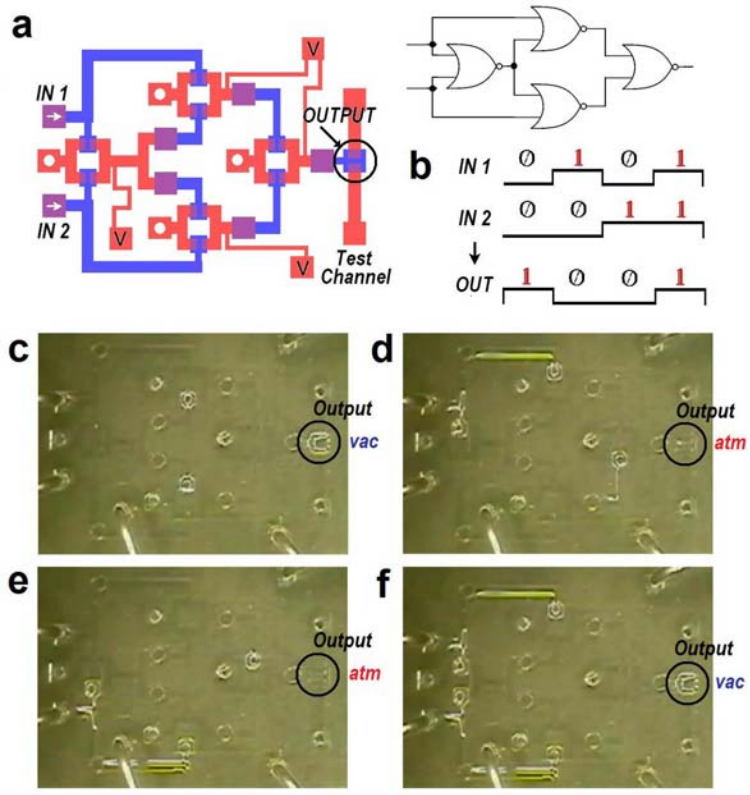

Figure S-4. XNOR gate operations. (a) CAD design of a XNOR gate. (b) Output variations depending on two inputs. (c) XNOR gate working with the 0-0 input. The output valve shows deformation due to the existing vacuum. (d) XNOR gate with the 1-0 input. The output valve now returns closed and its reflection disappeared. (e) XNOR gate with the 0-1 input. (f) XNOR gate with the 1-1 input. The output valve opens again.

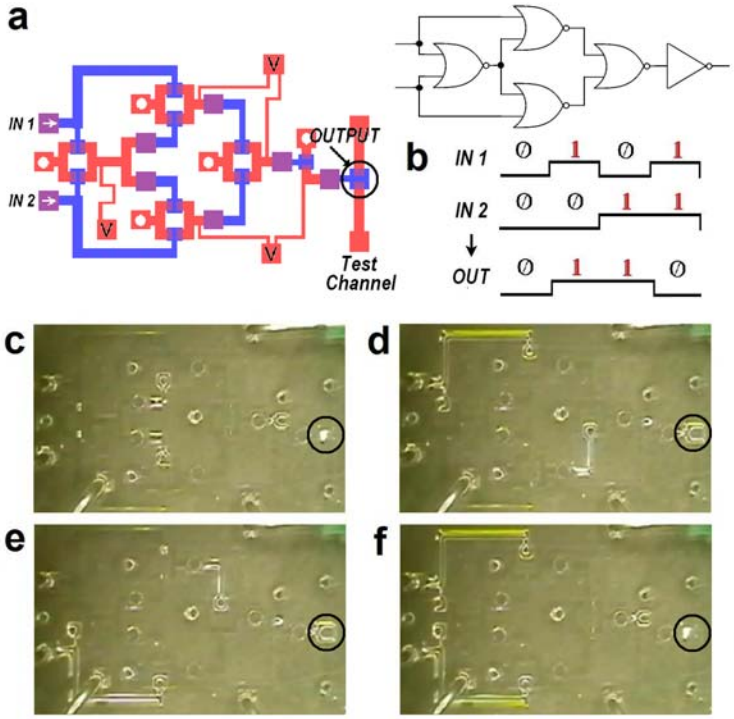

Figure S-5. XOR gate schematics and operations. (a) CAD design of a XOR gate. (b) Output variations depending on two inputs. (c) XOR gate working with the 0-0 input. The output valve will not open. (d) XOR gate with the 1-0 input. The output valve opens and shows deformation due to the existing vacuum. (e) XOR gate with the 0-1 input. (f) XOR gate with the 1-1 input. The output valve closes again.

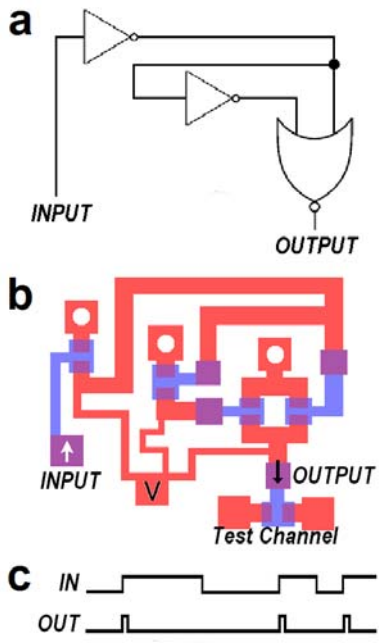

Figure S-6. Schematics of a positive edge detector. (a) Electrical representation. (b) CAD design. (c) Representation of output pneumatic signal variations. The device detects positive rises of pneumatic signals and produce a short (<200ms) pulse at every rise.

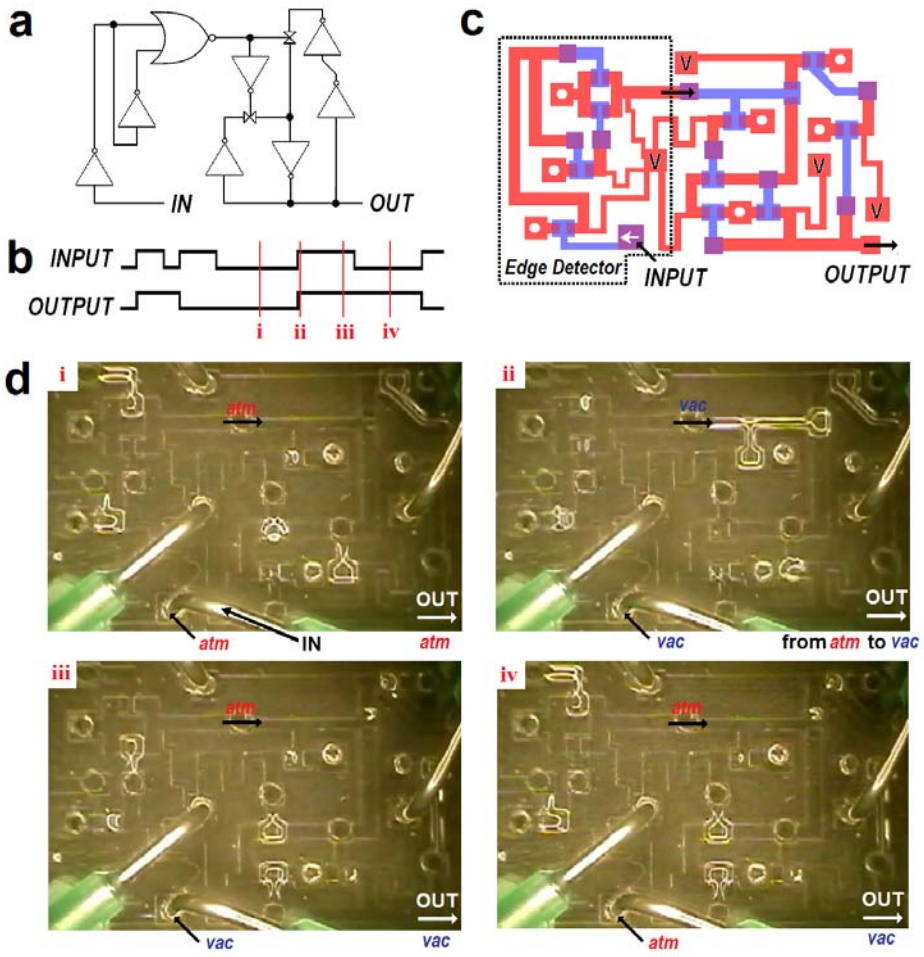

Figure S-7. Schematics and operations of a microfluidic toggle. (a) Electrical representation. (b) Output variations depending on the input signals. Every positive input signal switches the pressure level of output at its rising stage. (c) CAD design. (d) Sequential operations of the toggle function. Each frame corresponds to the signal status numbered in Figure 15c; *i)* toggle is at rest with the 0 (*atm*) input, the output is set to 0, *ii)* as soon as the toggle is fed with a 1 (*vac*) input, this positive rise in signal produces a transient vacuum signal at the embedded edge detector. The output then rapidly changes from *atm* to *vac*, *iii)* the transient vacuum signal vanishes after the output change is done, and *iv)* when the toggle is back at rest, the new output remains changed.

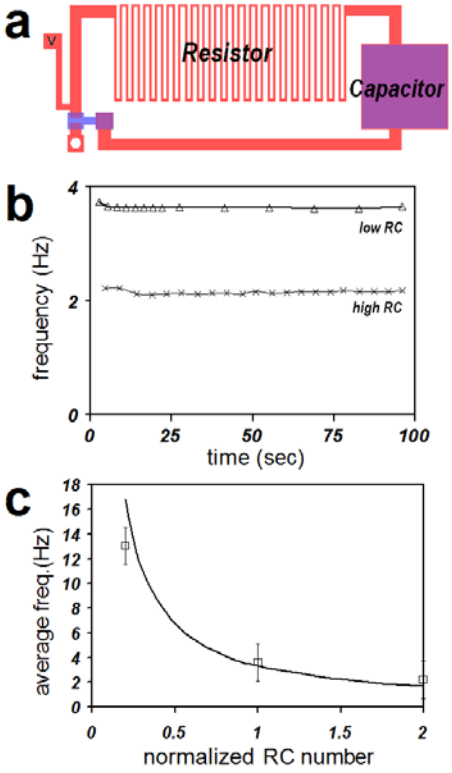

Figure S-8. Pneumatic clock generator. (a) CAD design of a clock generator. The clock frequency will be determined by characteristics of the embedded “resistor” and “capacitor.” (b) Plot of clock frequencies over time. The obtained clock frequencies show high stability over time. (c) Plot of average clock frequencies versus normalized RC numbers. Clock generators with a higher RC number tend to produce clock pulses with lower frequencies. The RC numbers were normalized against that of the clock generator with an intermediate frequency. Higher resistance and capacitance yield clock pulses of lower frequencies while at a lower RC number, the generated clock pulses have a higher frequency.

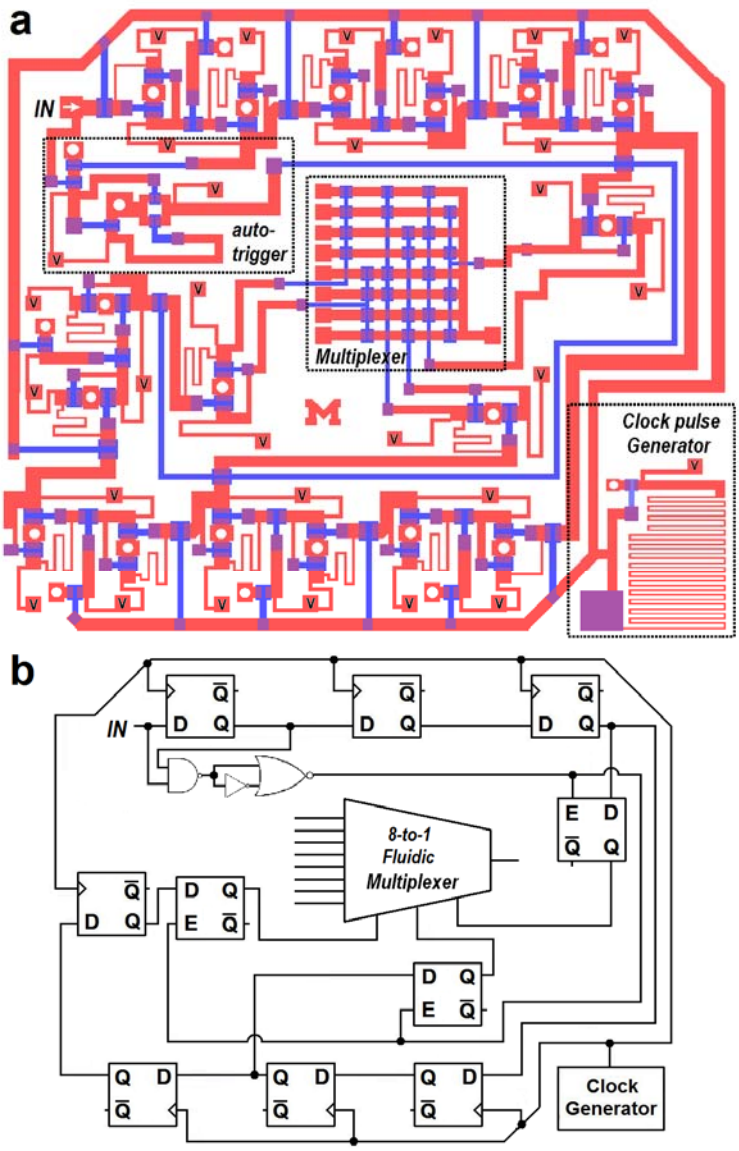

Figure S-9. 3-bit digital pneumatic microprocessor capable of auto-clocking and auto-triggering. This processor runs from a *single* input line and the clock pluses are generated autonomously as well as the triggering signals. Three parallel outputs allow for multiplexing eight individual channels. (a) CAD design and (b) electrical symbolic representation.

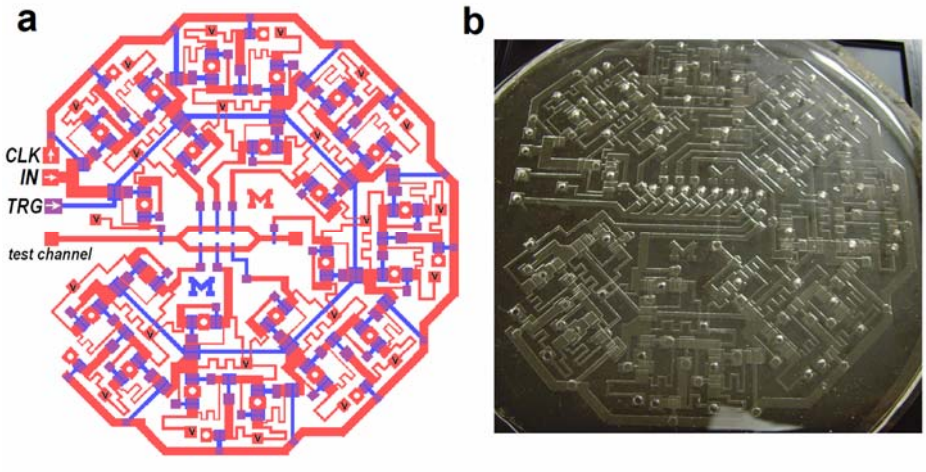

Figure S-10. Multipurpose 8-bit digital pneumatic microprocessor for venting and positioning. (a) CAD design of the 8-bit processor that produces eight parallel independent outputs from serially-encoded input commands. The output from each bit of the command actuates a membranous pump at the specific location to position, direct, and route fluid flows in the test channel. (b) Photo of the same 8-bit processor with different target test channels.