Supplementary Material (ESI) for Lab on a Chip

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Electronic Supplementary Information



Fig. S1. The fabrication of PS/PtOEPK thin film well. First is the fabrication of the PDMS stamp. SU-8 was spincoated on to a silicon wafer and prebaked at 65°C and 95°C for allotted amount of time. Photomask was placed on SU-8 and exposed to ultraviolet light. (a) Exposed SU-8 was postbaked and developed to reveal wells. (b) The master was silanized and PDMS was poured onto the SU-8 master and (c) cured on 75°C hotplate for 2 hours and was removed. The next step involved the patterning of PS/PtOEPK. (d) A PS/PtOEPK/Toluene solution was deposited on a coverglass and set aside for 24 hours for toluene evaporation. (e) PDMS was placed on PS with additional weight to insure close contact and was sat on a 100°C hotplate for 15 minutes. (f) PDMS, coverglass, and weight were cooled and removed from hotplate. The PDMS and weight were removed to reveal patterned PS. (g) The coverglass was released from microwells.